university of groningen

kvi - center for advanced
radiation technology
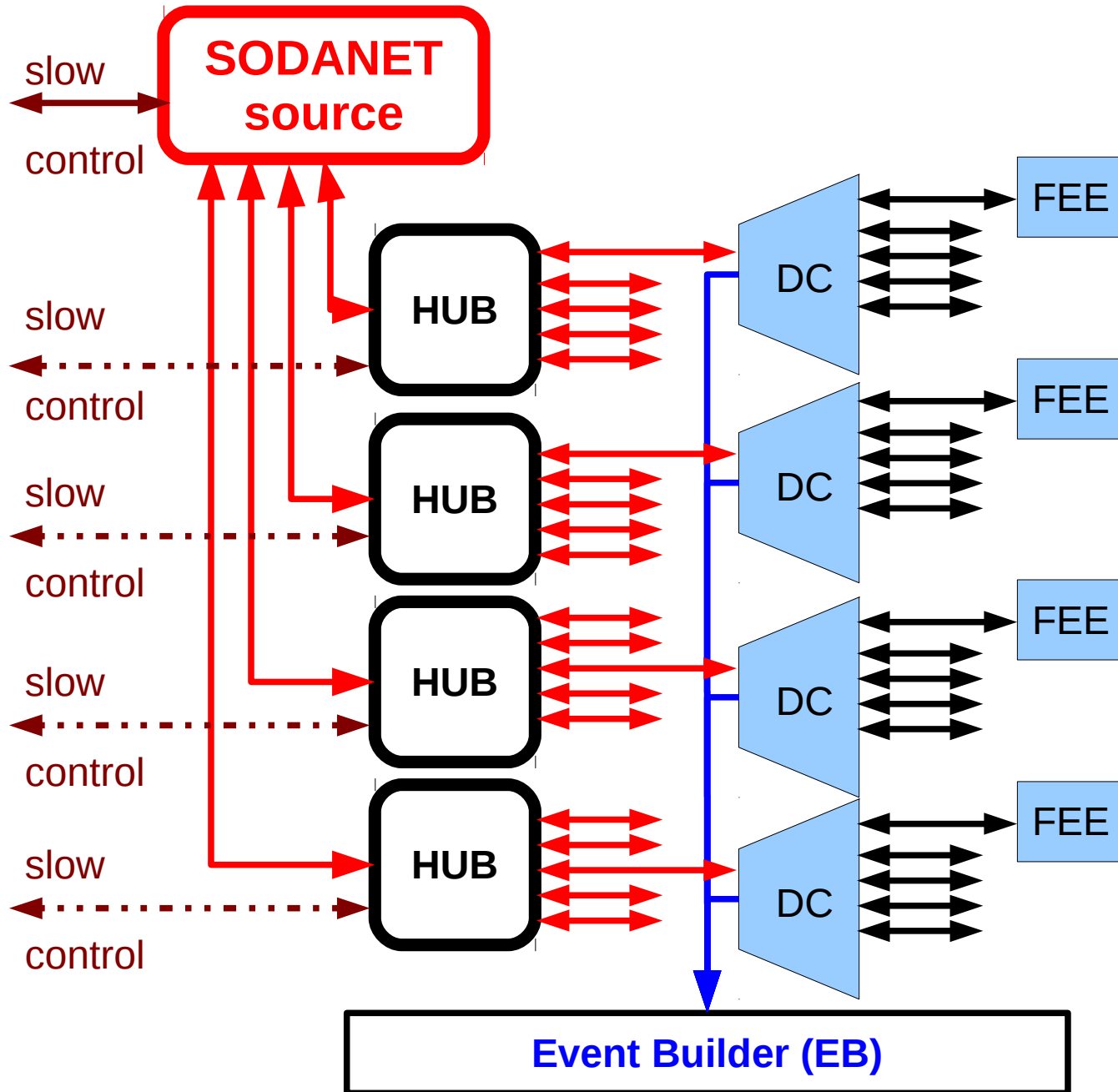
Status of the SODANET

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for the PANDA collaboration

SODANET Topology

SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
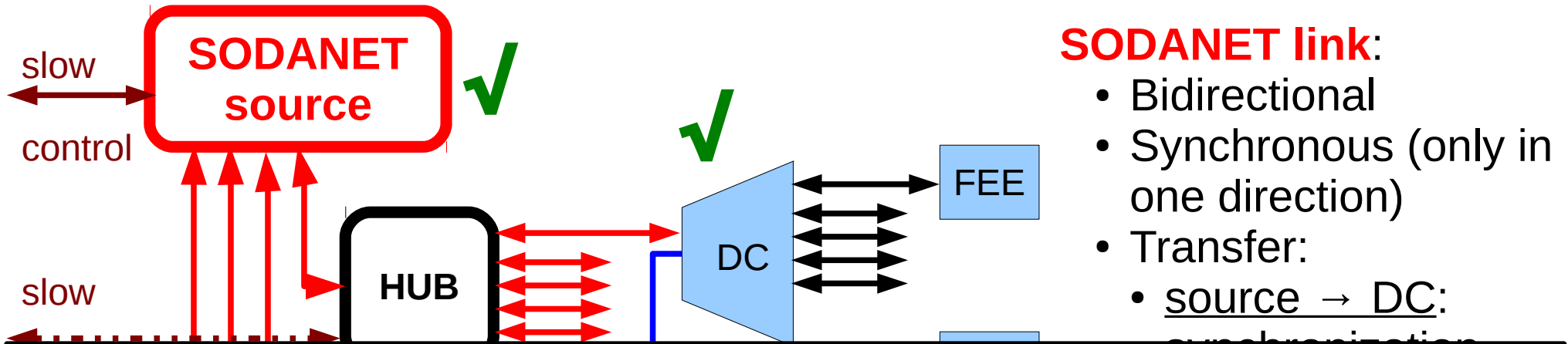 - DC → source: slow control, used for time calibration

Data link (DC → EB):
- Unidirectional Ethernet

Link DC ↔ FEE:
- Bidirectional, synchronous
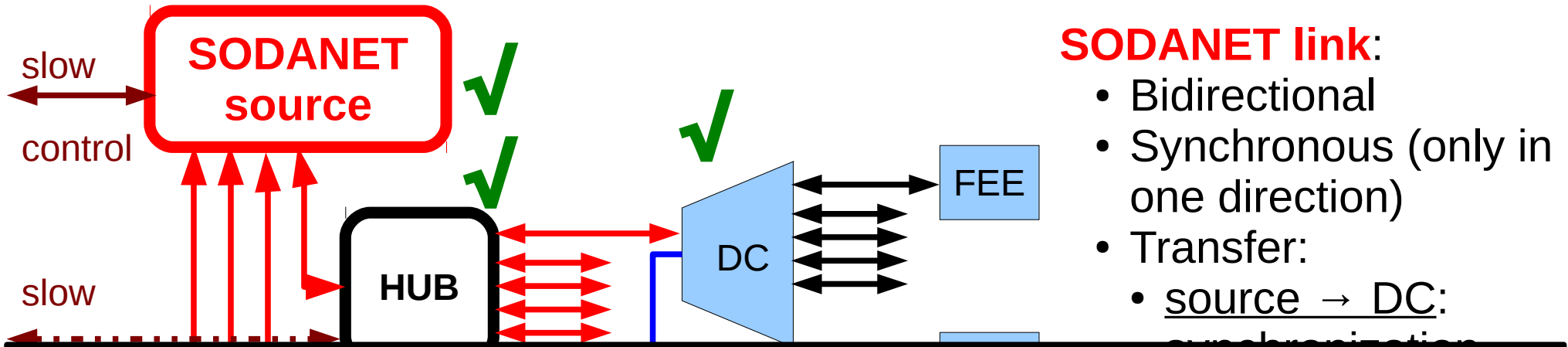- Protocol up to subsystem

SODANET Topology

slow

control

slow

SODANET source ✓

✓

HUB

DC

FEE

SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: ~~synchronization~~

Since before summer stable operation was only achieved

for point-to-point connection, bypassing

SODANET hub (required for multiple endpoints):

a "split" version SODA-NET has been developed:

slow-control data and synchronous commands

were sent using separate fibres.

~~synchronous~~

Event Builder (EB)

- Protocol up to subsystem

SODANET Topology

slow

control

SODANET source ✓

✓

✓

slow

HUB

DC

FEE

SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization

This summer core components of the SODANET were Re-implemented, which resulted in a working system:

SODANET is completely implemented and tested on:

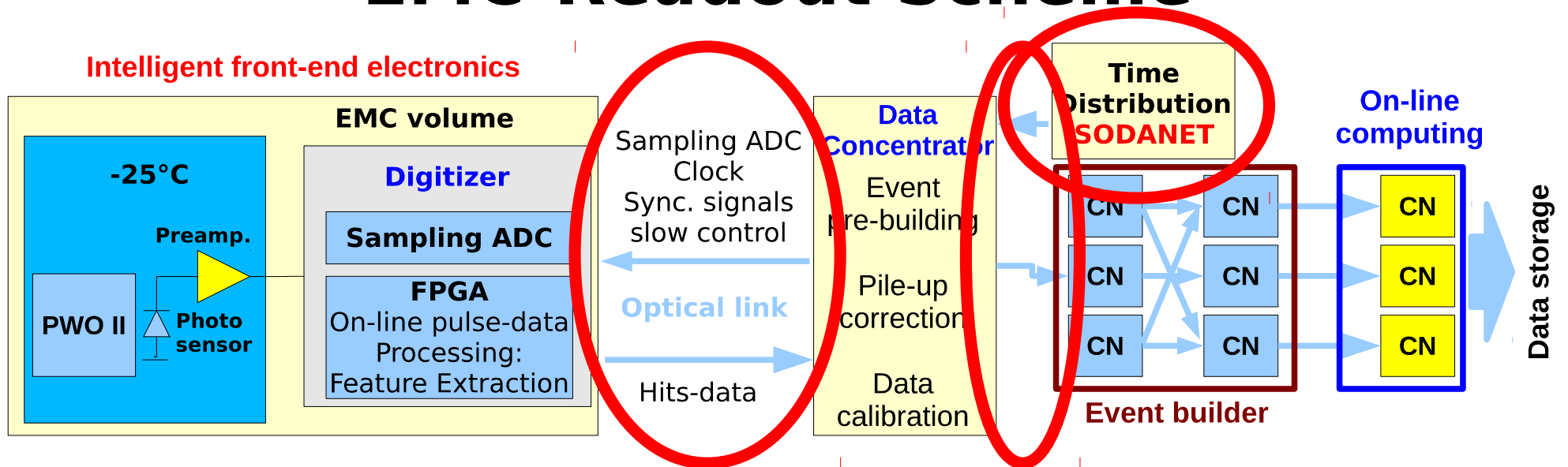**Lattice FPGA (ECP3, TRBv3), used by STT, DIRC, LUMI**
Xilinx FPGA (Kintex-7), used by SODANET network, EMC, MVD

So far SODANET is integrated only into the EMC readout

synchronous
- Protocol up to subsystem
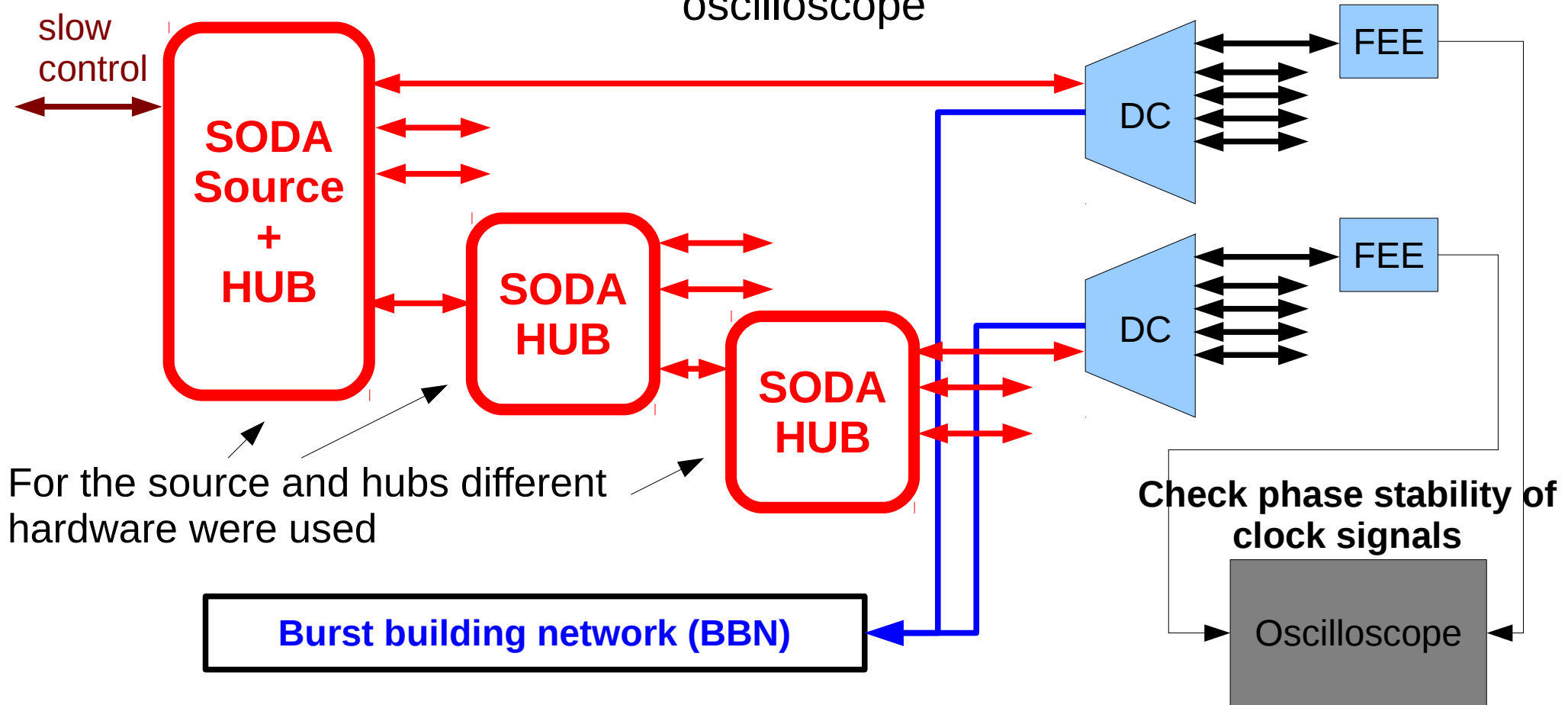
Event Builder (EB)

4

EMC-Readout Scheme

Components of the EMC readout:

- Intelligent front-end: **digitizer**

- Time-distribution system

- Data concentrators

- Burst-building network

- On-line computing

SODANET Test System
Clocking

During test relevant SODANET links were randomly disconnected and after recovery of the system stability of the clock-signal phase was checked with oscilloscope

slow control

SODA Source + HUB

SODA HUB

SODA HUB

DC

DC

FEE

FEE

Check phase stability of clock signals

Oscilloscope

For the source and hubs different hardware were used

Burst building network (BBN)

Systems with up to three levels of SODANET hubs did not show any instability

SODANET Test System
Synchronisation

Signal from one pulse generator was measured by two different front-ends.

During measurement FEE modules were reset to test synchronisation procedure
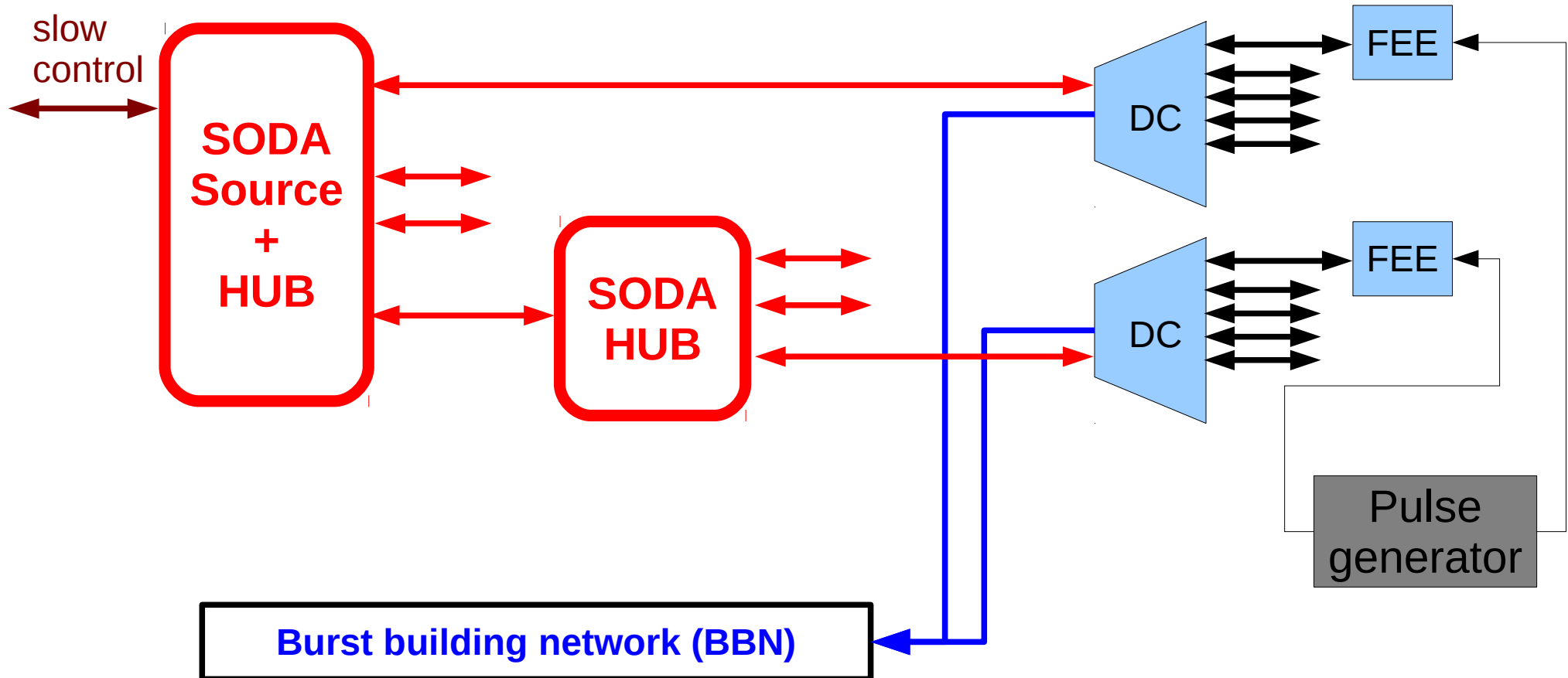
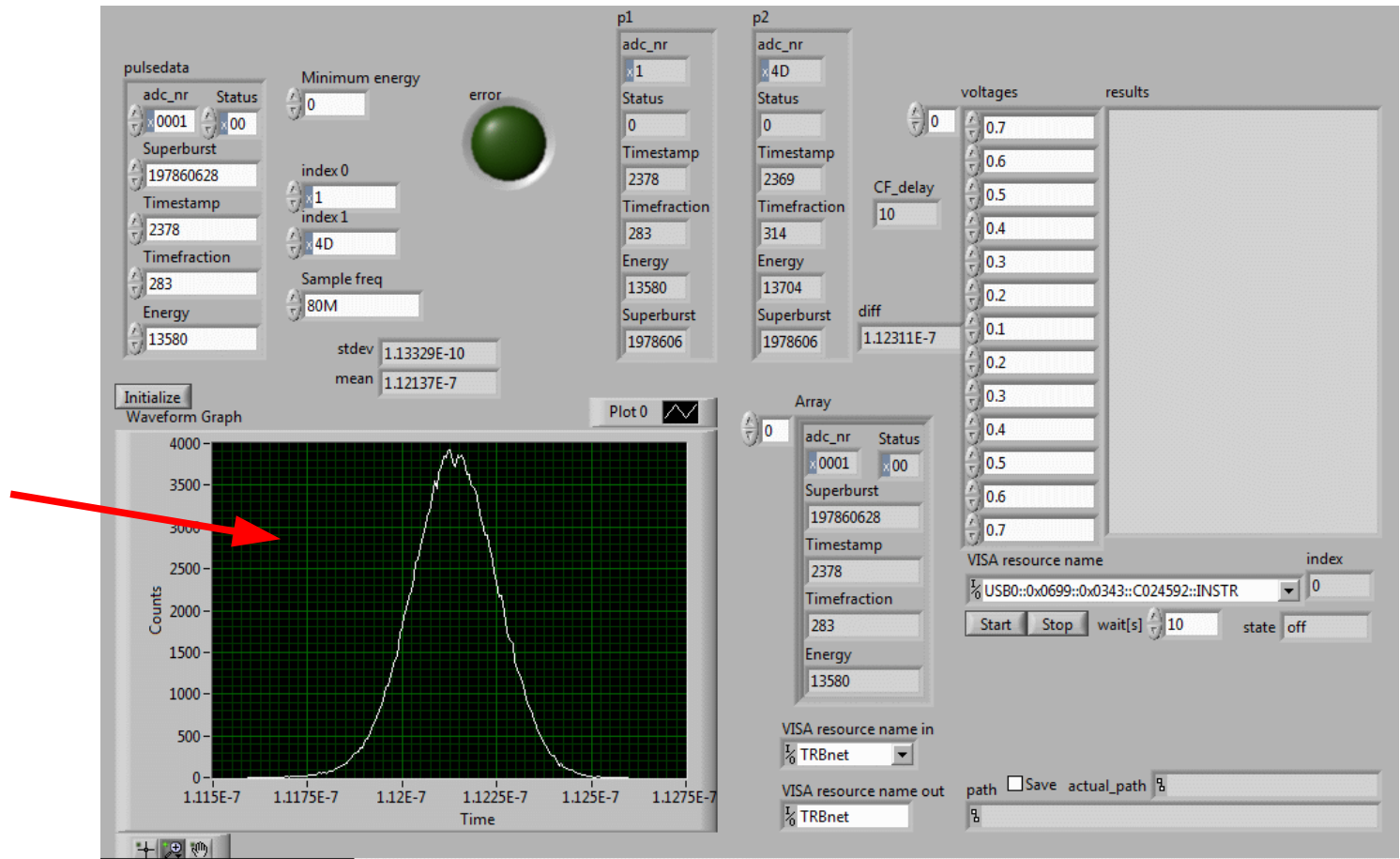Time-stamps of measured pulses were compared:

time difference should be constant

SODANET Test System
Synchronisation

Signal from one pulse generator was measured by two different front-ends.

During measurement FEE modules were reset to test synchronisation procedure

Measured time-difference between detected pulses

Measured time difference is constant →

synchronisation is working properly

Summary

- All components of the SODANET are **implemented** and **tested** on Lattice (ECP3, TRBv3) and Xilinx (Kintex7) platforms

- **SODANET is ready** for implementation for **ALL PANDA subsystems**:
    - EMC – done
    - DIRC, STT (TDC readout) – in progress
    - MVD – ?

Outlook

TRBv3 platform is being used for R&D only:

- SODANET network should be based on Xilinx platform (gain of network speed from max 2.4 Gb/s to 10 Gb/s)

- Lattice ECP3/5 FPGAs should be used as TDC front-ends (not a data concentrators)