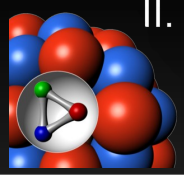

II. Physikalisches Institut

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

PTDAQ

M. N. Wagner, S. P. Reiter

in behalf of the $\overline{\text{P}}$ANDA Collaboration

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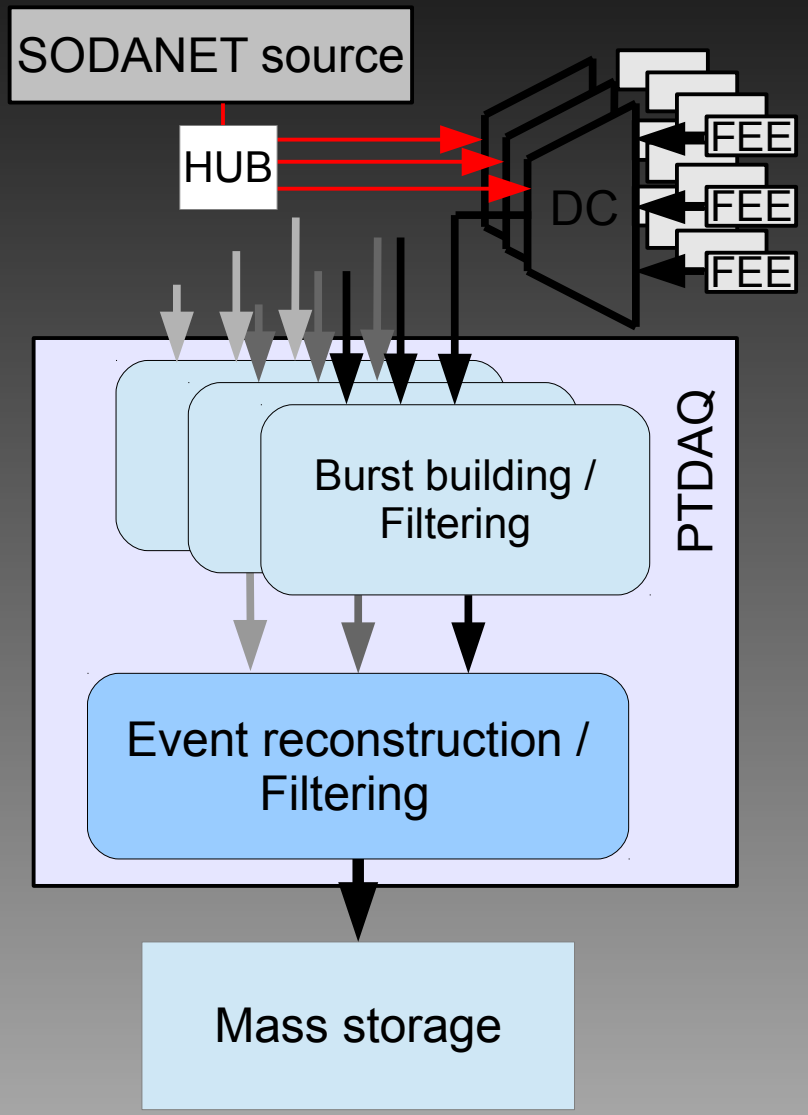
Bundesministerium für Bildung und Forschung

HGS-HIRe for FAIR
Helmholtz Graduate School for Hadron and Ion Research

HIC for FAIR
Helmholtz International Center

Prototype Trigger-less Data Acquisition (PTDAQ)

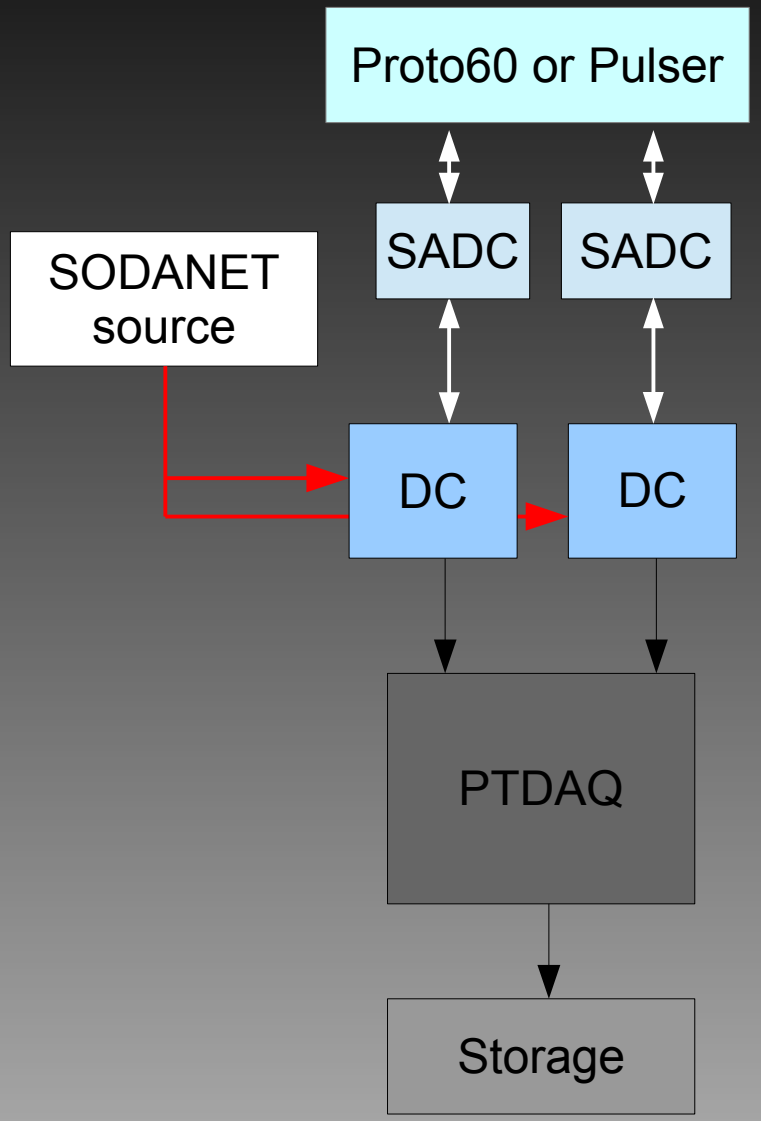


Functionality:

- Digitalized data front end electronic synchronized at data concentrator
- Burst building and first filter algorithm
- Event reconstruction and second stage of filter algorithm

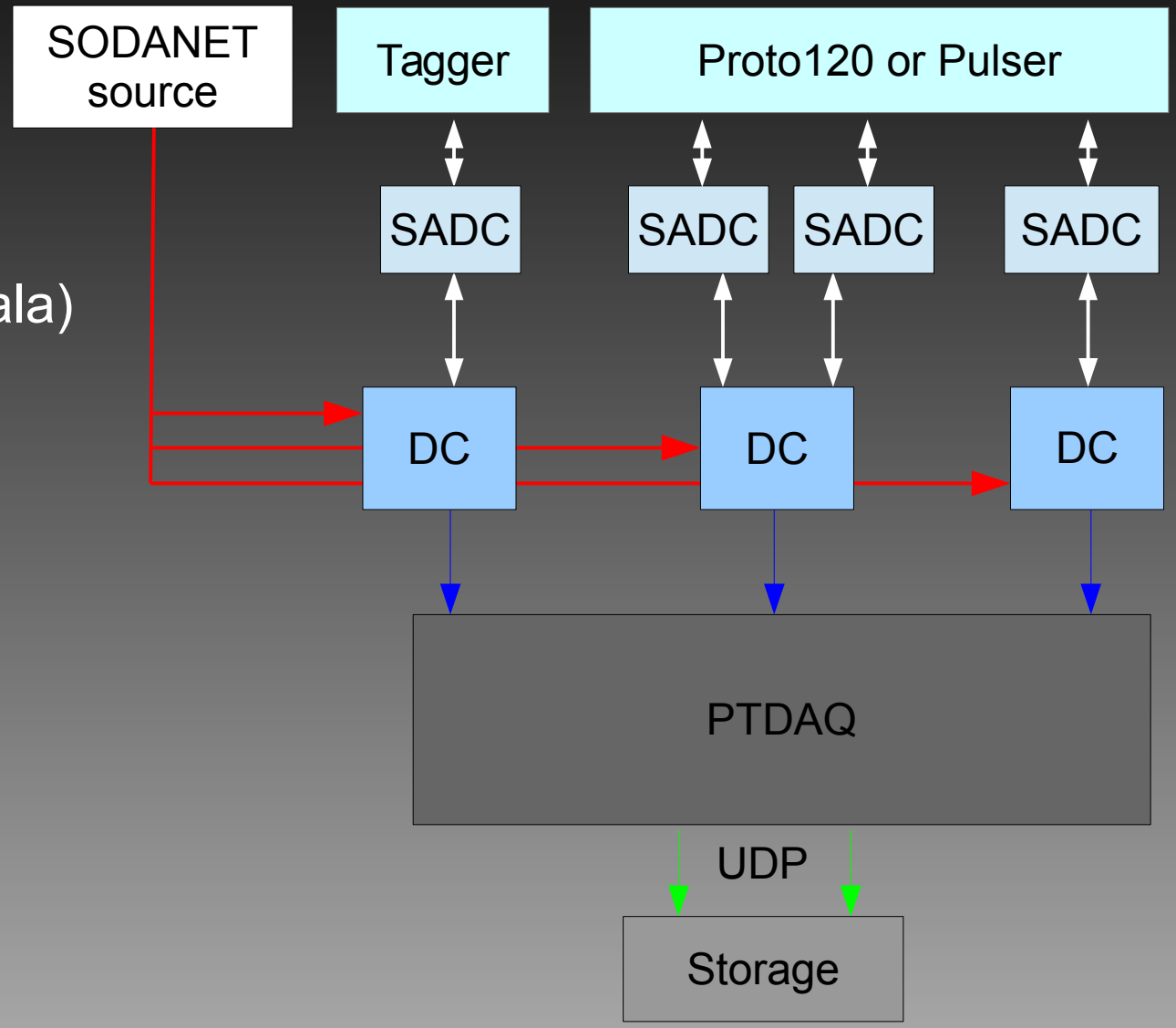
Gießen DAQ-Chain Test

- DAQ chain
- Detector/Pulser
- 2 Sampling ADC (Uppsala)
  - Feature extraction mode
- 1 TRBv3
  - 2 Data concentrator
  - 1 SODANET source
- 1 xFP version 3
  - Burst-builder
  - (Filtering)



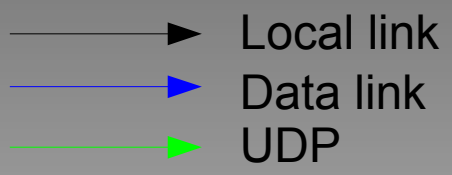
New Gießen DAQ-Chain Test

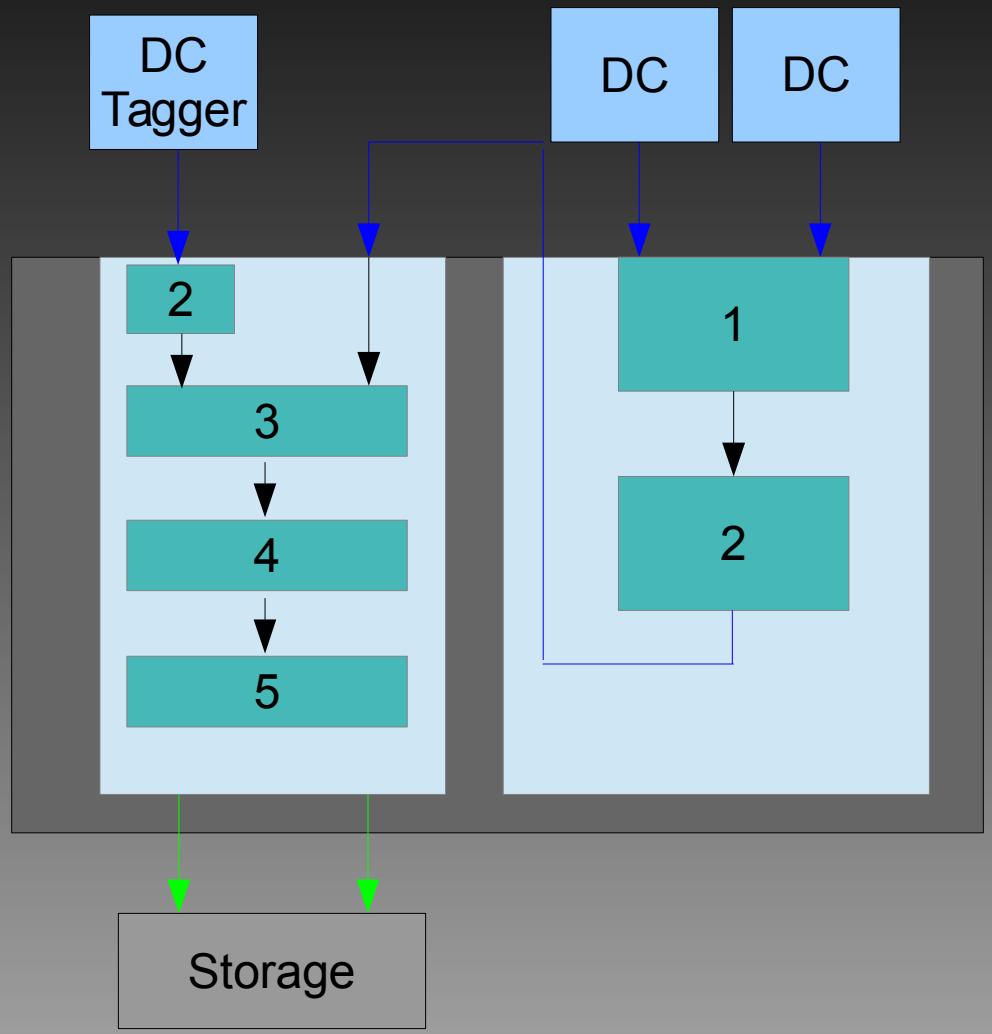
- DAQ chain
- Detector/Pulser
- 4 Sampling ADC (Uppsala)
  - Feature extraction mode
  - Waveform Mode
- 2 TRBv3
  - 3 Data concentrator
  - 1 SODANET source
- 1 - 3 xFP version 3
  - Burst-builder
  - (Filtering)



New Gießen DAQ-Chain Test

1. Merger
2. Zero suppression
3. Burst builder
4. Tagger filter
5. SBN filter





Outlook

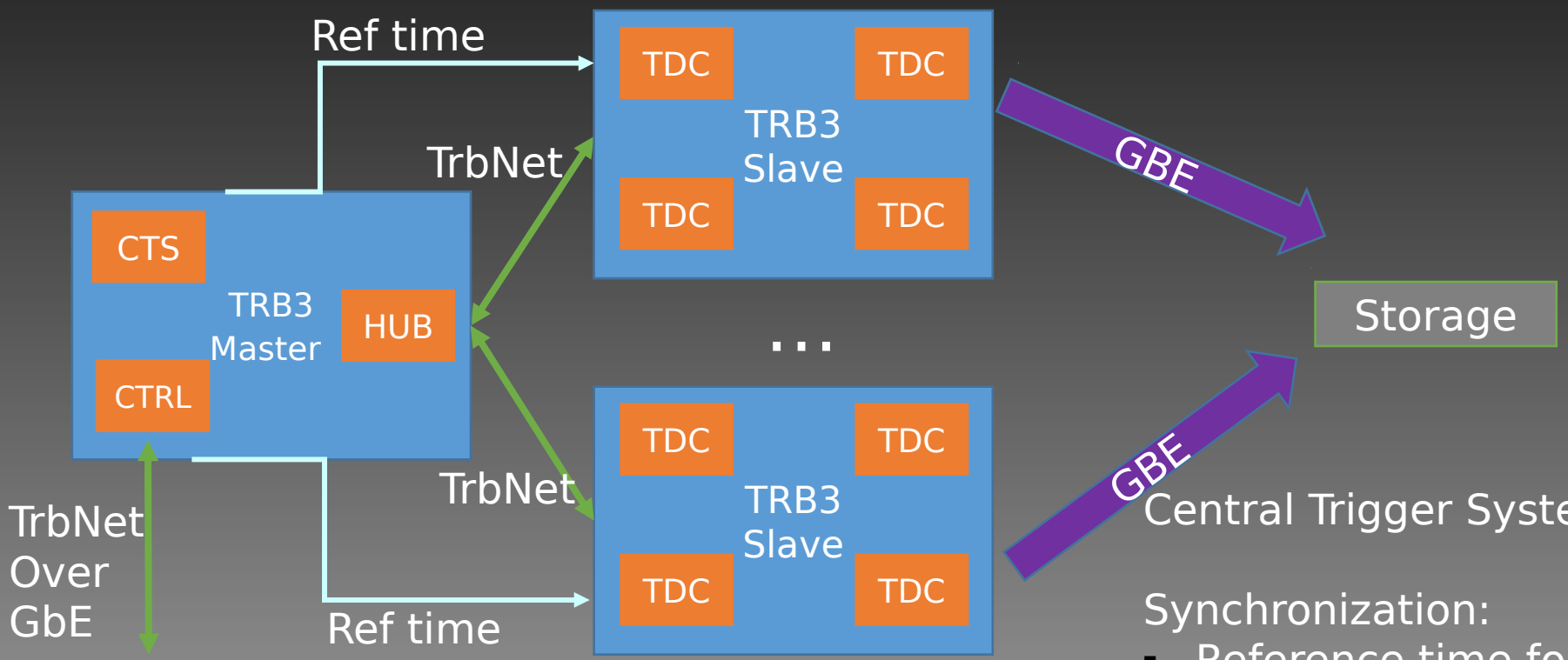
- In Beam environment
  - 11.12.15 – 14.12.15 at MAMI Mainz
  - Proto120 + Tagger + Veto
- Simon is working on CRORC (next talk)
  - Common Read-Out Receiver Card (Alice)
  - From optical via PCIe to storage

TRBv3 as SODANET Endpoint for the Straws

G. Korcyi

in behalf of the $\overline{\text{P}}$ANDA Collaboration

Multiple TRBv3s – Master & Slave

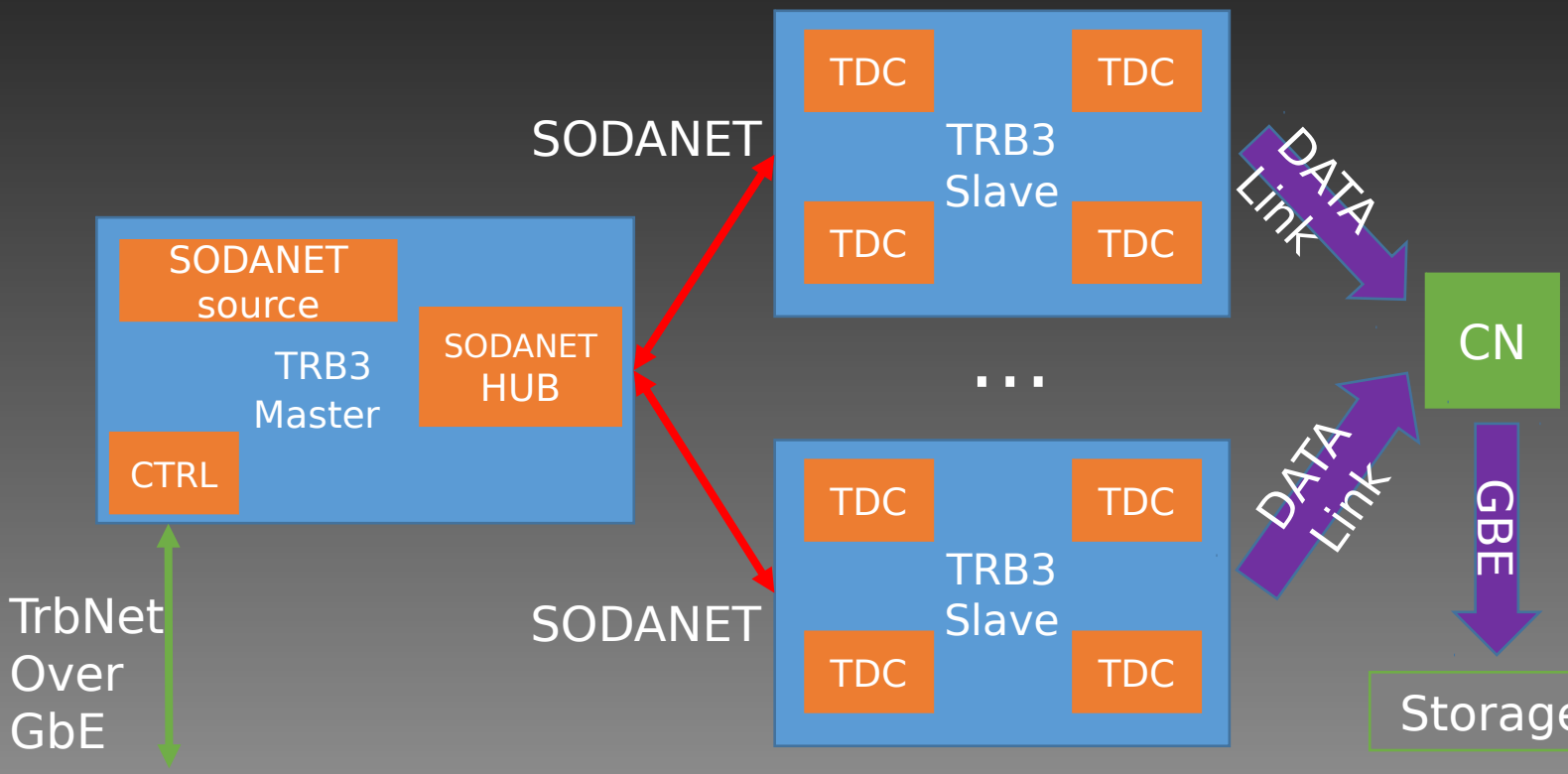


Central Trigger System

Synchronization:
- Reference time for TDCs
- LVL1 TrbNet readout request

Event building on PC

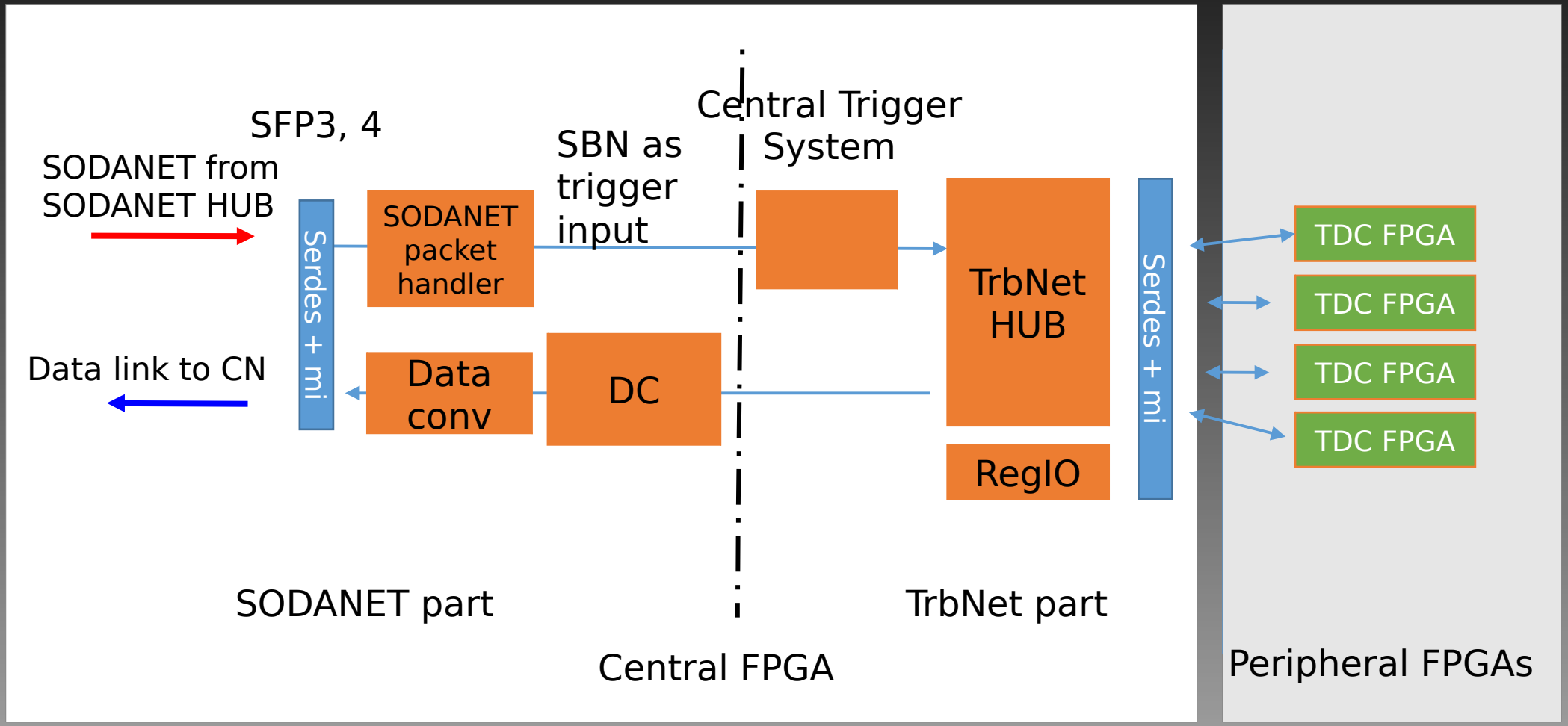
Multiple TRBv3s – SODANET



Fixed readout rate from SODANET source

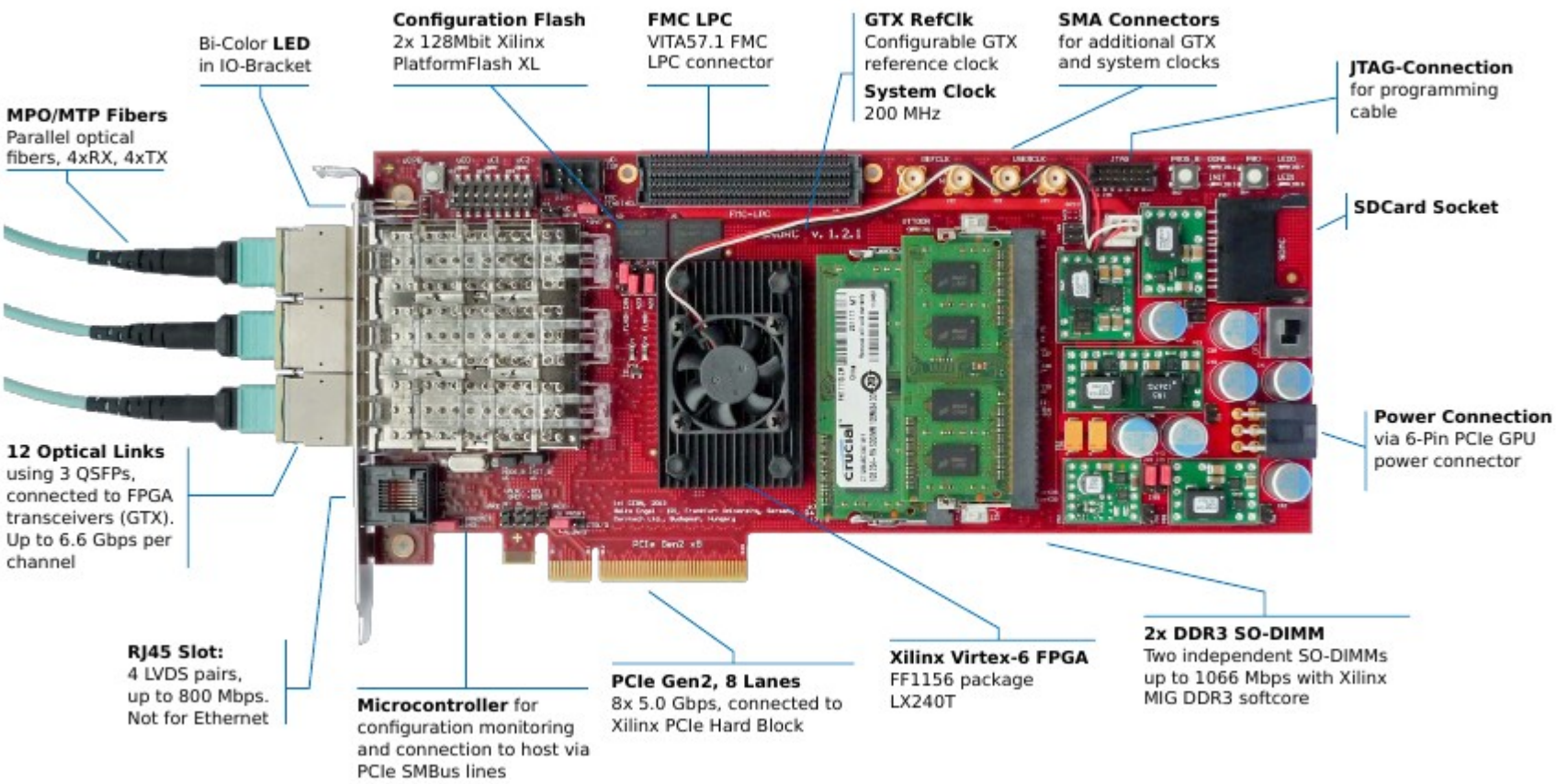
Synchronization by SODANET superburst updates

Slave TRBv3s as an Endpoint

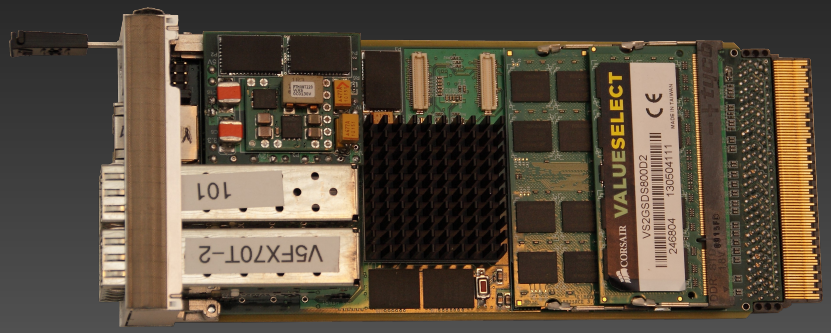


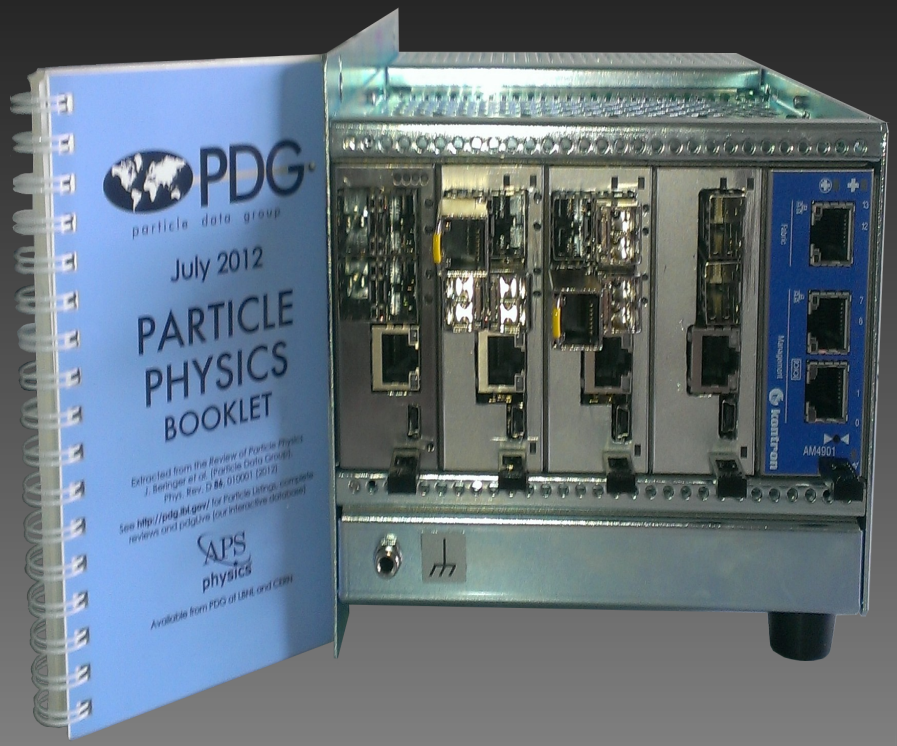
Backup

C-RORC Overview



Hardware Components





xFP board:

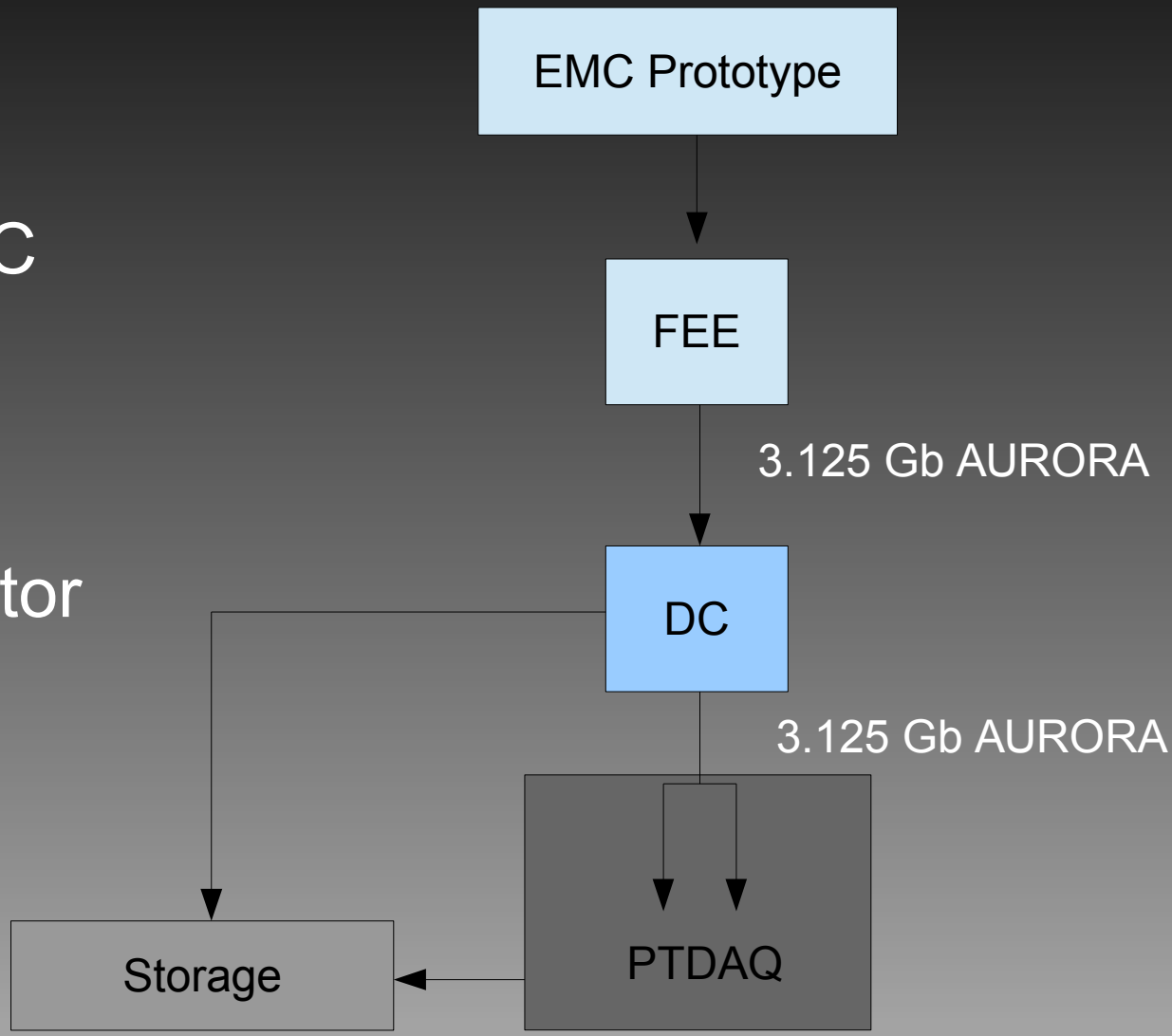
- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
  - 6.25 Gbit optical
- 1 Gb Ethernet

Micro TCA shelf:

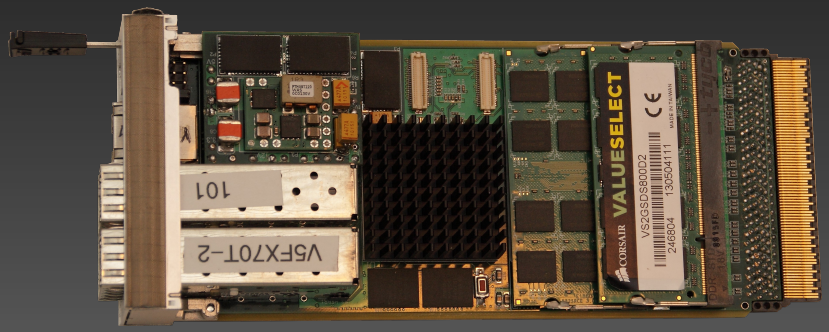
- Up to 4 xFP
- Up to 9 data concentrators

MAMI Test Setup

- DAQ chain
  - 1 Sampling ADC
  - Pile-up mode
- 1 xFP version 2
  - Data concentrator
- 1 xFP version 3
  - Burst-builder



Used Hardware



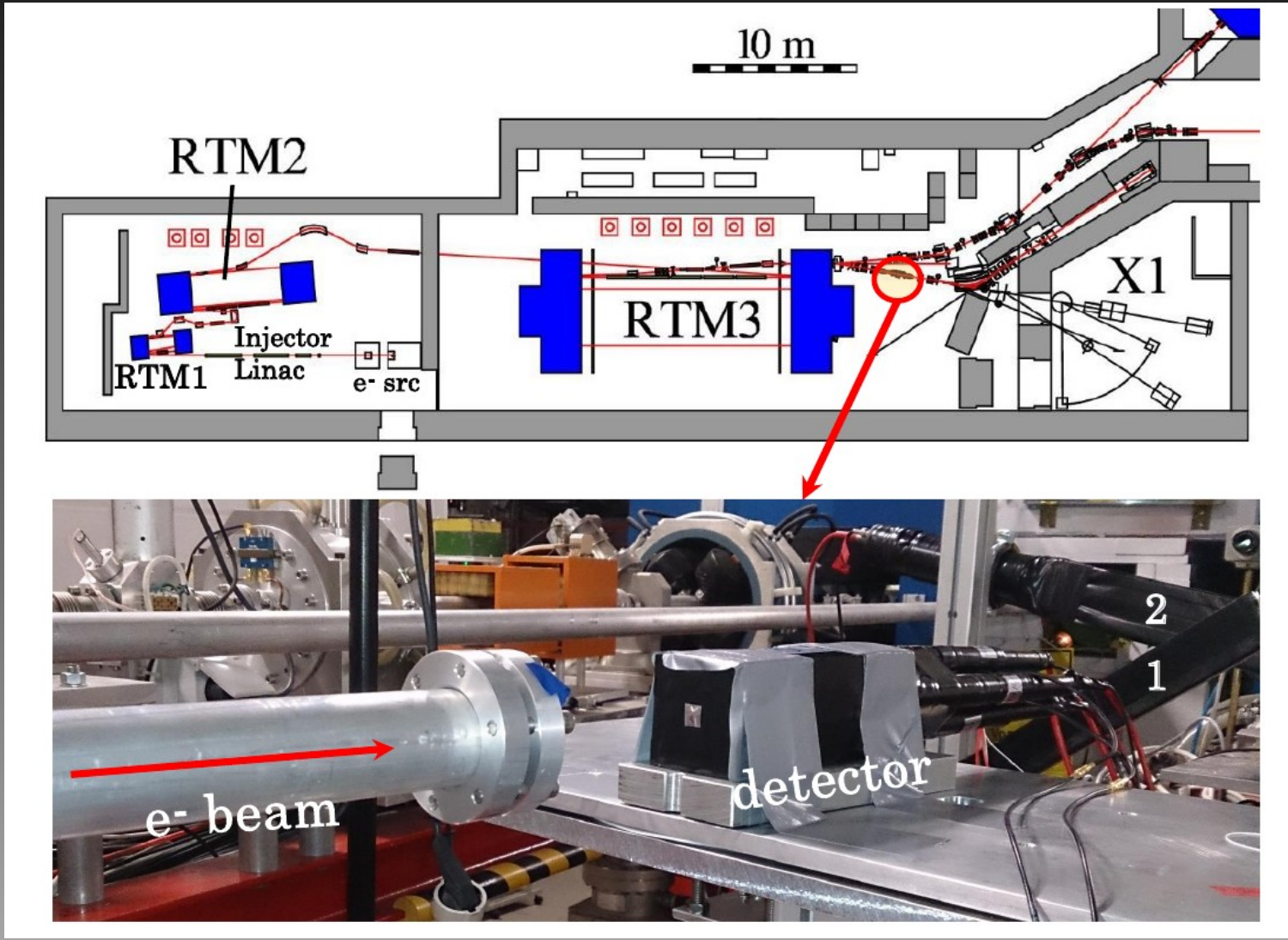
Sampling ADC (Uppsalla)

- Version 2011
- 16-ch, 14-bit
- 125 MSPS
- Virtex-5LX50

xFP board:

- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
  - 6.25 Gbit optical
- 1 Gb Ethernet

MAMI Test Location

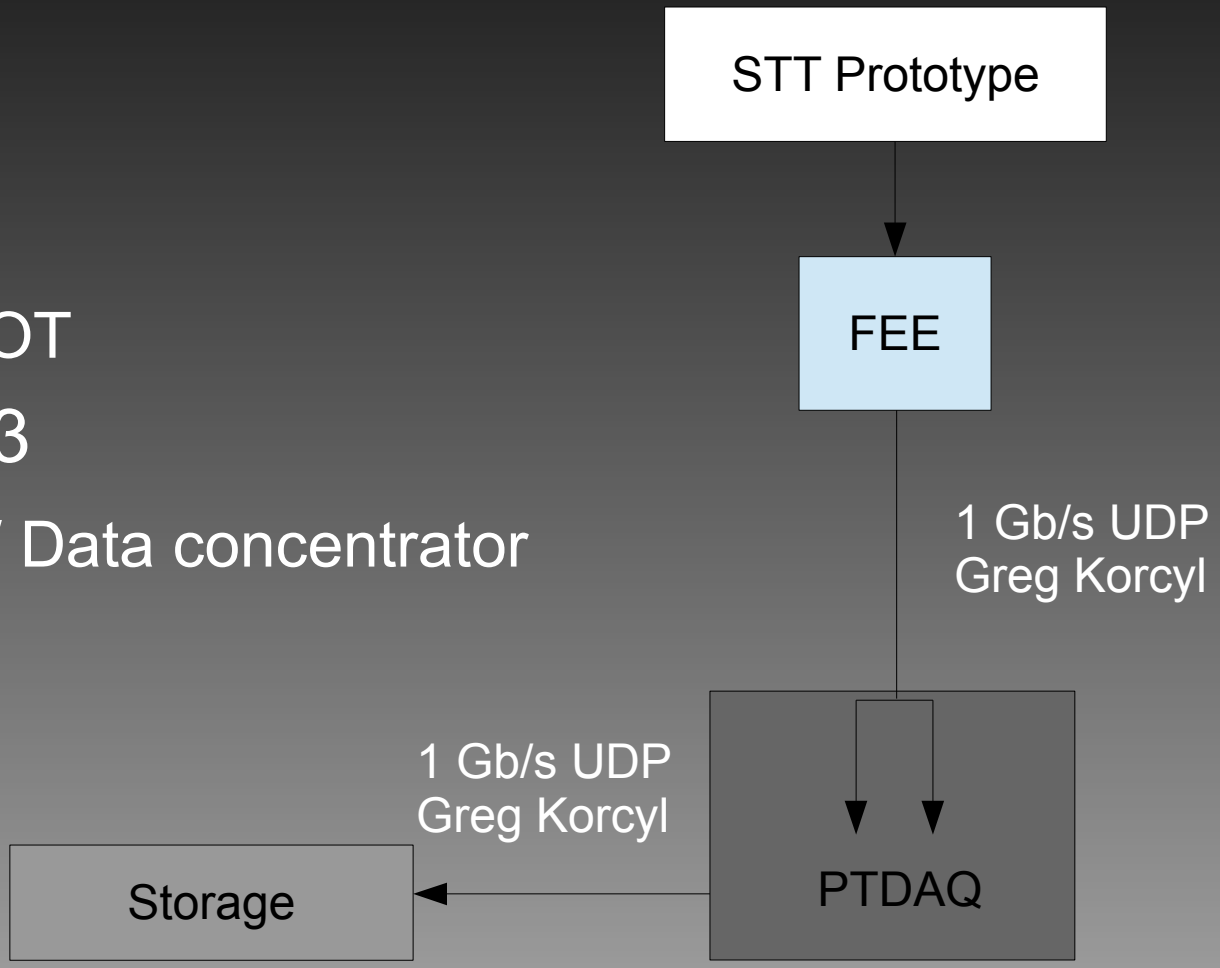


MAMI Test Results

- Stable Connection between DC and xFP
  - 2-Input burst building successful
  - For ~ 15 * 10^6 Stable events
    - Event size ~ 700 Byte
  - Data rate of ~1 Gbit/s

Jülich Connection Test

- DAQ chain:
  - 1 TRBv3
    - FEE board /TOT
  - 1 xFP version 3
    - Burst-builder / Data concentrator



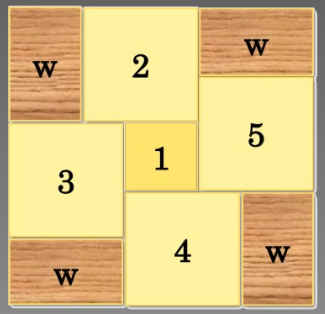
Groningen SODAnet Connection Test

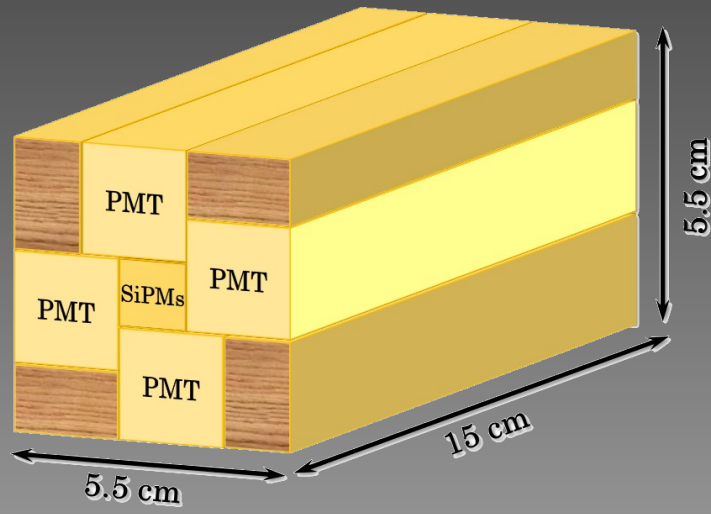
Sampling ADC (Uppsalla)

- Version 2012
- 32-ch, 14-bit
- 80 MSPS
- Virtex-6

MAMI Test Setup

- Beam parameter:
  - 210 MeV electrons
  - 0.003 - 2 MHz event rate
- Detector:
  - 1 mini PWO crystal
  - 2 HAMAMATSU SI-PM
  - 4 $\overline{P}$ANDA crystals





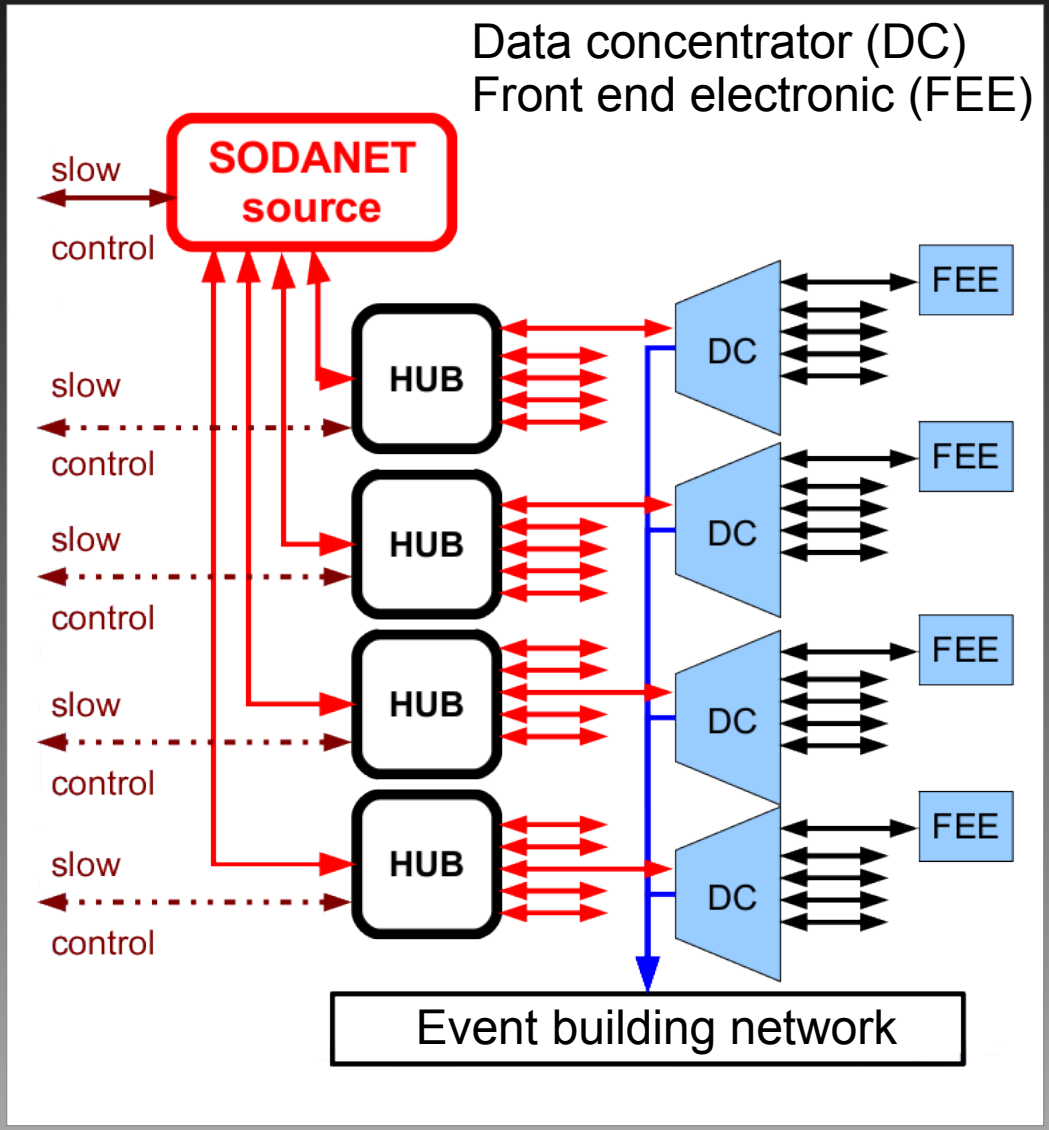
Synchronization of Data Acquisition

Functionality:

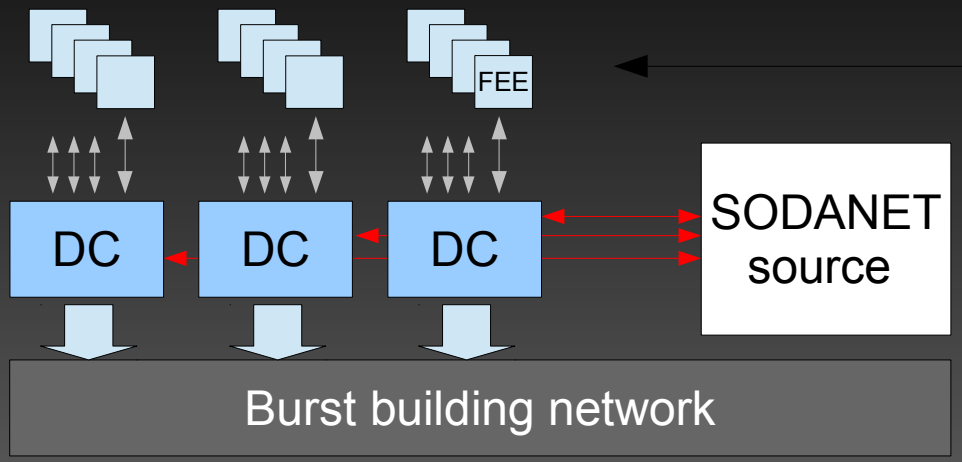
- Distribution of clock
  - Time stamp
- Distribution of synchronization commands
  - Start, stop, calibration
- Signal distributed over optical fiber
- Measurement of a signal propagation time
- Distribution of detector configuration data
- Slow control

SODANET link:

- Bidirectional
  - Source → data concentrator:
    - Synchronization
    - Front end electronic configuration
  - Data concentrator → source:
    - Slow control, used for time calibration



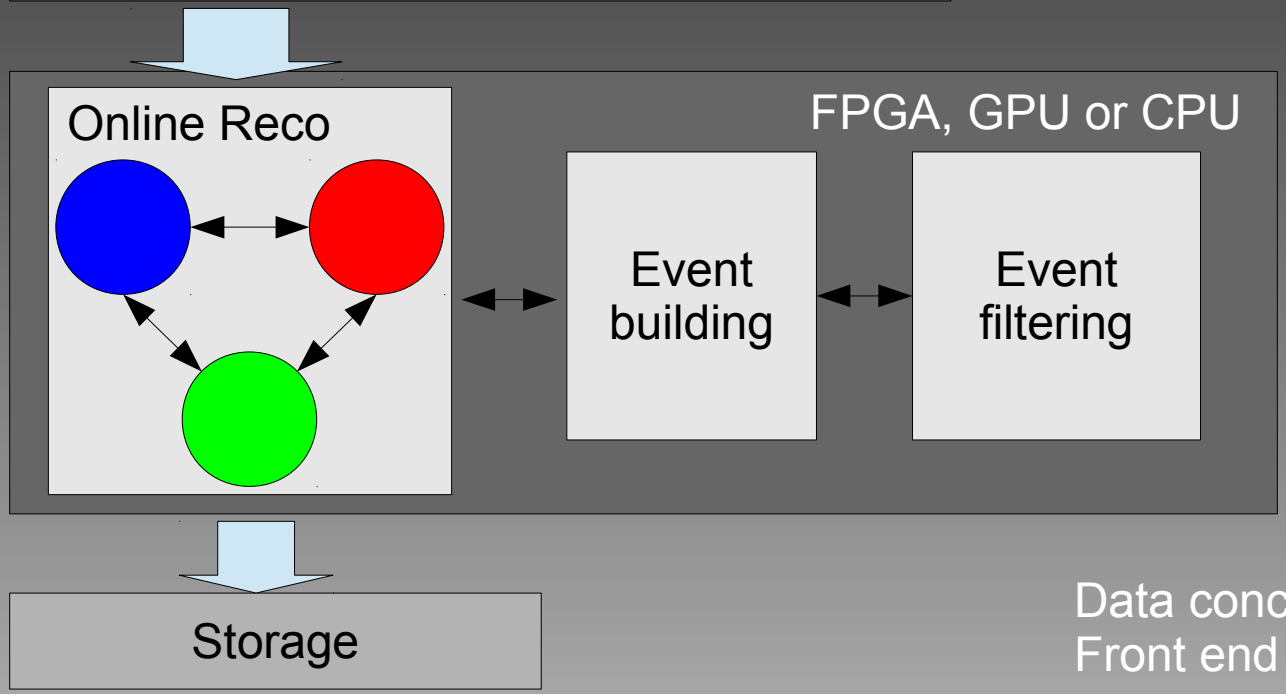
The PANDA DAQ



Autonomous FEE
Freely streaming data

Synchronization
Feature extraction

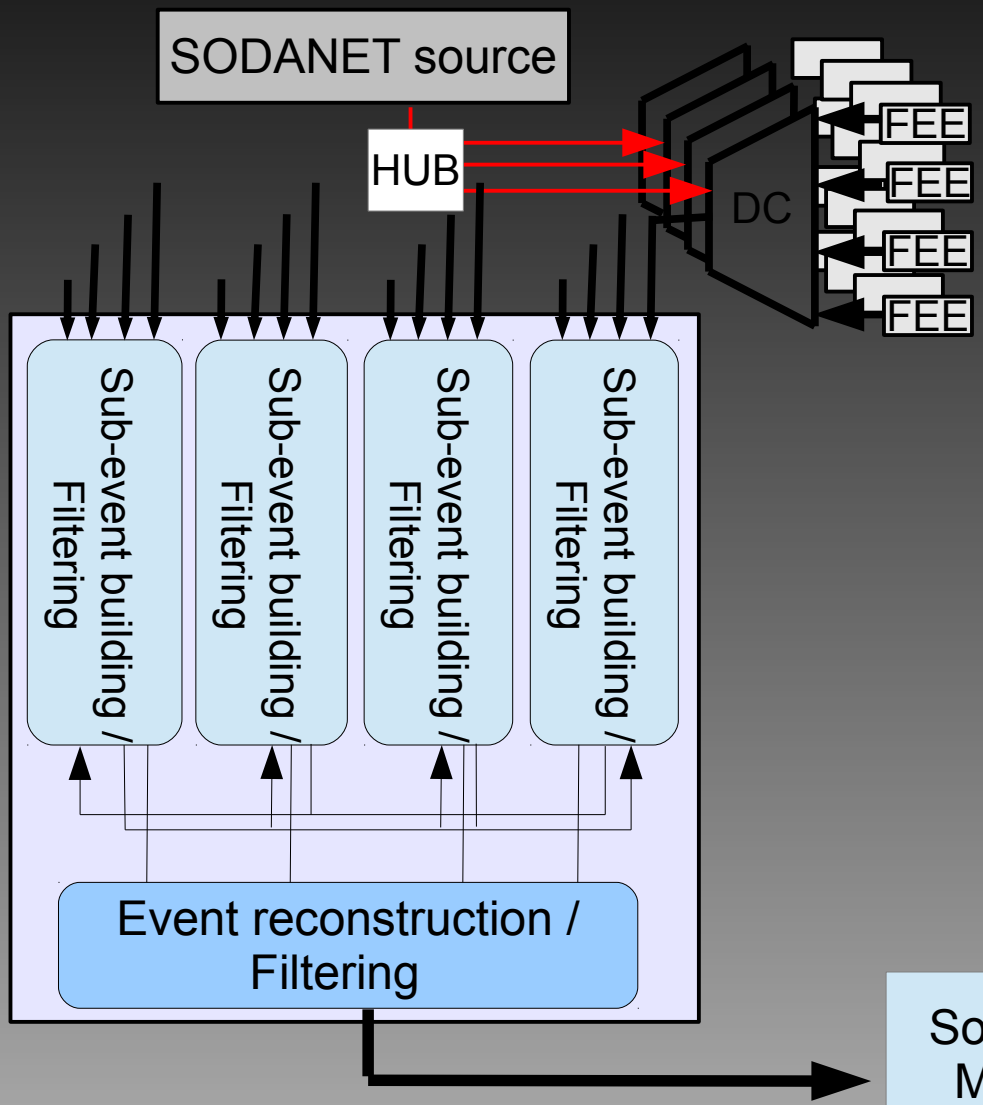
Burs building
Partly reconstruction



Full reconstruction
- Tracking
- PID
- Neutral reconstruction

Event building
Event filtering (based on physics)

Data concentrator (DC)
Front end electronic (FEE)



- VHDL code can be used without many changes
- Increased number of inputs per sub-detector
- Increase the possible data rate
- High performance event reconstruction
- High level event filtering
  - Software trigger on a sever farm or GPUs

The PANDA DAQ

- Freely streaming data :“Trigger - less”
- No hardware triggers
- Event filtering
- Autonomous FEE, sampling ADCs with local feature extraction
- Time-stamping (SODA)
- Data fragments can be correlated for event building
- Caveat: the high-rate capability implies overlapping events !!!
- average time between two events can be smaller than typical detector timescales
- This “pile-up” has to be treated and disentangled
- Real-time event selection in this environment is very challenging and requires a lot of studies