STT Status & News

Peter Wintz (FZ Jülich) for the STT group

PANDA CM 54, TRK session, Sep-9th, 2015

STT Outline

- STT news
- STT activities (WPs)
- Next in-beam test
- STT “pre-series“ test (M8)
- Electronic readout decision

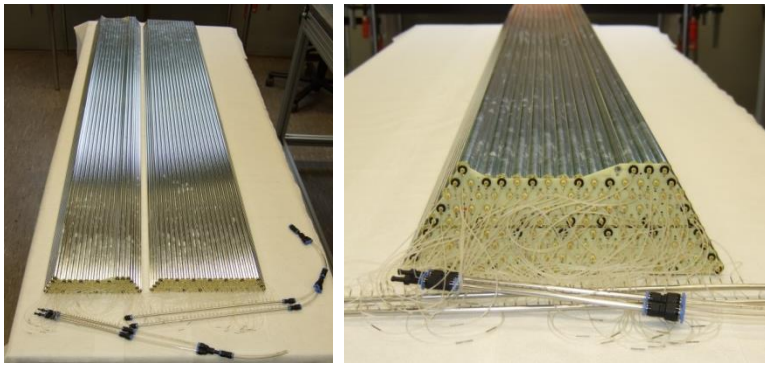
STT News & Agenda

- Some re-organization of STT WPs are needed due to current PANDA situation
- The STT “pre-series“ test in 2016 is still planned & prepared
- Pre-series tests can serve as data basis for readout decision

- Beam test time approved by CBAC, scheduled for Nov-2015
- **But date insecure** due to beam area cleanup by COSY
- New beam test area (COSY-TOF) setups
- STT + Forward Tracker test systems

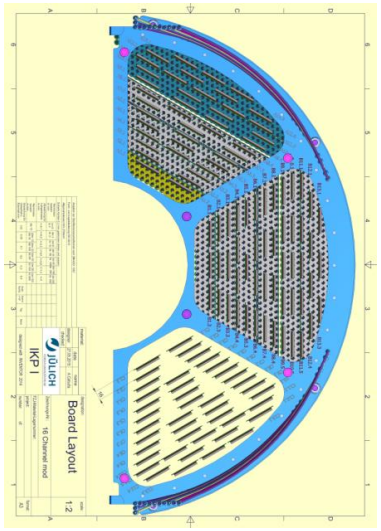
WP: Straws & Modules & Mech. Frame

- Straw mass production ongoing, current period started last week
- First straw quad-layer modules are assembled (figs below)
  - New precision profile plate, straw pitch 10.14mm, 10-20µm glue gap
- Mounting of modules in STT prototype frame next
- Frame adapters & supports for new geometries, mounting scheme defin. ..
- Design iteration of frontend layout ongoing, supplies & readout boards



The first two inner straw modules of the STT, glued with the new straw pitch.

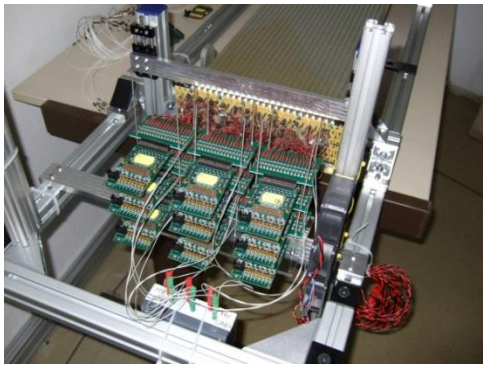
Dario, Daniele, Vincenzo, Artur & Peter with the prototype frame



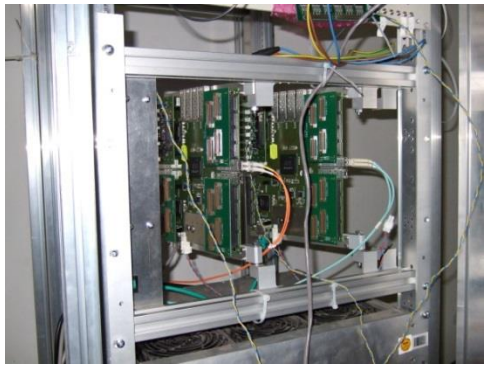
Placement of FE-boards (CAD by Artur)

WP: ASIC/TRB - Readout

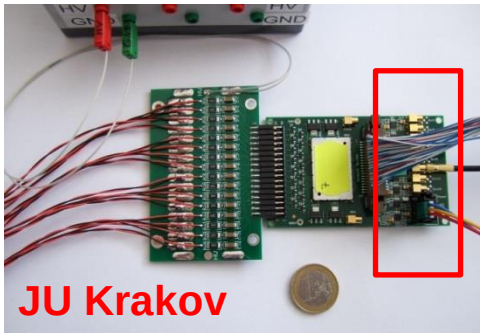
- ASIC/TRB readout (time-over-threshold for dE/dx)
- “PASTTRECv1“ - ASIC (8 ch)
- 2× ASICs per FE-board (total: 16ch), additional analog out (red box)
- 16×signal out (LVDS), 4×ASIC control lines via 20 pairs micro-ribbon cable
- ASIC setting by TRB-FPGA (gain, thresh. peak time, BL, TC)
- FPGA programming by JU Krakov
- TRB3 boards, multi-board crate design



Front-end boards at STT test system



TRB crate, 2x TRB3 boards mounted



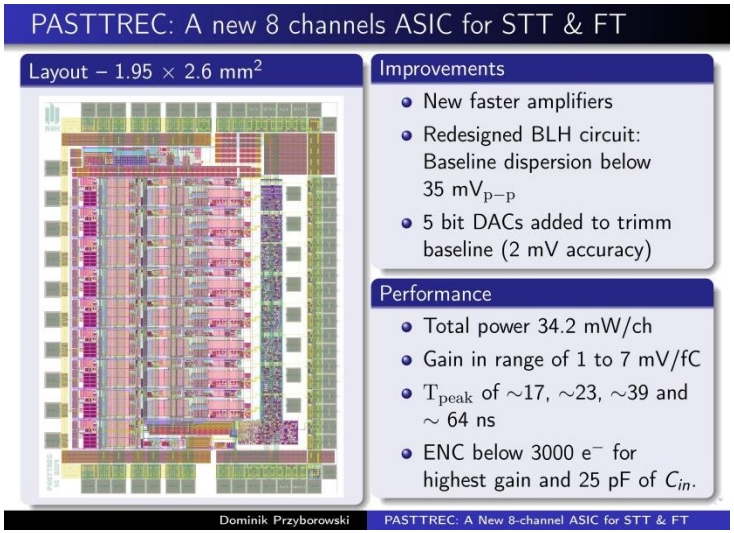
Straw coupling board and FE-board, additional analog out (red box)

WP: ASIC & FE-Boards

- 16× FE-boards bonded with ASICs (2× ASICs per board, 2× 8ch)
- ICs leftovers from last production (2014) ordered, shipped to AGH Krakov
- 16× FE-boards more available, ASIC bonding next
- In total: 32× FE-boards with ASIC - PASTTREC-v1
  - For STT and FT test systems
  - 512 channels alltogether

- Verification of ASIC parameters ongoing
  - Main goal of next beam time data
- Improvements for ASIC setting & control via FPGA-TRB were sucessfully done in Krakov (Pawel S., Greg)

ASIC design by AGH Krakov



PASTTRECv1 parameters

WP: PASTTRECv2 - ASIC & FE-Boards

- ASIC 8ch layout re-confirmed, allows 16/24 channel FE-boards in future
- No advantages seen for 16ch ASIC (space, power consumption)

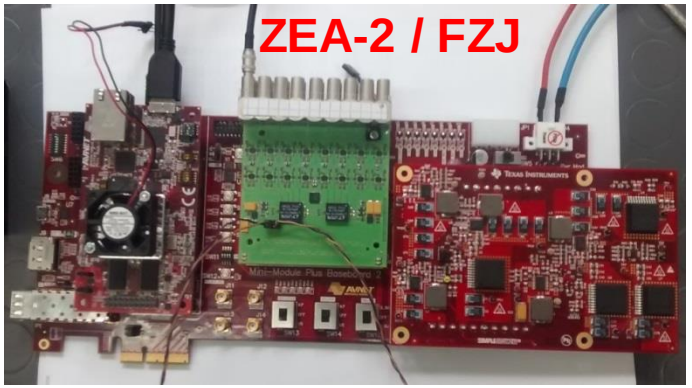
- Option for 2nd version ASIC in 2016 if necessary, “PASTTREC-v2“
  - Shaping parameters based on beam test results
  - Severe changes to be discussed, i.e. two-threshold feature, 2nd higher thresh for time-over-threshold (better resolution to be checked)
  - Design workout not possible in 2015 (AGH Krakov)

- New FE-board design in preparation (JU Krakov)
  - Same current ASIC footprint
  - Iterations done with AGH experts, new 6-layer board layout
  - Some voltage supply & space improvements
  - Only 2 analog output channels per ASIC, less power consumption
  - Reminder: no analog output for final version boards

WP: ADC - Readout

- ADC readout, front-end electronics free (FEE-free)
- Straw signal transmitted via micro coax cables, 0.5mm Ø, 12m length, HV stable
- Amplifier backend, HV distribution backend

- New ADC type tested: LTM9011-14
  - 14-Bit, 125Msps Low Power Octal ADC (8ch), 2 ADCs per board (green)
  - ADC readout via commercial FPGA board (AvNet with Kintex-FPGA)
- FADC board & readout by ZEA-2/FZJ
- To do: amp integration & HV in/to ADC board
- Verification of new ADC (sampling) ongoing
- Integration in PANDA-DAQ



→ talks by Ljuba and Andreas (ZEA-2)

Upcoming Beam Test

- One week scheduled, 15th - 23rd of Nov., COSY-TOF beam area
- Protons, 3× diff. momenta, 2.95, 0.8, 0.6 GeV/c
- New TOF - beam test area
  - ~2m beam line height, dedicated platforms & lifts for detectors in prep.
  - Detector & readout re-installation necessary, cabling, new counting room
  - Detector and DAQ tests with cosmics prior to beam time
- Main beam test program: ASIC-TRB and ADC tests
- STT test systems + ForwardTracker modules
- Additional tracking chambers and scintillators

- Beam areas currently being cleaned up by COSY (Big Karl, COSY-TOF)
- Severe administration & radiation safety control procedures

Beam time scheduled for Nov. but date insecure

STT Pre-Series Test (M8)

- Pre-series test (M8) of STT is still planned and prepared under the current funding situation for ≥ Q2/2016
  - Straw modules, prototype mech. frame system
  - Pre-series / prototype readout systems
- ToDo: definition of test system(s), measurements & criteria (STT group & TC)
- Proposal: split STT test systems & tasks (on next slide)

- Simple gas supply system sufficient (premixed gas, flushing mode)
- PANDA-DAQ not expected available: no high-rate readout, no real-time tracking

STT Pre-Series Test

Proposed test systems & tasks:

- Full system test: one STT sector (~700 straws)
  - Mount straw modules in existing prototype frame (adapt. to new geo.)
  - Front-end electronics & readout system & cable routing
  - Cosmic tests (3D-tracking)
  - Only moderate beam intensity (no uncontrolled aging)
  - Straw modules can be used later in final system
- High-rate readout in-beam tests: ~ 1-2 MHz / cm wire
  - 2 setups for ADC and ASIC/TRB readout, each min. ~192 straws
  - Similar straw modules as in STT
  - Quad-layer modules (16-24 straws per layer)
  - Mechanical precision tests of modules with beam
  - Straws can be not used later, due to rates up to ~100x PANDA-STT

Towards Electronic Readout Decision

- Decision between both readout options for PANDA-STT required
- Decision process definition and approval by the STT group and TC
- General criteria: performance results, system complexity, robustness, economics

- “Pre-series“ in-beam readout tests can serve as data basis
- Proton & deuteron beams in momentum range 0.6 – 3.0 GeV/c
- Similar to proton / kaon / pion separation <1 GeV/c at PANDA
- Measurement program (1st ideas):
  - Particle track reconstruction and spatial resolution and efficiency
  - dE/dx as function of momentum & particle ID
  - High particle rates up to 1 MHz/straw
  - Continuous readout mode (no external trigger)
  - Beam incident at several wire positions along z, inclined beam
  - ..

Towards Readout Decision Process

- Definition of information & requirements to be fullfilled
  - Full chain of electronics design (CAD best, prototype systems)
  - All components specified (analog, digital, cables, .. manufactures)
  - Latest cost estimates
  - No further R&D requirements
- Calibration and analysis steps & procedures defined
- Performance criteria
  - Spatial and time resolution (unbiased, 16-24 straw layers)
  - Efficiency (unbiased)
  - Real-time capability (FPGA, data rates)
  - Robustness (noise, hit bursts, ..)
  - High rate readout and full signal dynamical range

Decision process & criteria to be further defined and iterated inside the group and with TC

Thank you
for
your attention
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