JÜLICH
FORSCHUNGSZENTRUM

Hardware characterization of ADC based DAQ-System for PANDA STT

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General DAQ concept

- Conception of an ADC based DAQ
- Development of 16-channel prototype
- Test of the prototype (test beam in May 2015)
- Processing of the acquired data in order to get the spatial resolution

Conception of an ADC based DAQ

- Maximize channel density/Process massive amount of data
- Get the required accuracy
- Nice to keep the system flexibility in term of bit resolution and sampling rate

Maximize channel density/ ADC choice

1. Sampling rate: Reduce a sampling rate in order to reduce power consumption and required processing power, thus reducing ADC and FPGA chip counts.

We have verified the system with the sampling rates 240, 166, 133, 120, and 80 MHz .

2. High integration: using of multichannel ADCs reduces overall board space requirements.

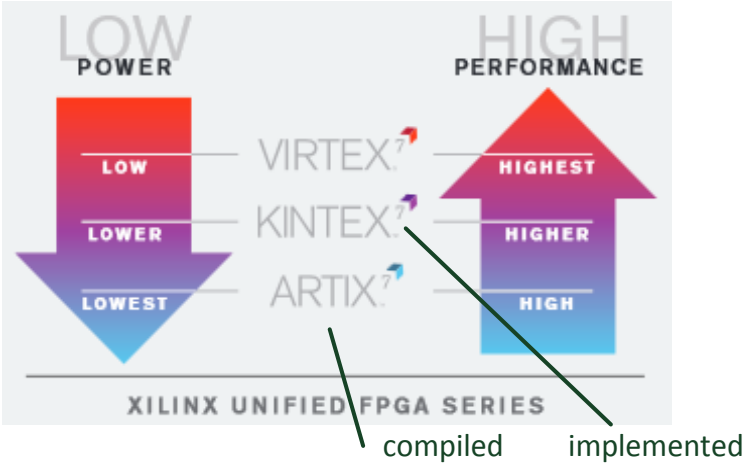
The 8-channel LTM9011-14 ADC is used.

3. Power consumption: Low power consumption per channel reduces heat in high channel count applications.

3.1 Choice of ADC type

The pipelined ADCs offer the best trade off between power consumption and sampling rate

3.2 Choice of FPGA



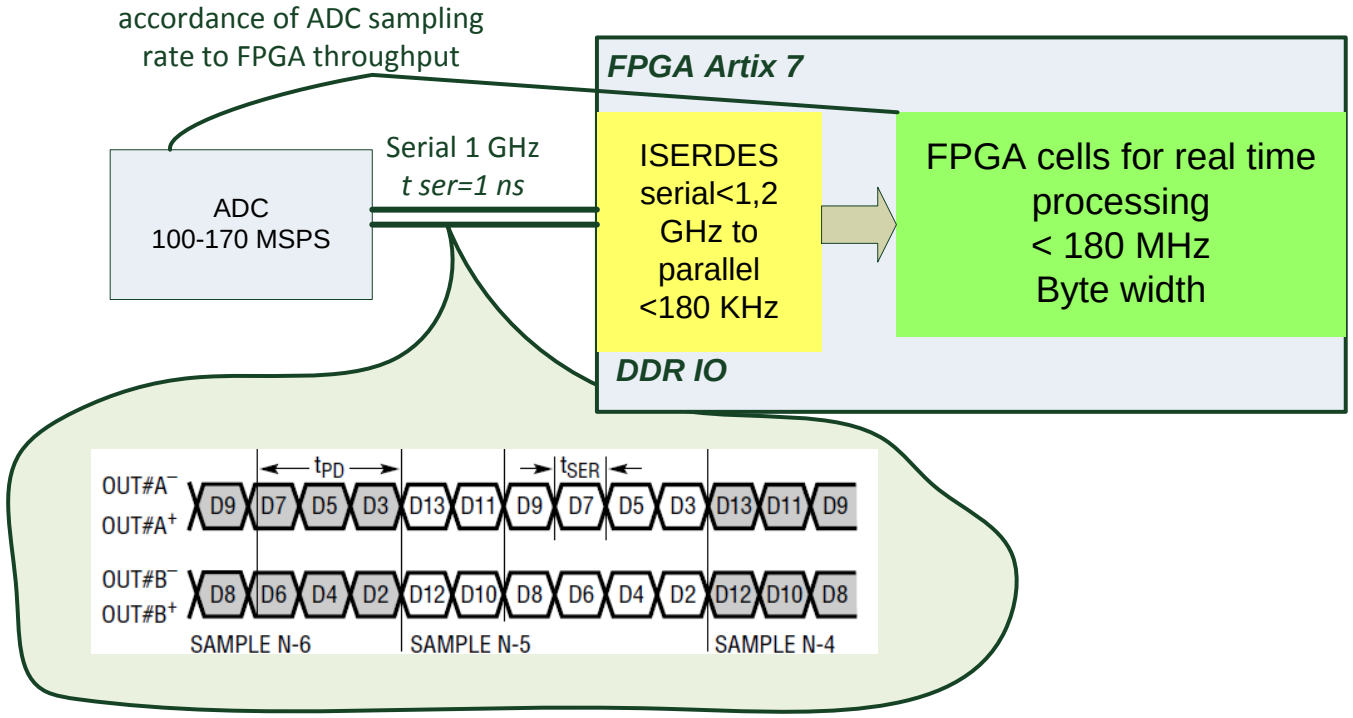
4. ADC to FPGA bandwidth matching

ADC to FPGA bandwidth matching

1. matching of ADC output to FPGA input

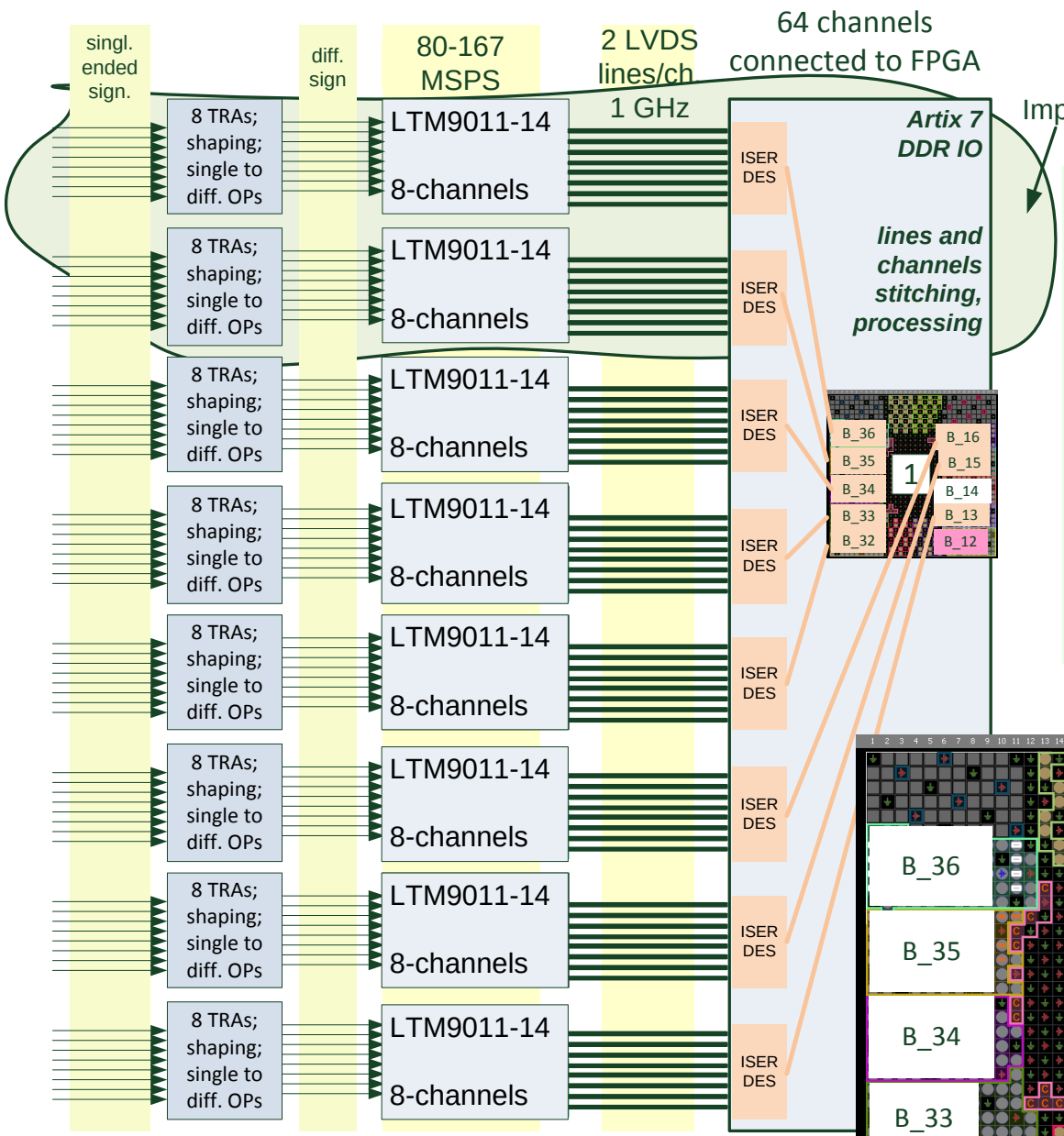
The key feature is: ADCs PLL should perform up to 1GHz,

providing 1 GHz serial data stream. This is the highest data stream, that FPGA is still capable to capture.



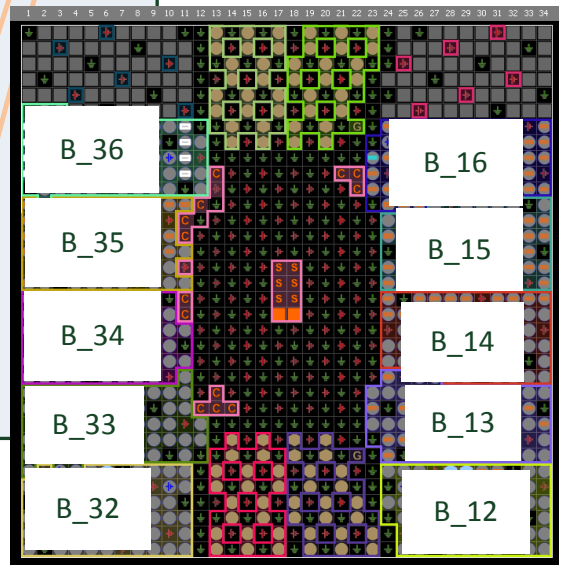
- 125 MSPS/ 14 bit to 1000 Mb/s data stream (2 lines x 8 bit)
- 133 MSPS/ 12 bit resulting to 800 Mb/s data stream (2 lines x 6 bit)
- 167 MSPS/ 12 bit resulting to 1000 Mb/s data stream (2 lines x 6 bit)

Linear Technology LTM9011-14, is specified for a sample rate of 125 MSPS in 14- bit mode.



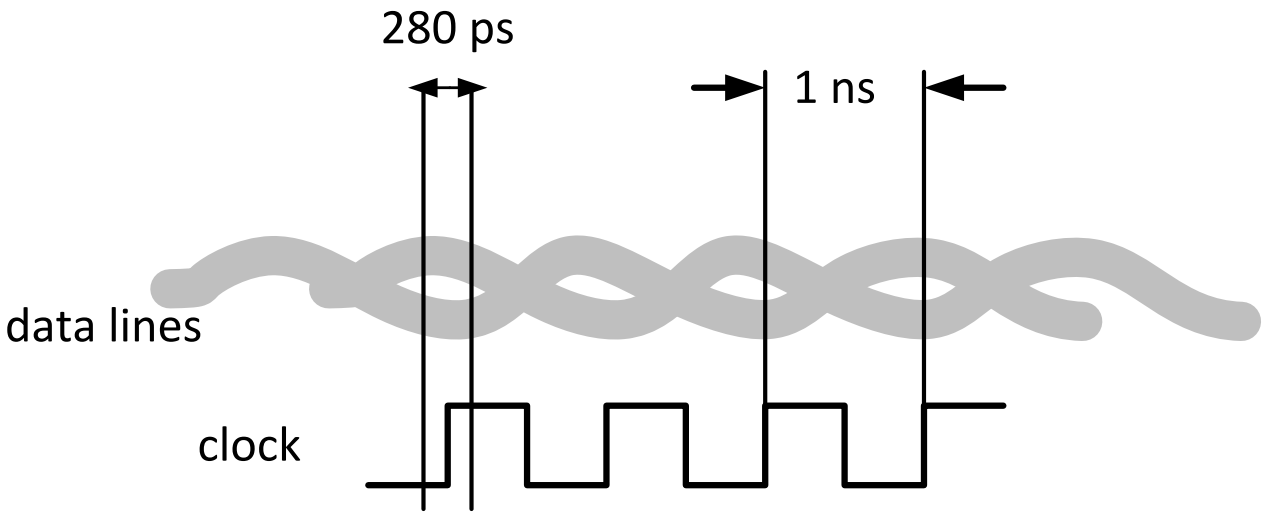
Second aspect – using almost all FPGA I/O banks to acquire the data

- 8 from 10 I/O banks to acquire the data
- Each bank has 20 differential I/O pairs. This is enough for connecting of one 8-channel ADC to single FPGA bank.



Open eye test

Each LVDS signal enters FPGA chip passing individual adjustable I/O delay unit (IDELAYE2).
This unit delays LVDS data until the clock front pass in the opening eye.
It is performed with variable number of delay tabs (>=32). Each tab introduces delay of 70 ps.

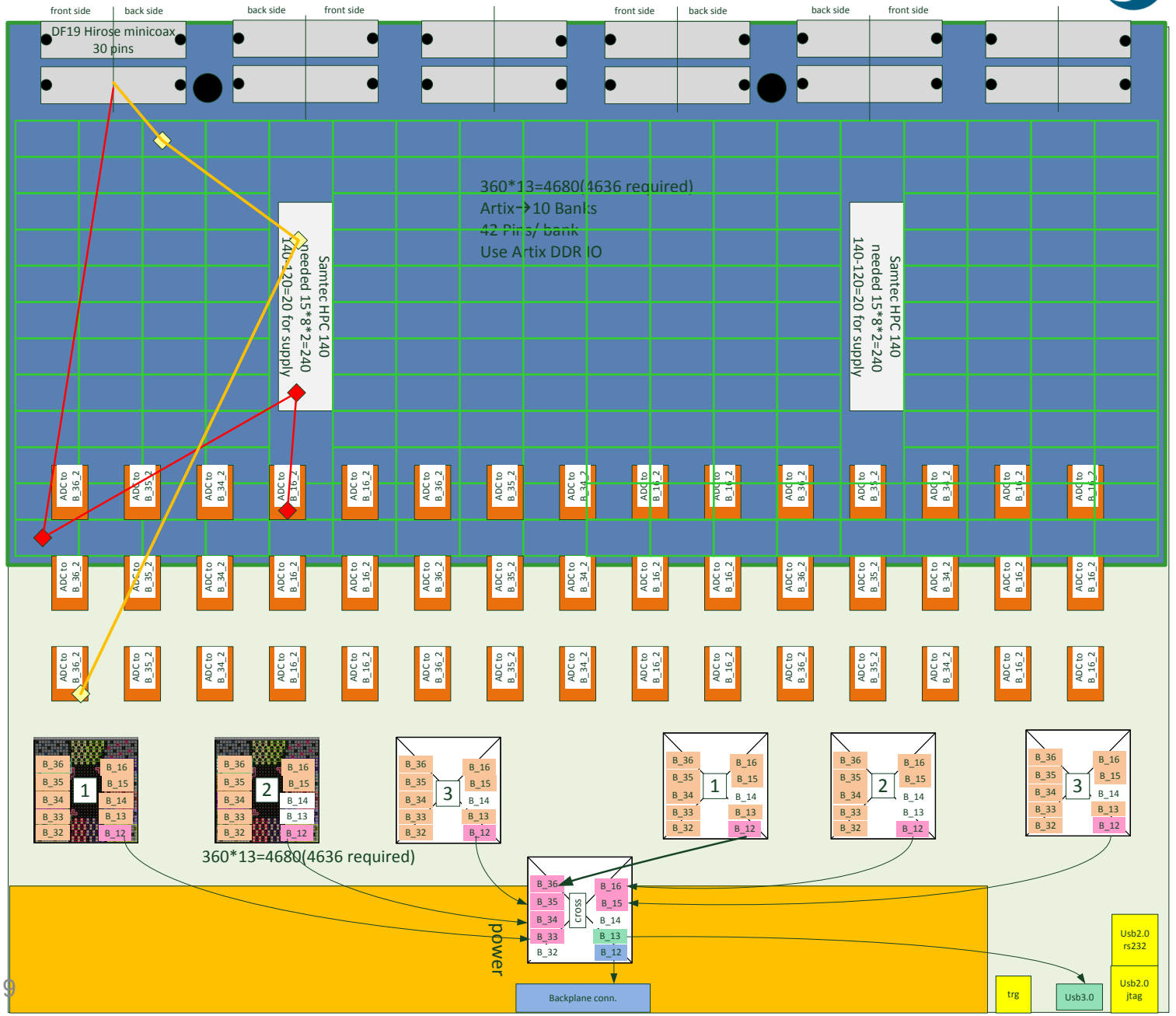


Been tested in our experimental setup:

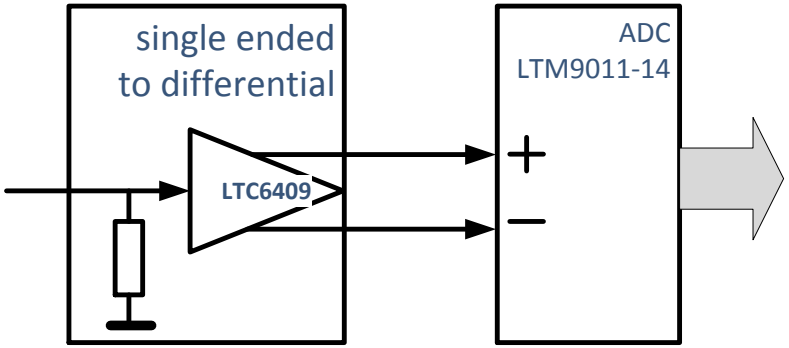
The opening eye value decreases from 8 to 4 delay taps (560 to 280 ns) with increasing LVDS line length from 14 to 28 cm.

Desired length of 1 GHz-LVDS-line connecting ADC and FPGA should be not more as 30 cm.

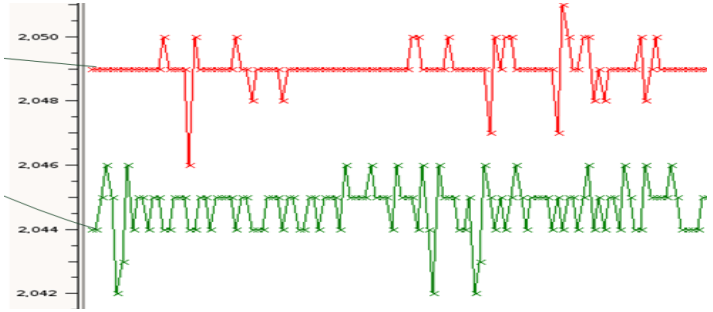
Electronic elements inside ATCA board



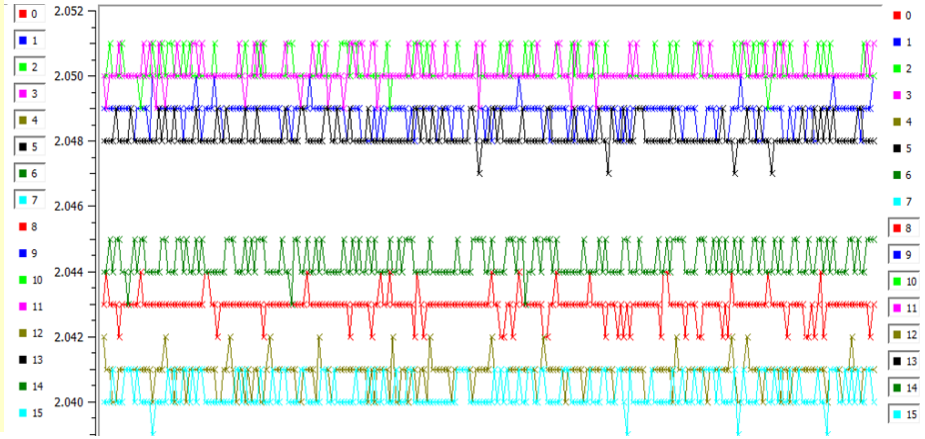
Noise/ offset measurements



12- bit mode, 166,7 MSPS



12- bit mode, 125 MSPS



The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \cdot N + 1.76_{dB}$$

The best ratio that can be achieved for 12-bit ADC: 74db

AC performance LTMR9011-14 includes 73.1dB SNR

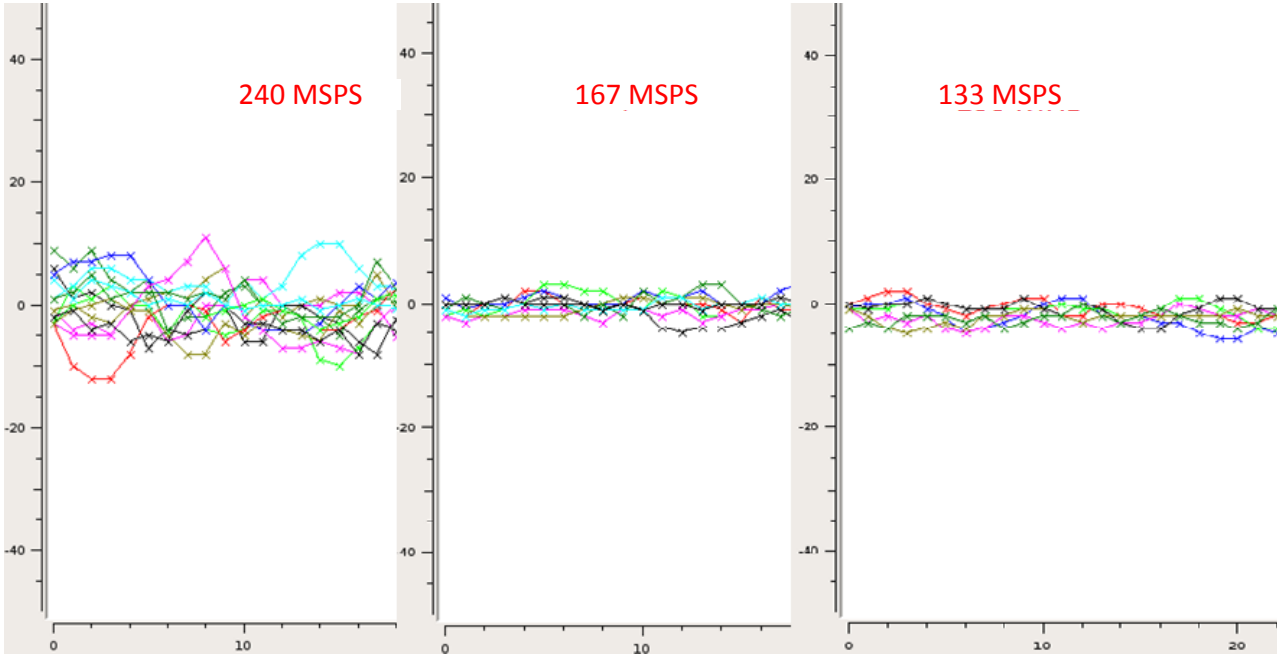
Offset channel-to-channel deviation:	10 bit
Noise 125 MSPS:	1-2 bins
Noise 166,7 MSPS:	3-4 bins

Signal-to-Noise measurements during test beam 05.2015

The whole chain Straw tube +10 m-cable +TRA/shaping amplifier +ADC

The same measurement (energy, HW), same TRA/shaping amplifier

The only difference is ADC: 240 MSPS-old LTC2242-12; 166 and 133 MSPS LTM9011-14



Noise 240 MSPS: ~20 bins compared with an average cluster (est. 30 bins)

Noise 166 and 133 MSPS: ~10-12 bins

power estimation

per channel

- FPGA, each consuming ~8 W/ 64 ch. → 80mW
- A/D channel, ~180mW
- Analog electronic ~100mW
- At all/channel →360mW

per board

360 x 0.360~ 130 W (spec. for ATCA board in crate <200 W)

Interleaving ADCs for Higher Sample Rates

combine more than one analog-to-digital converter (ADC) in an effort to increase the effective sample rate

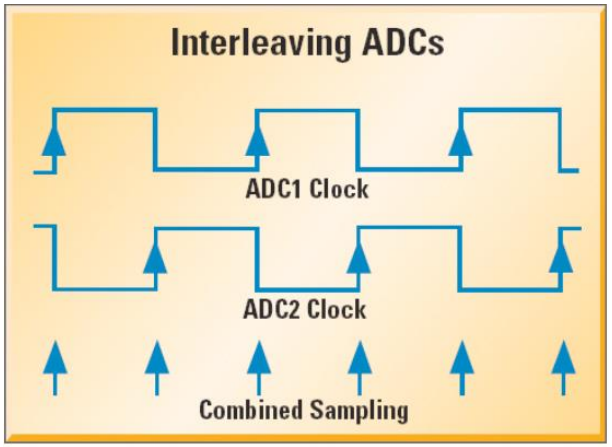
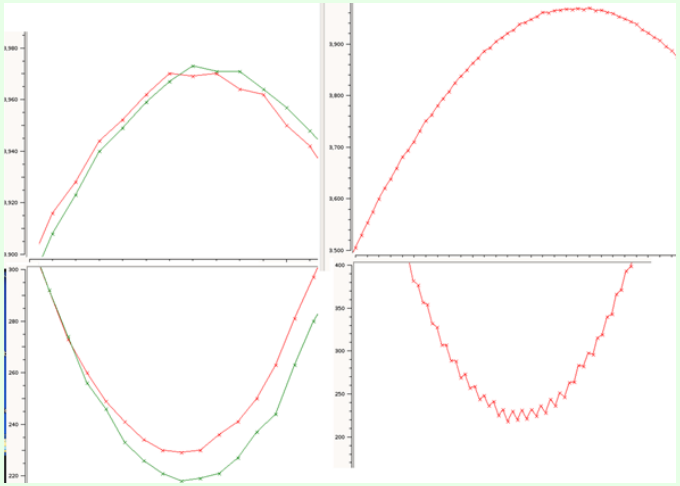


Figure 1. Interleaving two ADCs is the process of using a second ADC to fill data half way between the samples of the first ADC



Matching of 2 channels to single one is not ideal, the differ offsets and gains of 2 LTM9011-14 ADCs destroys the sinus.

HMCAD1520 offers self-calibration feature where offset, gain,
and linearity errors are minimized,
making it much easier to interleave them without spurs.

Table 17: Maximum Sampling Rate vs Number of Output Bits for Different HMCAD1520 Configurations

Number of bits	Single Channel High Speed [MSPS]	Dual Channel High Speed [MSPS]	Quad Channel High Speed [MSPS]	Quad Channel Precision [MSPS]
8	1000	500	250	-
12	660	330	165	82.5
14	560	280	140	70
16	500	250	125	62.5
Dual 8	-	-	-	125

Comparison: was, is and can be

	LTC2242-12 (was)	LTM9011-14 (is proved)	HMCAD1520 (to be or not to be)
Power dissipation /ch., 166 MSPS	740 mW (spec. only for 250 MSPS)	180 mW	123 mW
SNR (dB)	65.4	73.1	70
ADC-to-FPGA matching	Poor, causing by single channel output running at 250 MHz	Very good, 2-LVDS serial lines per channel each running up to 1 GHz	Very good, 2-LVDS serial lines per channel each running up to 1 GHz
Sampling rate in 12-bit mode	10-250 MSPS	80-125-166(not spec.) MSPS	80-166 MSPS, up to 1 GSPS by interleaving and in 8-bit mode
Flexibility to diff. experiment requirements	Poor, single mode 12-bit	Good, 12 /14-bit, increasing sample rate by low bit mode	Very good, 8/12/14, increasing sample rate by low bit mode
proved	yes	yes	No, but it offers the same control and data transfer as LTM9011-14
Channels/chip	1	8	4

outlook

- ***16-channel prototype was successfully tested***
- ***We should only scale up the verified design in order to build the whole 4636- channel DAQ system***

THANK YOU!