

News & Activities

Peter Wintz (FZ Jülich) for the STT group

LIII. PANDA CM Uppsala, TRK session, June-9th, 2015

Outline

- News
- STT activities (WPs)
- Beamtest report (STT/FT)
- FT report (Jurek's slides)

News - Personnel

- **Dominik Przyborowski** (AGH Krakov) finished his Ph.D., was key-person for ASIC design (PASTTREC)
- **Tomek Fiutowski** (AGH Krakov) contact person for ASIC development
- **Harout Ohannessian** (IKP, FZ Juelich) finished his master thesis
- **Alexandros Apostolou** (KVI Groningen, Ph.D.) research visit in Juelich, took over data analysis
- **Pawel Strzempek** (Jagiell. Univ Krakov) presented STT/FT at ELBA - conference

Group Activities

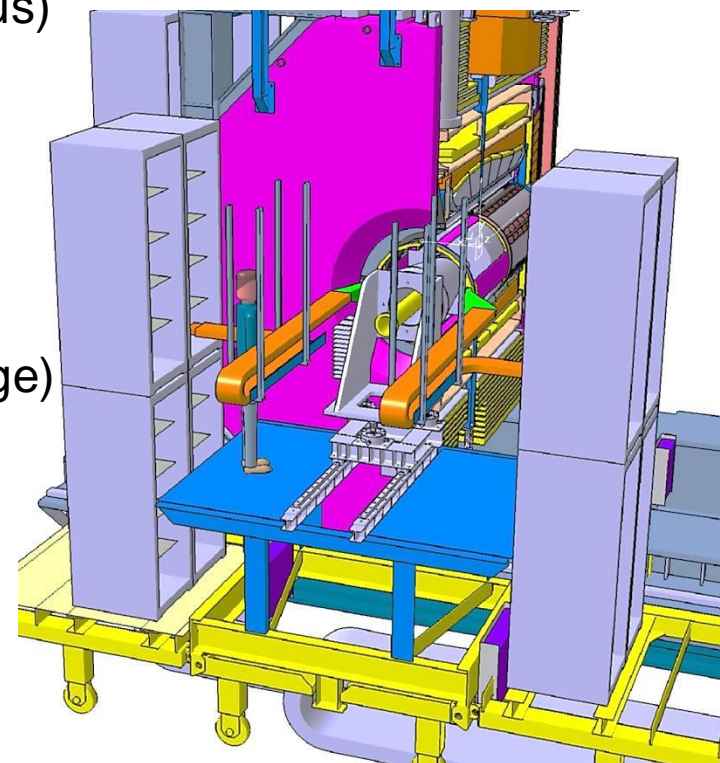
- **March-25/26th**: Frascati-Juelich WShop, CF&STT prototype frame assembly
- **April-9/10th**: PANDA DAQT-FEE Wshop at GSI
- **April-27/28th**: PANDA Mech. WShop at GSI
- **May 4th-10th**: COSY testbeam time for STT / FT, FADC & ASIC/TRB readout

- **Summer**: Installation of STT test systems in new beam area (COSY-TOF)
- **Nov-2015**: 1 week beam time requested, CBAC meeting on June29/30th
- **2016**: Further beam tests planned
- **Q2 / 2016**: “Pre-series“ test

Group Activities: Mec. WShop at GSI

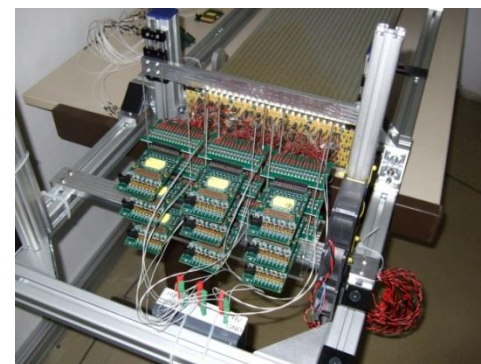
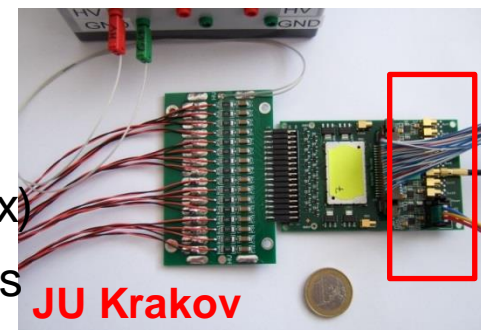
- Topic: Integration & installation of detector systems in Target Spectrometer
- Installation procedure for STT & CF-System presented by Dario
- STT services (cables & gas pipes)
- Rack positions downstairs (to be verified by us)
- Patch panel requirements

- STT system concept: system is split into two separated semi-barrels (L/R)
- Closed cable chains for L/R – barrel (in orange)
- To be further worked-out (position, cable bending radius, ..)



STT Status: Electronic Readout System

- ASIC/TRB readout (time-over-threshold)
- New PASTTRECv1- ASIC & FE-boards
- 2 ASICs (8ch) per board, additional analog out (red box)
- LVDS micro-ribbon: 16×signal out, 4×ASIC control lines
- ASIC setting by TRB-FPGA (gain, thresh. peak time, BL, TC,)
- First tests in beam last May, to be continued
- New TRB3 boards, multi-board crate design



ASIC design by
AGH Krakov

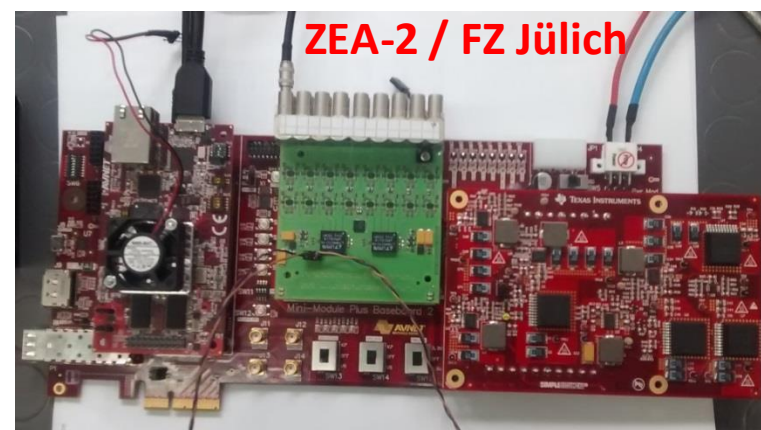
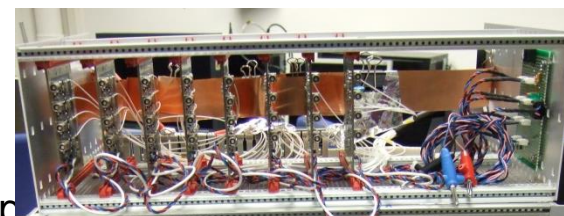
PASTTREC: A new 8 channels ASIC for STT & FT

<p>Layout – 1.95 × 2.6 mm²</p>	<p>Improvements</p> <ul style="list-style-type: none"> • New faster amplifiers • Redesigned BLH circuit: Baseline dispersion below 35 mV_{p-p} • 5 bit DACs added to trimm baseline (2 mV accuracy) <p>Performance</p> <ul style="list-style-type: none"> • Total power 34.2 mW/ch • Gain in range of 1 to 7 mV/fC • T_{peak} of ~17, ~23, ~39 and ~64 ns • ENC below 3000 e⁻ for highest gain and 25 pF of C_{in}.
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Dominik Przyborowski PASTTREC: A New 8-channel ASIC for STT & FT

STT Status: Electronic Readout System

- FADC readout, front-end electronics free (FEE-free)
- Straw signal transmitted via mini coax cables (1mm Ø, 10-12m), HV stable
- Amplifier backend, HV distribution backend
- 240MHz FADCs, 128ch (WASA@COSY)
- New FADC: LTM9011-14
 - 14-Bit, 125Msps Low Power Octal ADC (8ch), 2 ADCs per board (green)
 - ADC readout via commercial FPGA board (AvNet with Kintex-FPGA)
 - 1st test board (16ch) in May beam time, 2 more boards upcoming
- Lower sampling of straw signals
to be verified (beam tests)
- To be Done: integration of amplifier &
HV distribution in/to FADC board

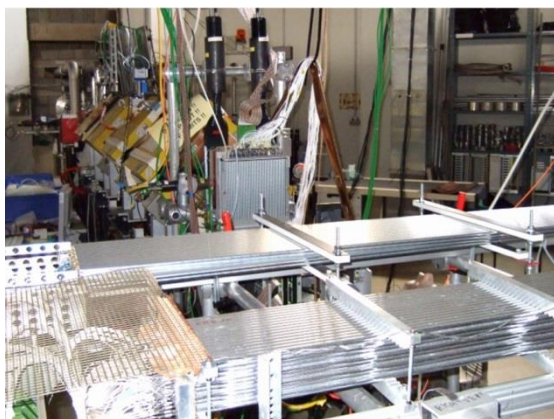


Beam Test Report

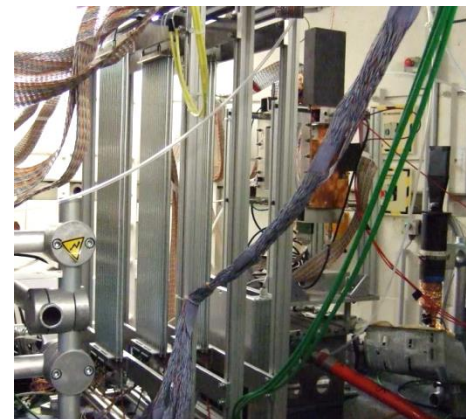
- One week beam time in May 4th – 10th, proton beam: 3.0, 0.8, 0.6 GeV/c
- STT test systems
 - FADC readout, 128ch (240MHz FADC), new FADC test board (16ch, 125MHz)
 - completion of dE/dx series measurement
 - test of new FADC (lower sampling), comparison of resolutions
 - ASIC/TRB readout, 144ch
 - new PASTTREC(v1) – ASIC (8ch), new ASIC front-end boards
 - new TRB3 boards & firmware, new data format
 - new ASIC control via TRB-FPGA
- Forward Tracker prototype modules (FT1-2)
 - 3x 32 straws, 68cm straw length, double layers (2x16 straws)
 - ASIC/TRB readout
 - Summary report (Jerzy's slides)
- Additional scintillators for triggering, straw chambers, GEM for beam monitor

Beam Test Report

- STT - FADC test system: readout unchanged, very reliable (Krzysztof's talk)
- STT - ASIC/TRB test system: completely new readout system
 - TRB/FPGA problems at high counting rates, STT: ~ 75 straws \times 300kHz
 - Crashes at readout rates > 10 kHz \rightarrow operated with trigger limit set
 - ASIC setting via TRB-FPGA unreliable \rightarrow higher NL (oscill.), wrong settings
 - FPGA code now updated by GSI, tests ongoing in Krakov
 - Beam data inspection ongoing, preparations for next beam time (Nov-2015)
- FT - ASIC/TRB: much less affected, fewer straws in direct beam



**The two STT test setups
(beam from back).**



**Three FT prototype modules with
3x 32 straws (beam from left).**

FT Beam Test Summary

Jurek's Forward Tracker Beam Report Slides

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