university of groningen

kvi - center for advanced radiation technology

Overview of the EMC Readout

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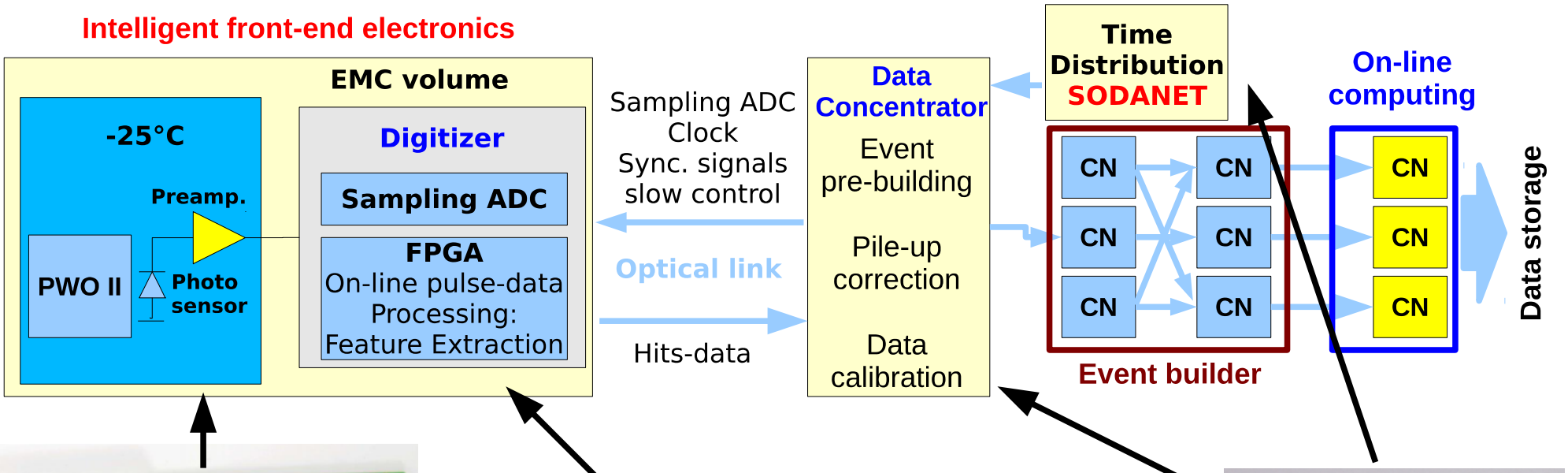
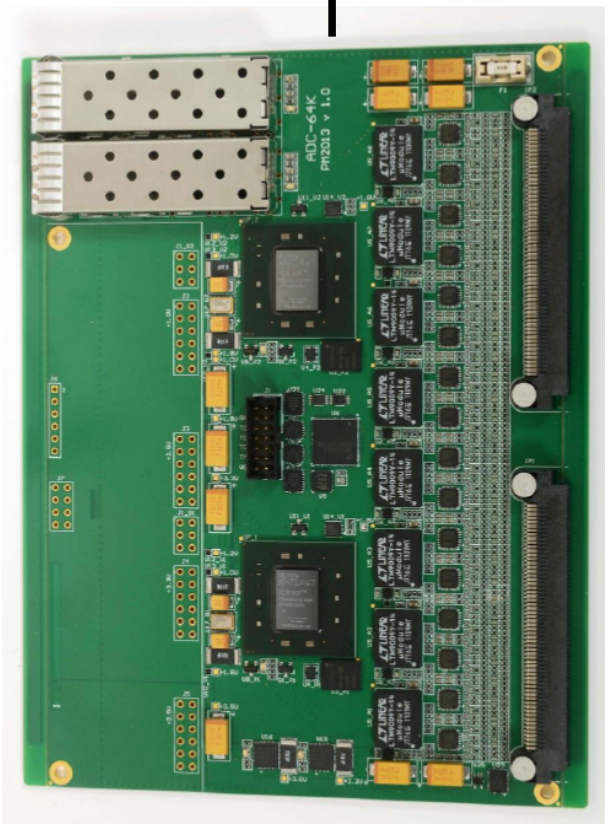
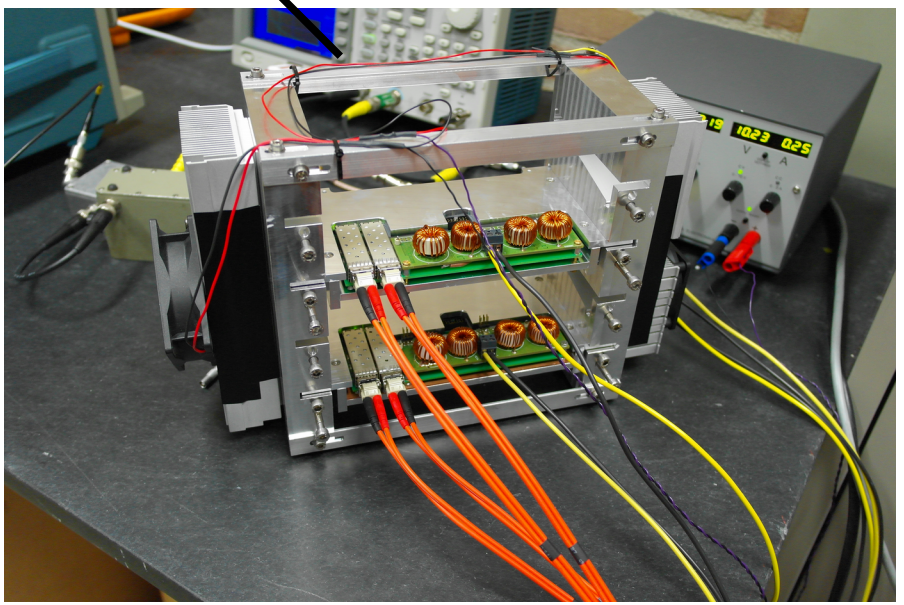
for the PANDA collaboration

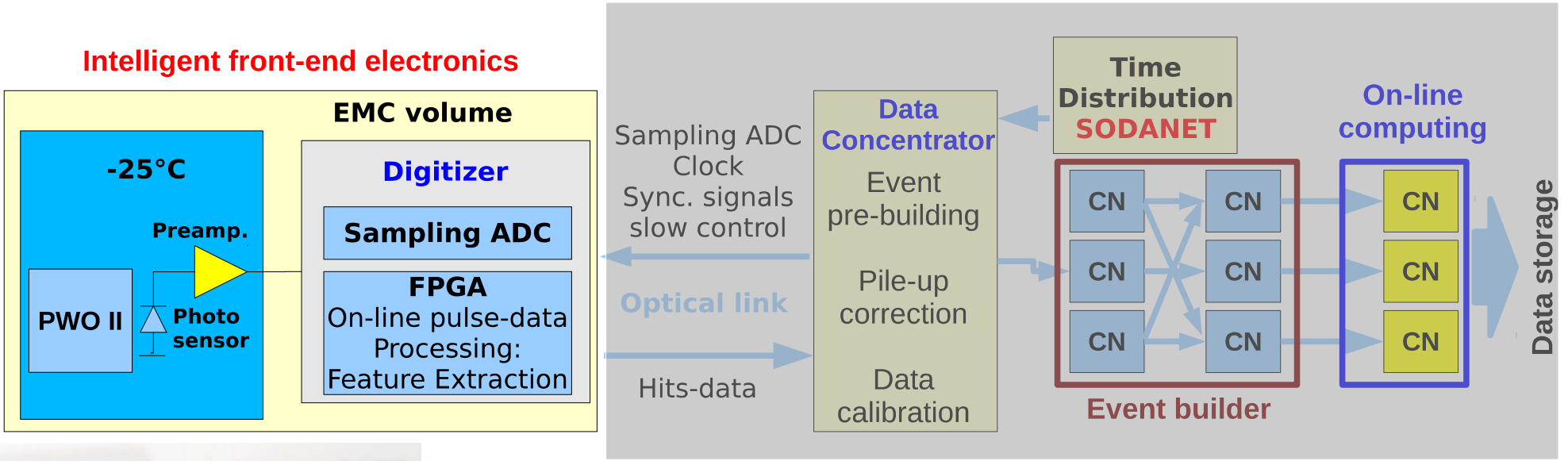
EMC Readout

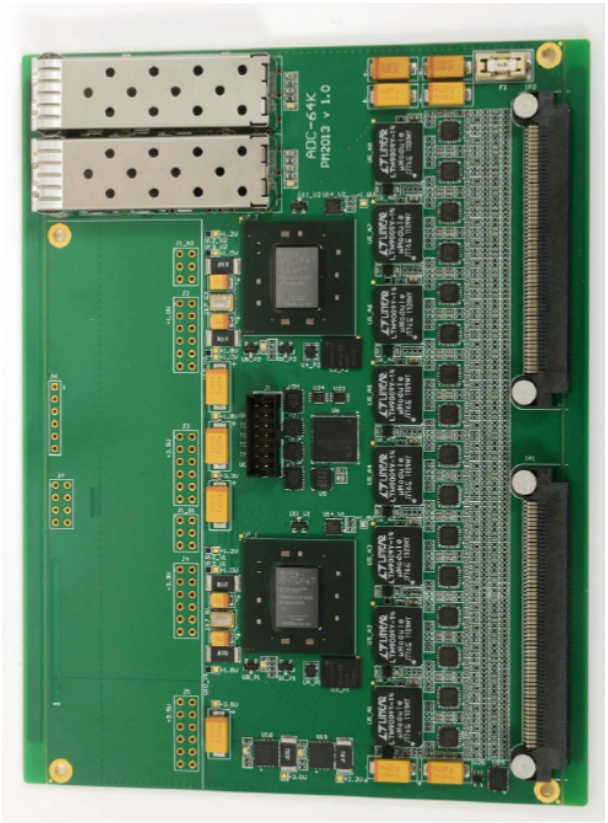

Intelligent front-end electronics
EMC volume
-25°C
Preamp.
PWO II
Photo sensor
Digitizer
Sampling ADC
FPGA
On-line pulse-data Processing:
Feature Extraction
Sampling ADC
Clock
Sync. signals
slow control
Optical link
Hits-data
Data Concentrator
Event pre-building
Pile-up correction
Data calibration
Time Distribution
SODANET
CN
Event builder
On-line computing
Data storage





EMC Front-End Electronics





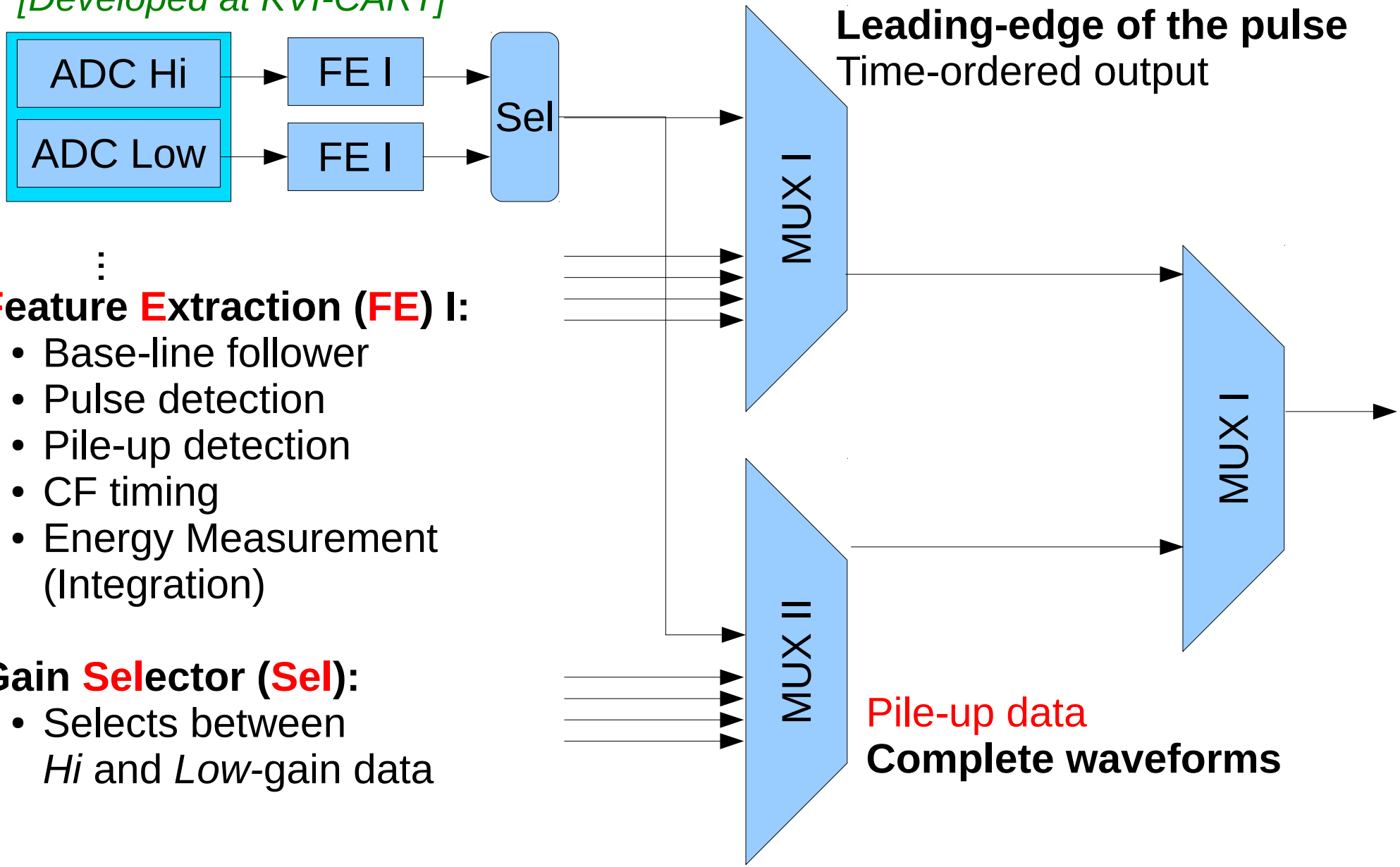
EMC digitizer:

- 64 ADC channels (32 dual-gain readout channels)
- 14 bit resolution
- 80-125 MHz sampling rate
- On-line detection of hits, extraction of hit information, pulse pile-up recovery by two Xilinx Kintex-7 FPGAs

Digitizers are located in radiation area → precautions have to be taken against configuration changes and SEU in FPGAs

Feature-Extraction Algorithm

[Developed at KVI-CART]



Feature Extraction (FE) I:

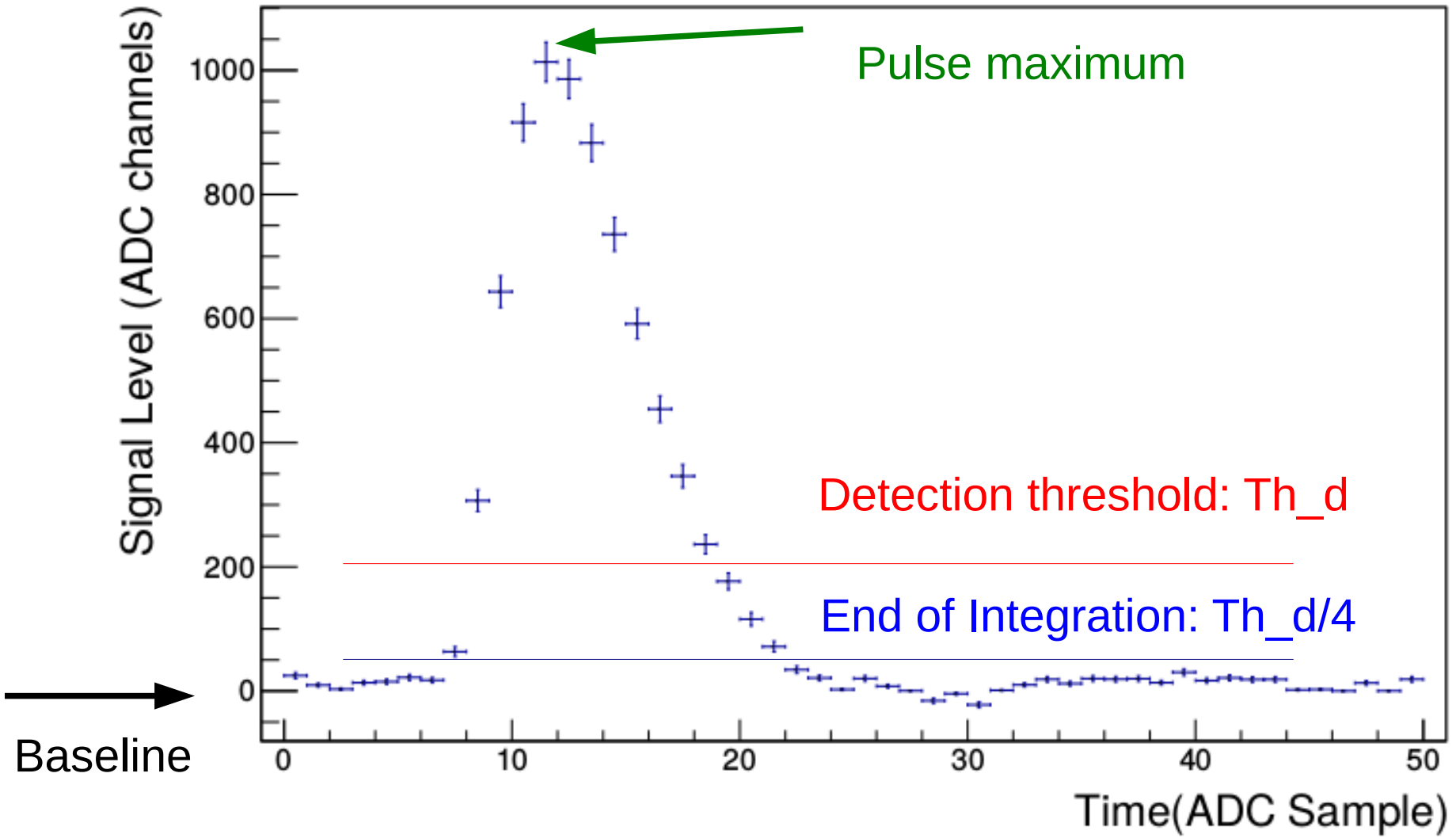
- Base-line follower
- Pulse detection
- Pile-up detection
- CF timing
- Energy Measurement (Integration)

Gain Selector (Sel):

- Selects between *Hi* and *Low*-gain data

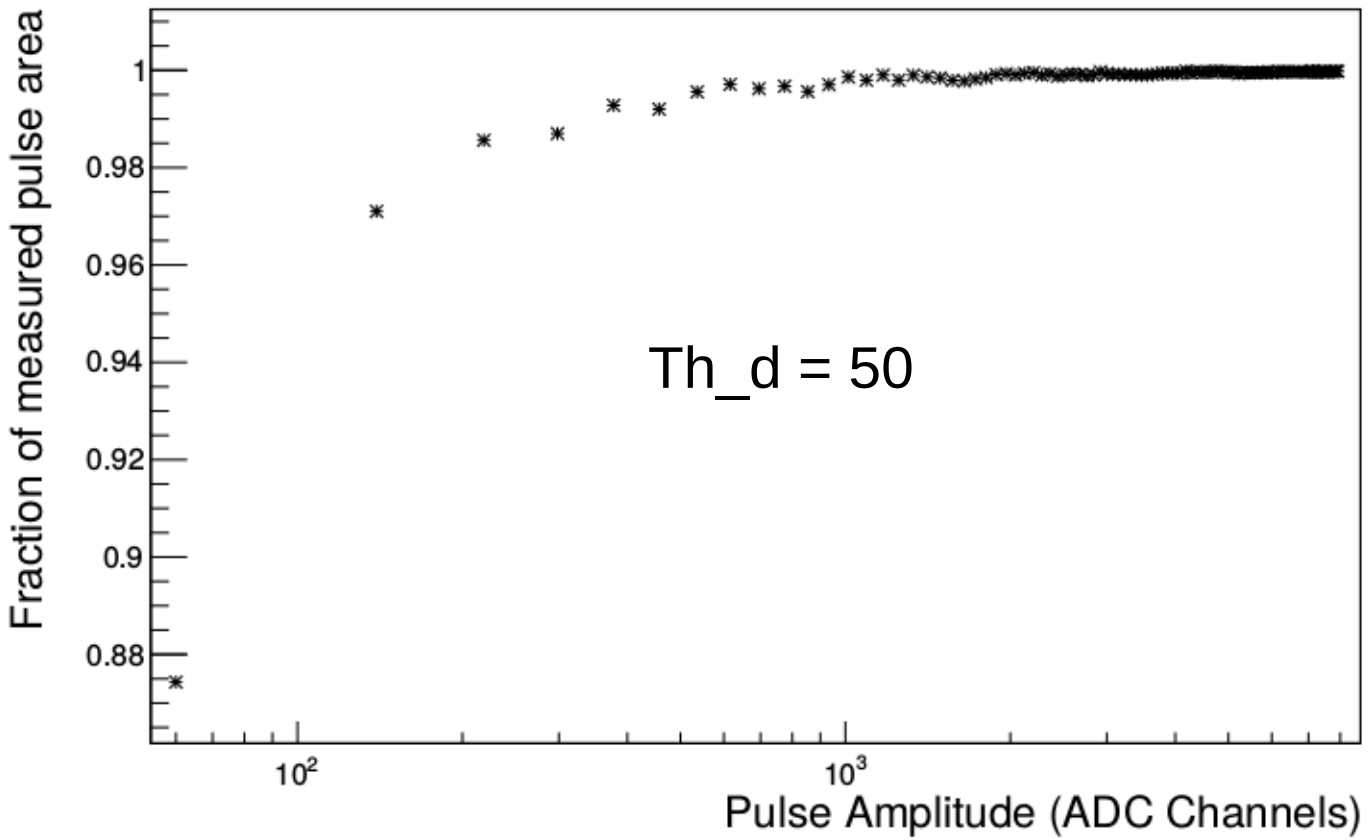
FE-I

ADC samples after base-line subtraction



Integration includes: one sample before Th_d till last sample above Th_d/4

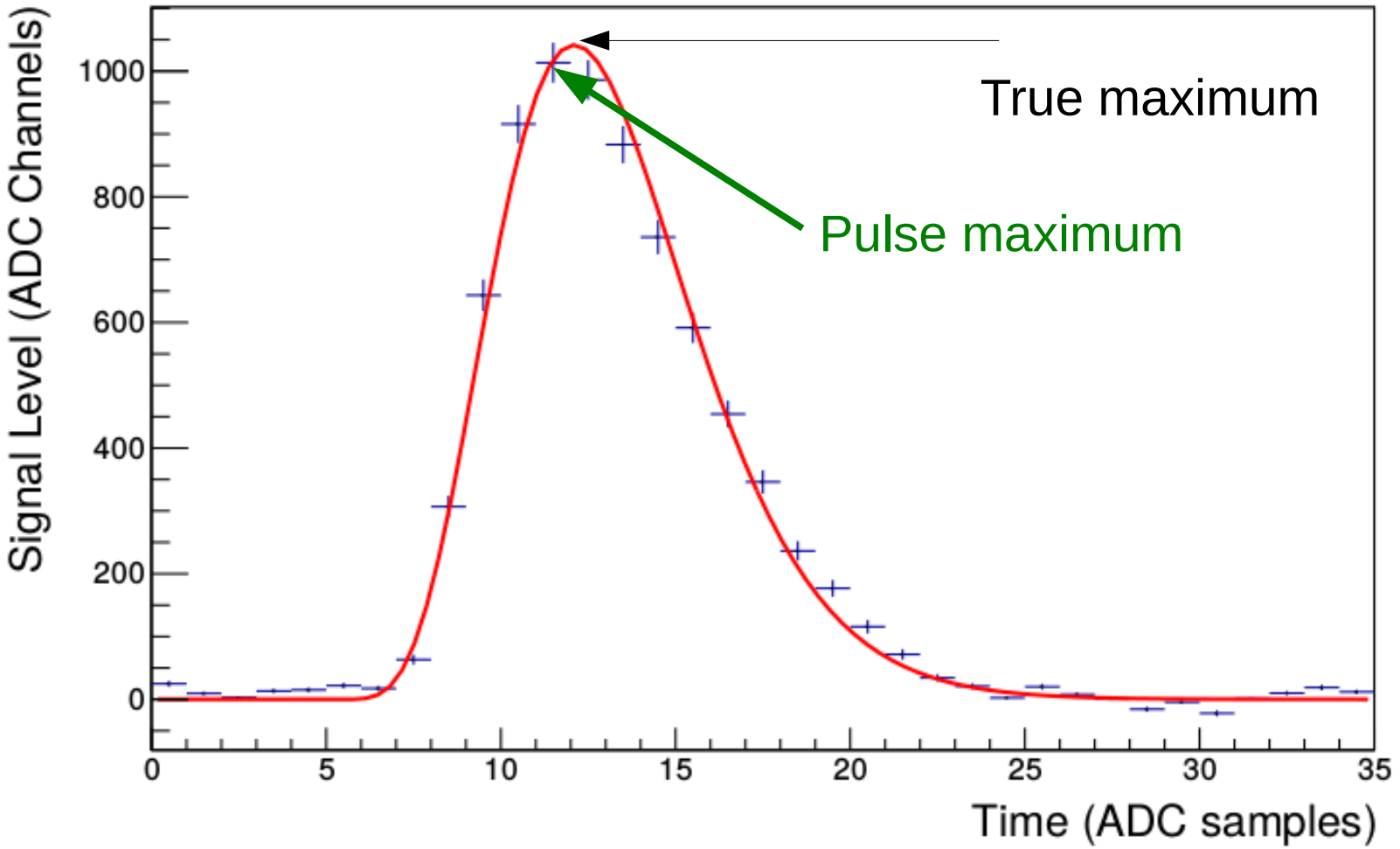
Pulse-Area Measurement



Summing samples above threshold:

- Reduces noise induced by ADC
- Not complete pulse-integration near threshold: **Acceptable?**

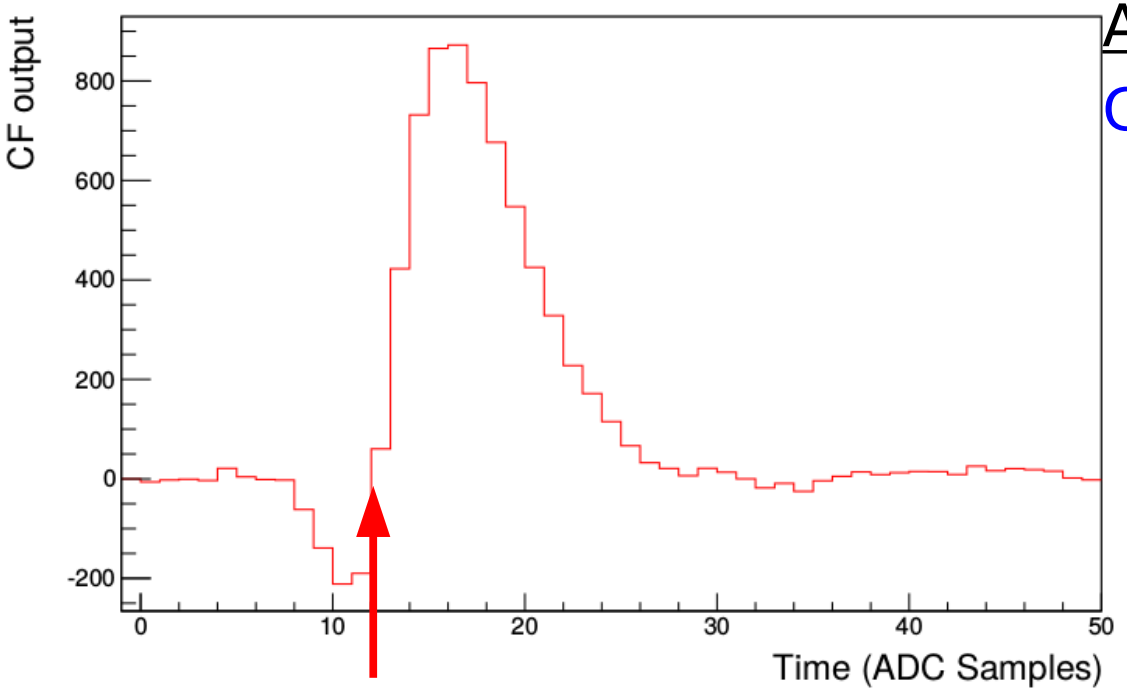
Precise Amplitude Measurement



Measured “maximum value” is always smaller than the pulse amplitude:

- Difference depends on pulse phase (fraction) between start of the pulse and phase of sampling clock

Time Measurement



Time stamp: zero-crossing
(linear regression)

Analogue-like implementation:

CFT(n) = MWD(n-*d*) – *R*·MWD(n)

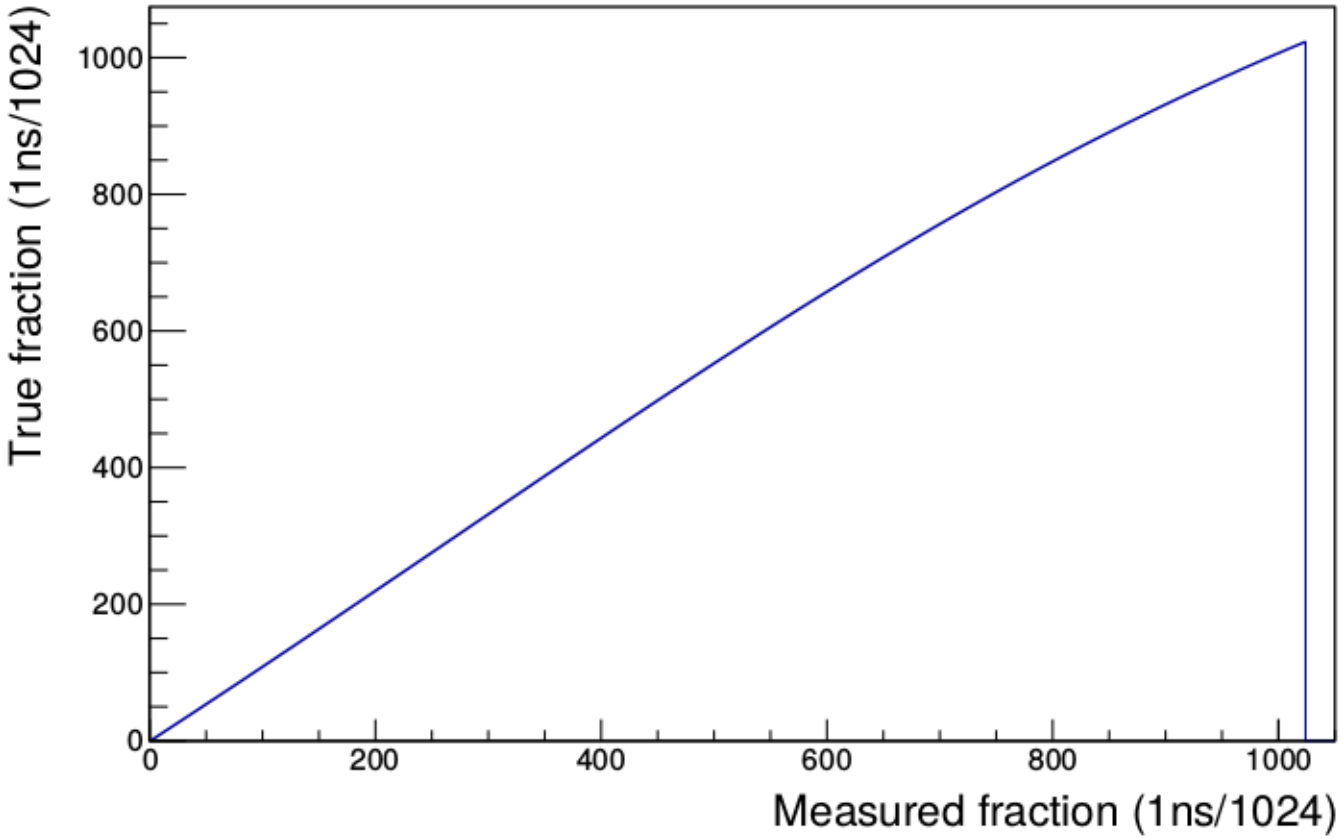
- Delay *d* = signal rise time
- Fraction *R* – to select most linear part of the signal leading edge (**R=1/4**)
- *N* – number for the linear regression
- Symmetry against zero level

Linear regression induces some error in the time measurement

Has to be corrected

Time-Stamp Correction

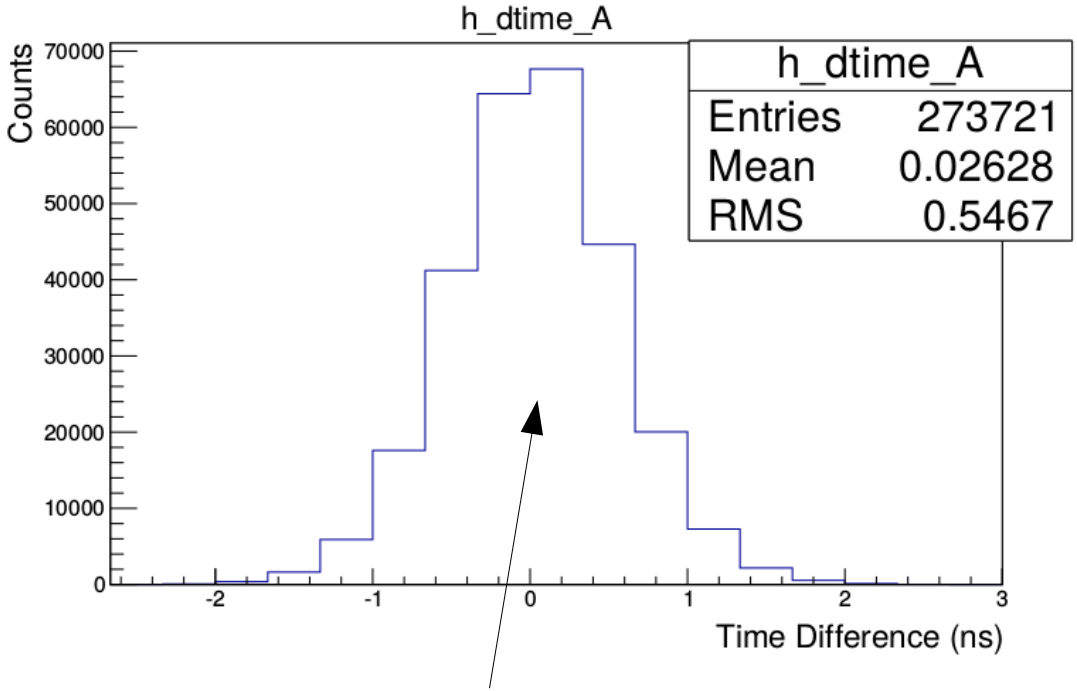
- A correction LUT is calculated using measured waveform
- Correction is performed at the data concentrator
- There is one LUT for one DC (channel-to-channel pulse-shape variations can not be corrected)



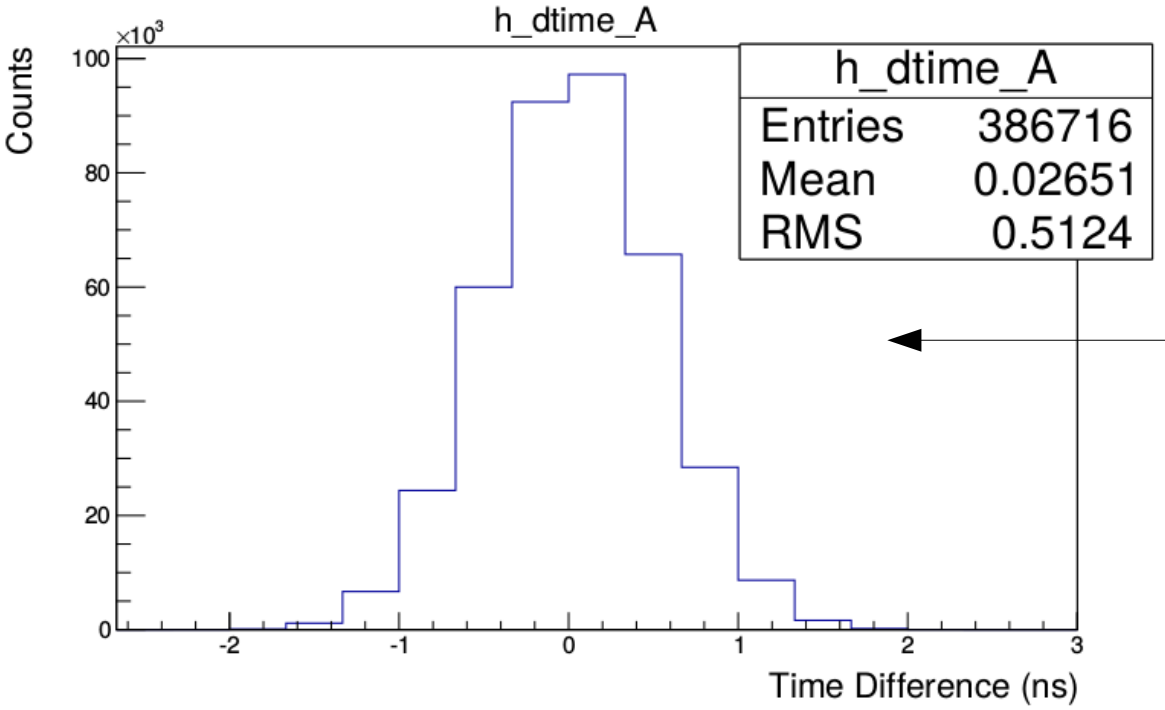
Correction in Action

Measurement with LED pulser and EMC proto

Time difference between two channels



No Correction

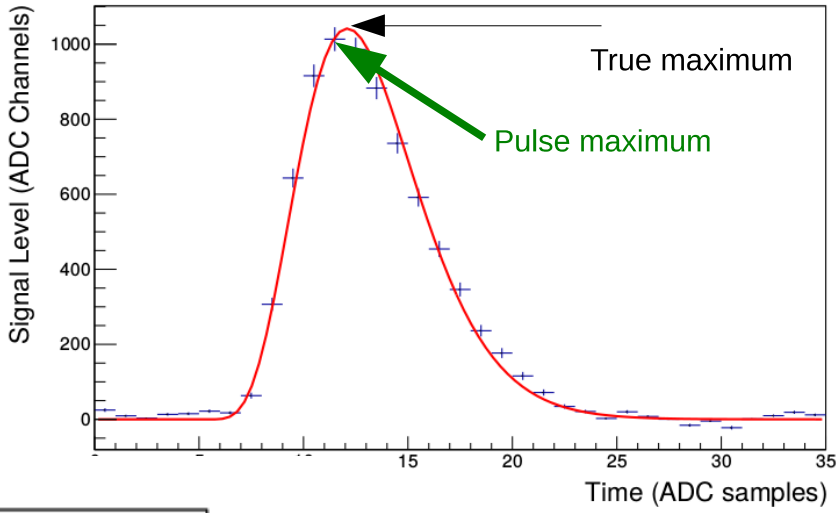


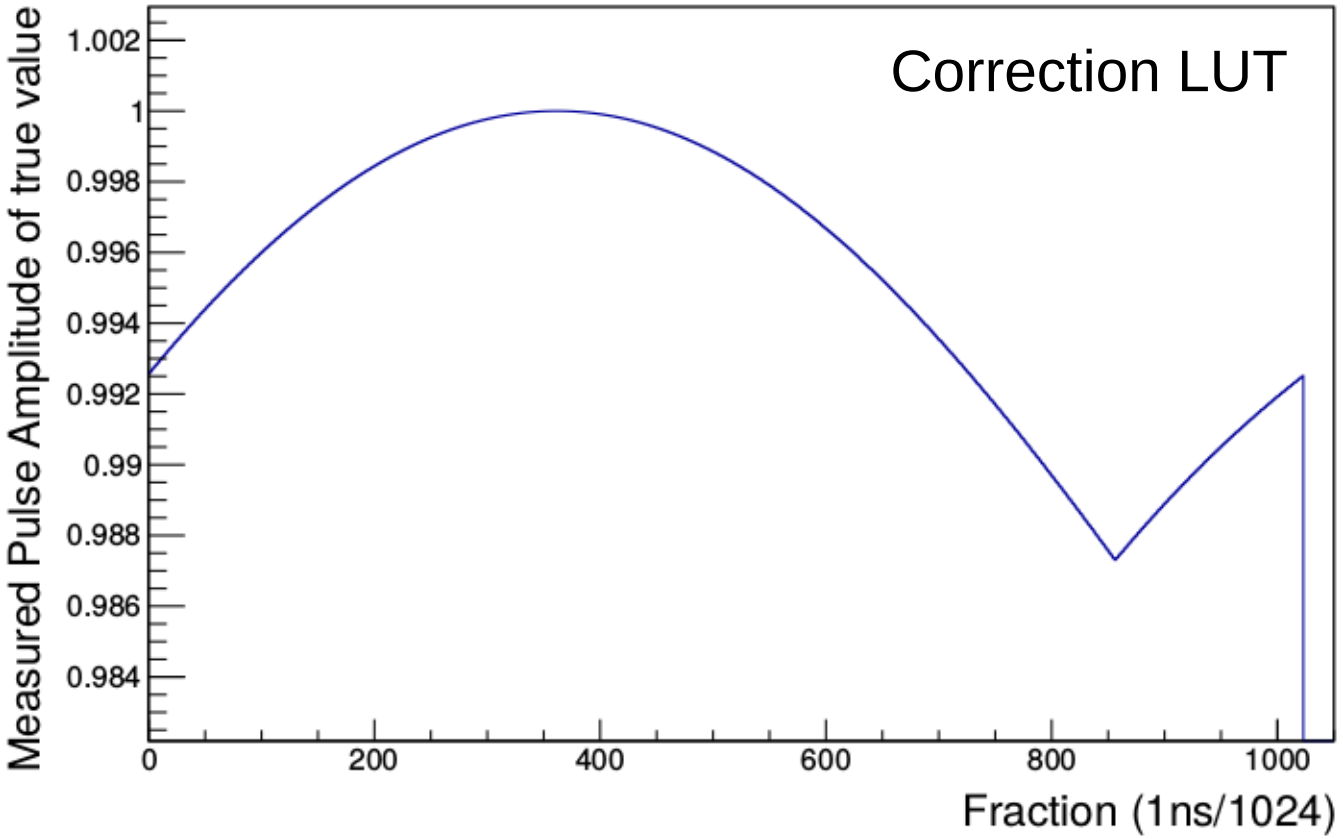
With on-line correction

It Works!

Correction for “Maximum”

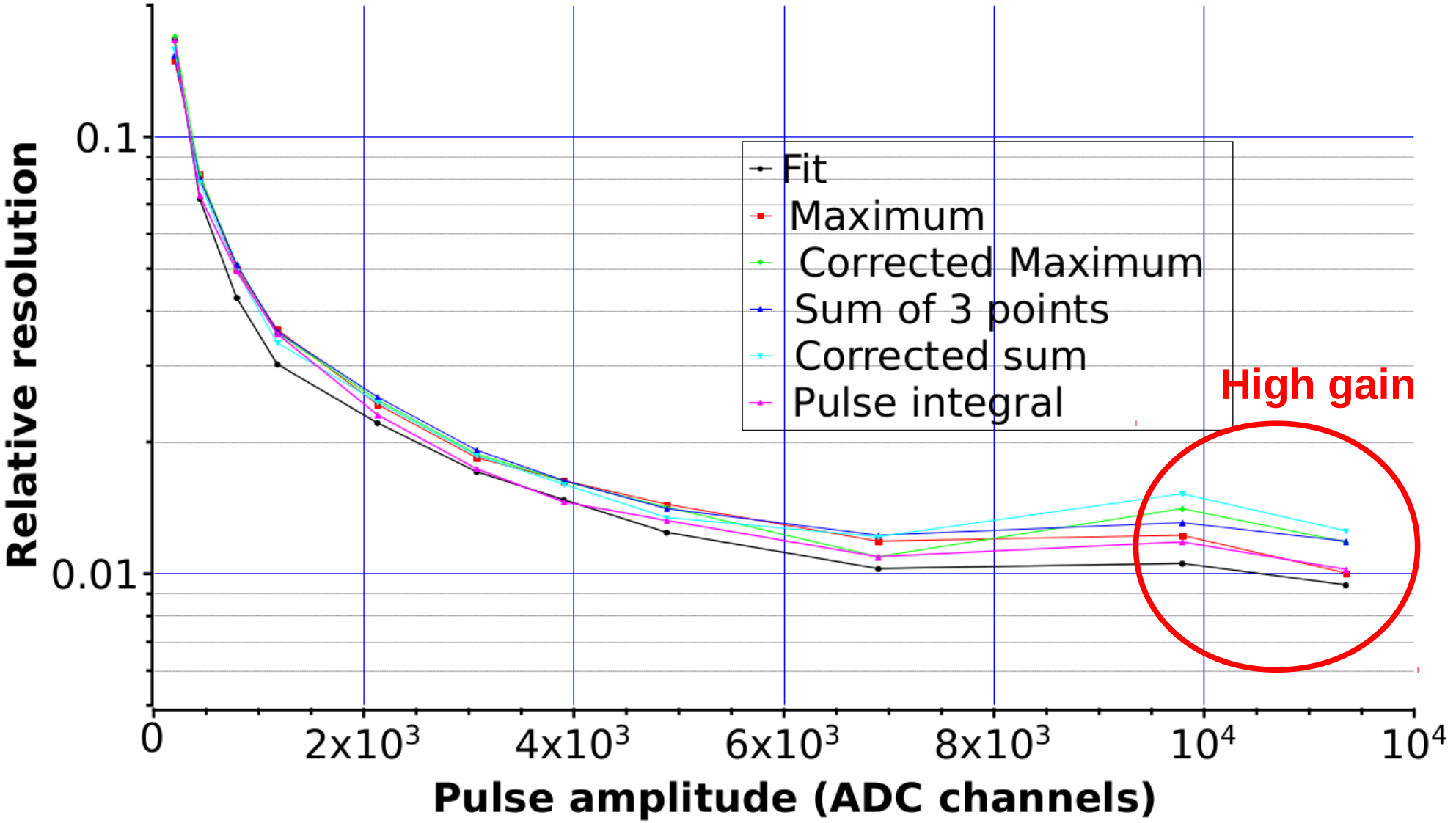
Correction LUT can be constructed to calculate true amplitude of a pulse





- No threshold effects as with “integration”
- Very sensitive to pulse shape (no gain in resolution for realistic case)

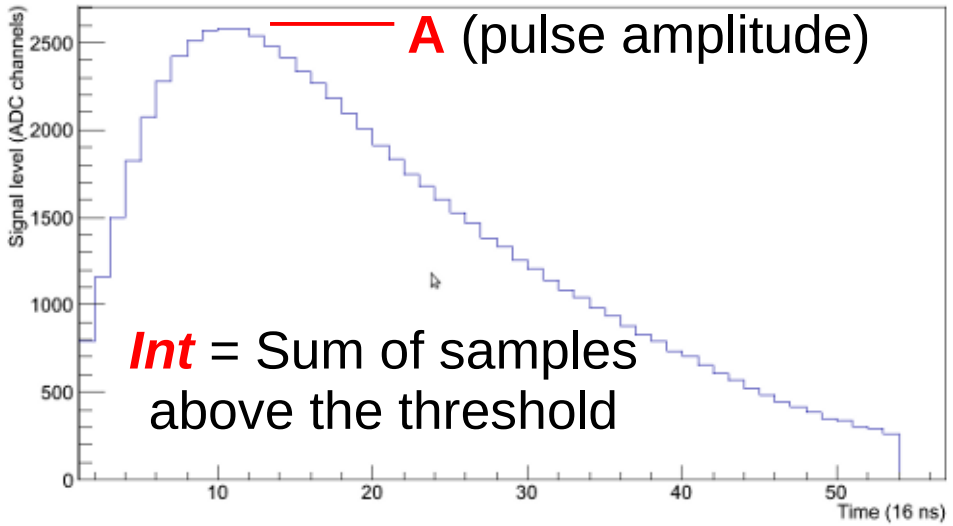
The Best “Energy” Measurement



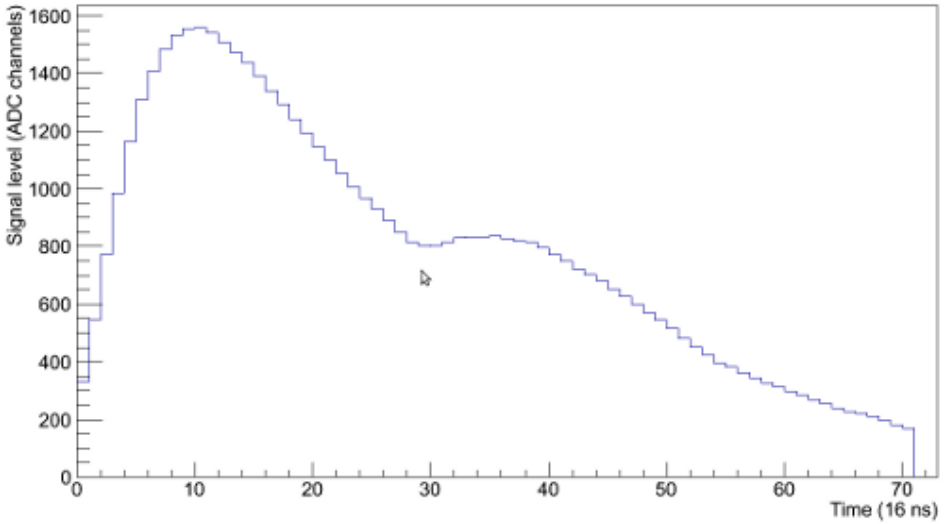
Integration – the best option?

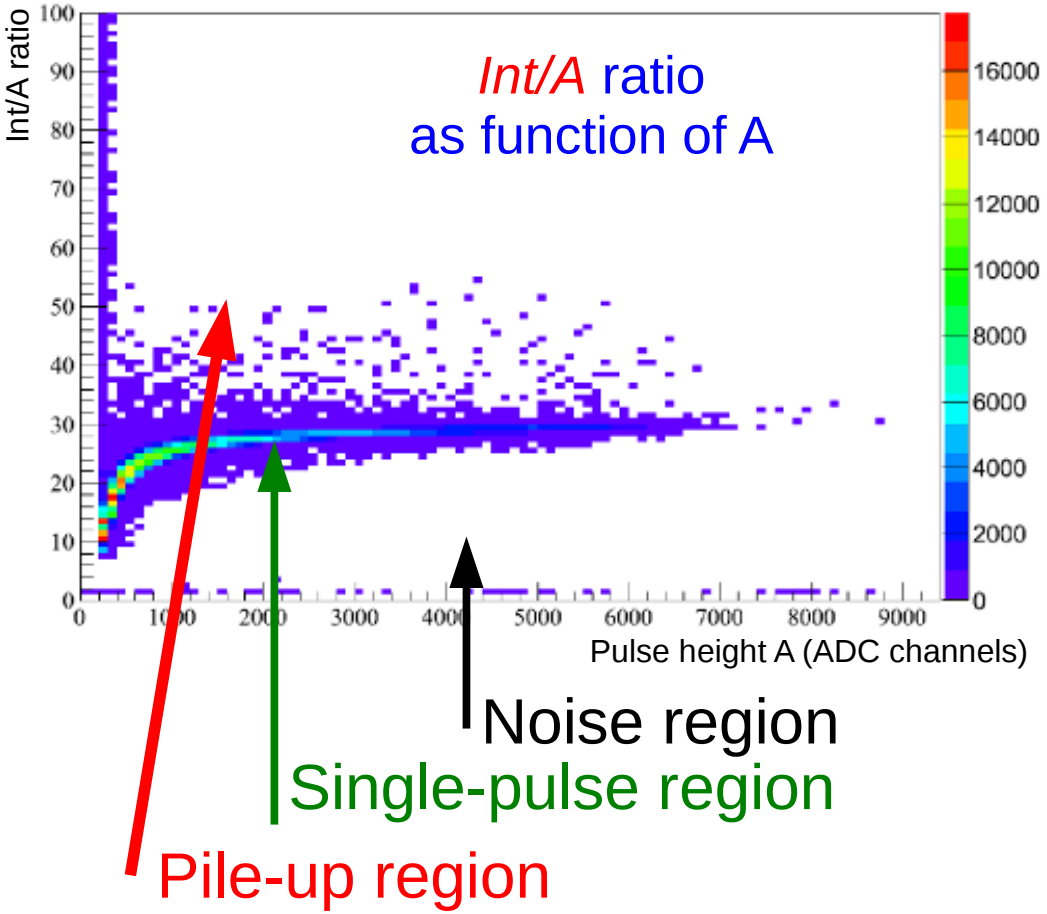
Pile-up Detection

If samples above threshold satisfy ***Int/A*** criterion → Pulse is detected



Pile-up event identified on-line





Pulse-detection works properly:

- Detection of single pulses

Detection of pile-up structures

Data Concentrator

Implemented and tested:

- Time ordering of data from all inputs
- Packaging of the output data according to the SODANET protocol
- On-line data reduction (combing data from two different channels related to two LAAPDs, reading out one crystal; data-streams from two digitizers)
- On-line Calibration
- On-line correction of time-stamps (amplitudes)

To be done:

- On-line pile-up recovery

Work in progress:

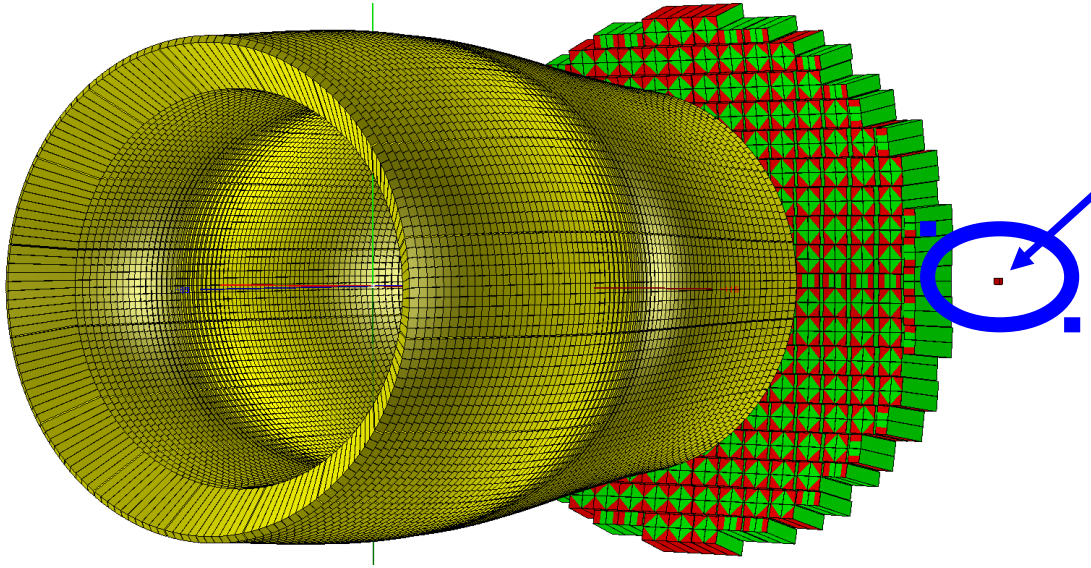
- Change speed of synchronous optical links to 2 Gb/s

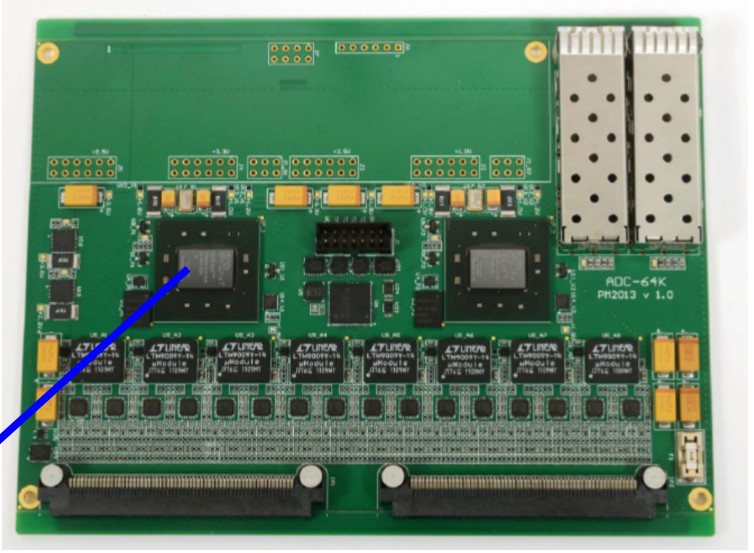
Expected Particle-Flux at FPGA Location

Monte Carlo input:

- Flux of charged particles and neutrons

Hossein Moeini, Ganesh Tambave (KVI-CART)





(Pawel Marciniewski, U. Uppsala)

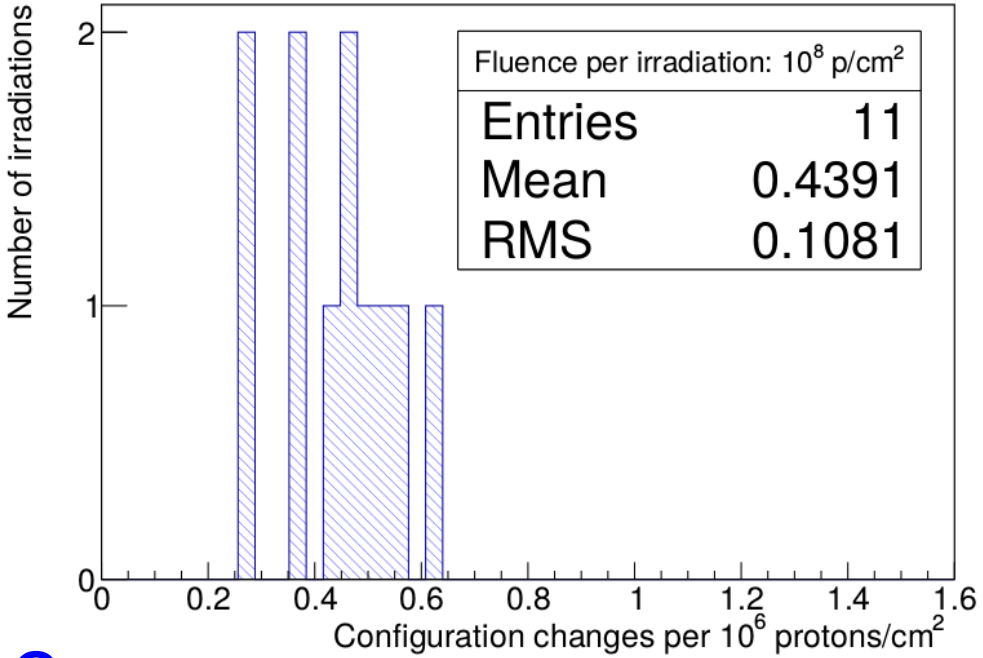
- FPGA on the EMC digitizer implemented in PANDAroot
- Estimated flux of charged particles: ~ 70 /s/cm^2
- **Neutron flux to be estimated** by FLUKA simulations

Irradiation of Kintex-7 (XC7K325T)

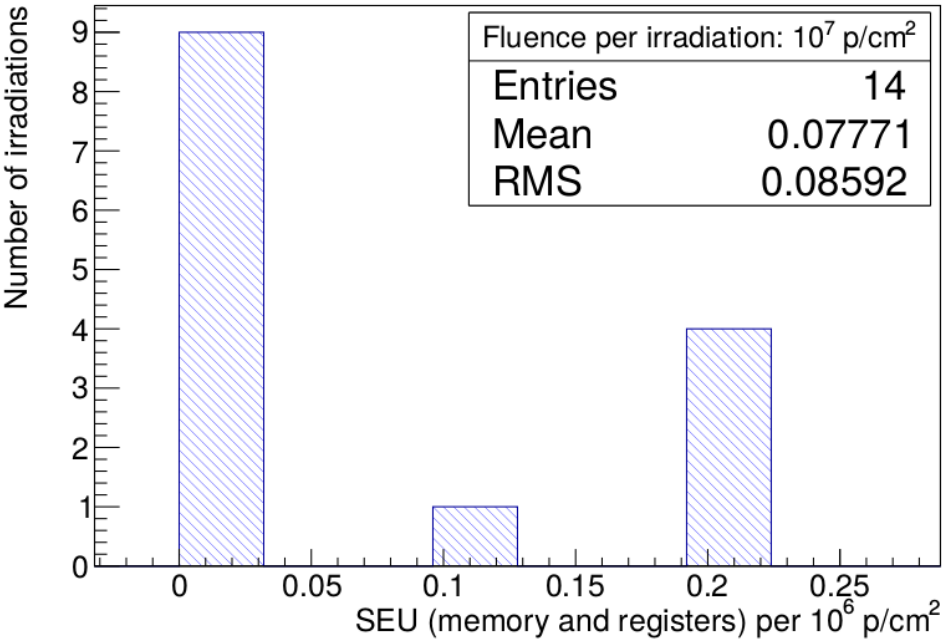
150 MeV protons, homogeneous field

Resources involved in the SEU test: Registers: **54%** (=$2.2 \cdot 10^5$)
Block RAM: **86%** (=$1.4 \cdot 10^4$ kb)

Configuration changes per 10^6 /cm^2



SEU per 10^6 /cm^2



On average:

configuration changes:
0.44(11) per 10^6 /cm^2

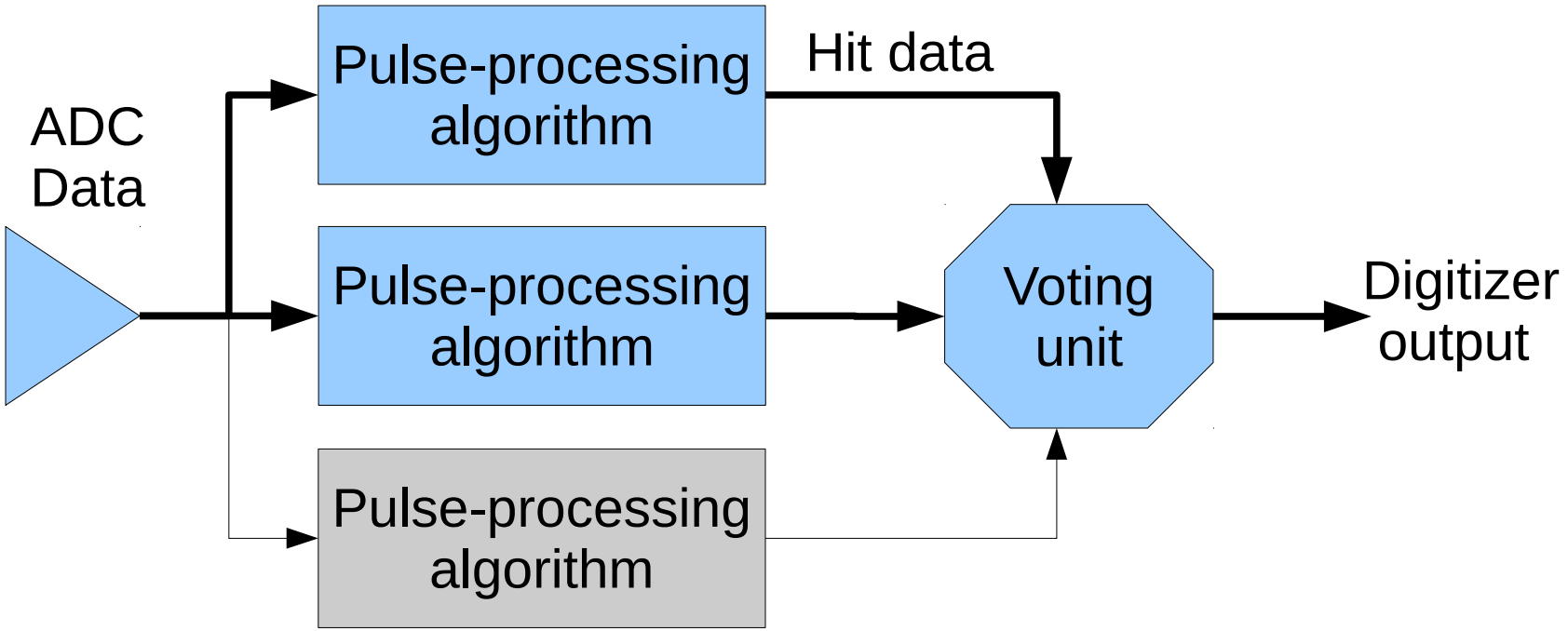
SEU events:
0.08(8) per 10^6 /cm^2

➔54 min operation without reconfiguration (incl. safety factor 10)

Modular Triple Redundancy (MTR)

Current implementation contains double redundancy:
in case of SEU, the output of one module will be corrupted.
Measurement: **~ 2 ms** recovery time after SEU error

➔ Extend mean operation time of EMC digitizer in radiation environment:
MTR: 3 identical implementations in FPGA.
for the most sensitive modules of the data-processing algorithm



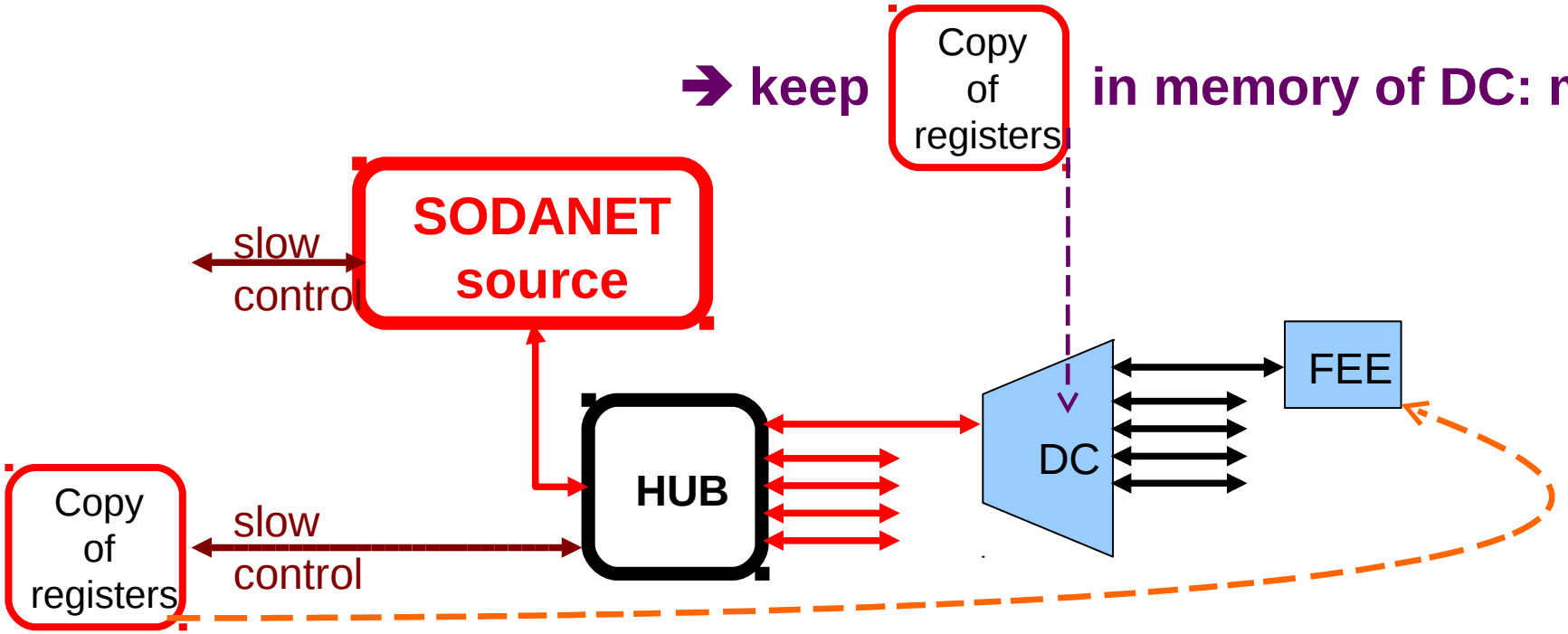
Recovery of EMC Digitizer

configuration change requires restart:

- reconfigure FPGA
- reprogram registers used by the on-line feature-extraction algorithm

Fast reprogramming is crucial for decreasing the dead time:

too slow (~seconds) via slow control



Together with a fast reload of configuration from a flash memory: implemented reboot procedure takes ~ 10 ms

Outlook

- **Feature extraction**
  - The algorithm is fixed, the pile-up recovery still has to be implemented in the data concentrator/digitizer

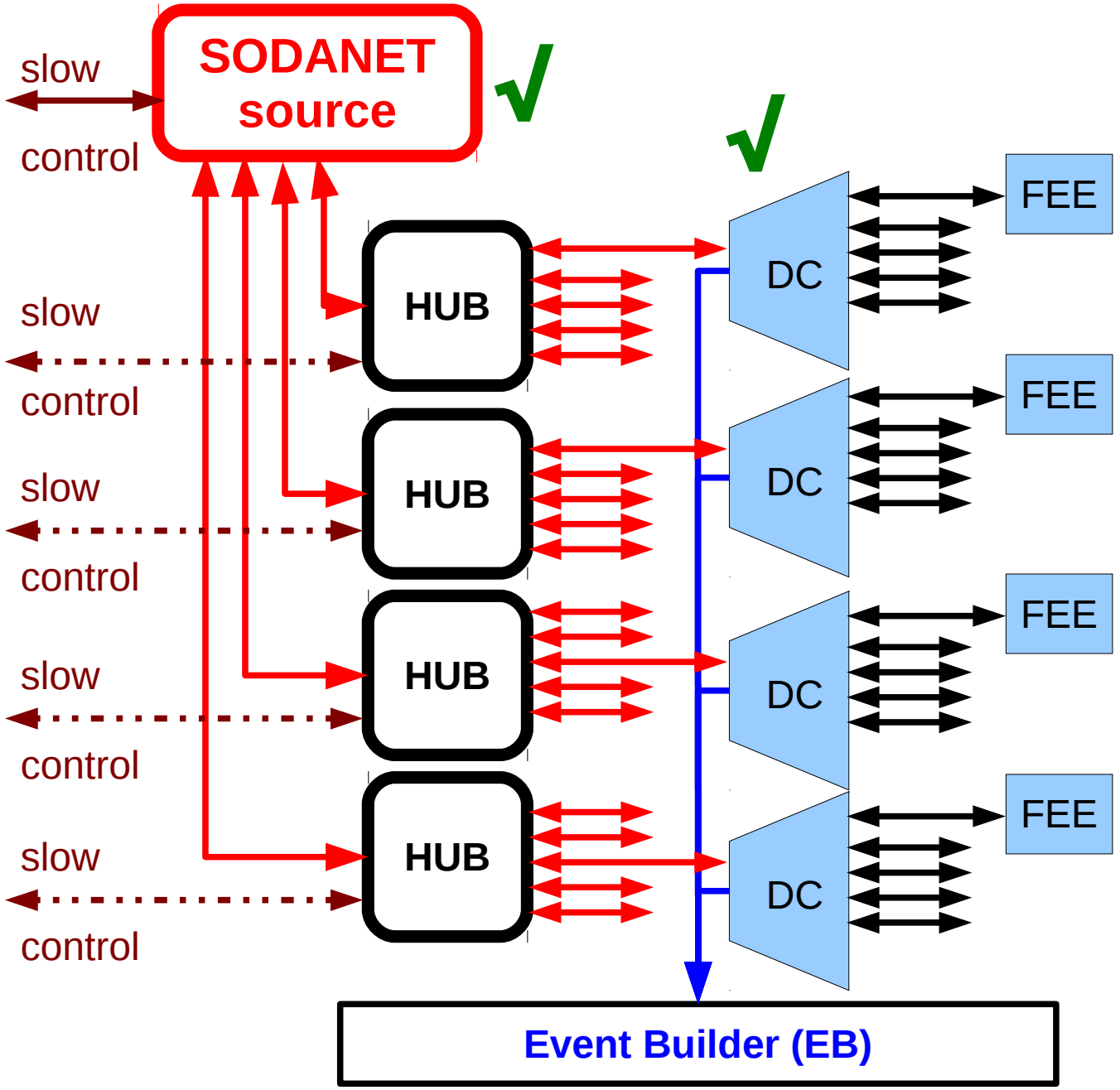
- **Radiation hardness**
  - Kintex-7 is less (X 3) prone to configuration changes even though it has X10 more resources
  - Measurements reveal SEUs always together with configuration change → SEUs much less probable than configuration change

  - Digitizer using standard FPGA can be used in PANDA EMC
  - Modular Triple Redundancy is feasible for data-processing → will be implemented in next revision of EMC digitizer

  - Fast reboot of the EMC digitizer (~10 ms) lowers dead-time of the readout system

- **Next steps:**
  - Test readout with external SODA source, connect FEE with burst-building network (CN): beginning of 2015
  - Irradiate “Kintex” version of the digitizer

SODANET Topology



SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
  - DC → source: slow control, used for time calibration

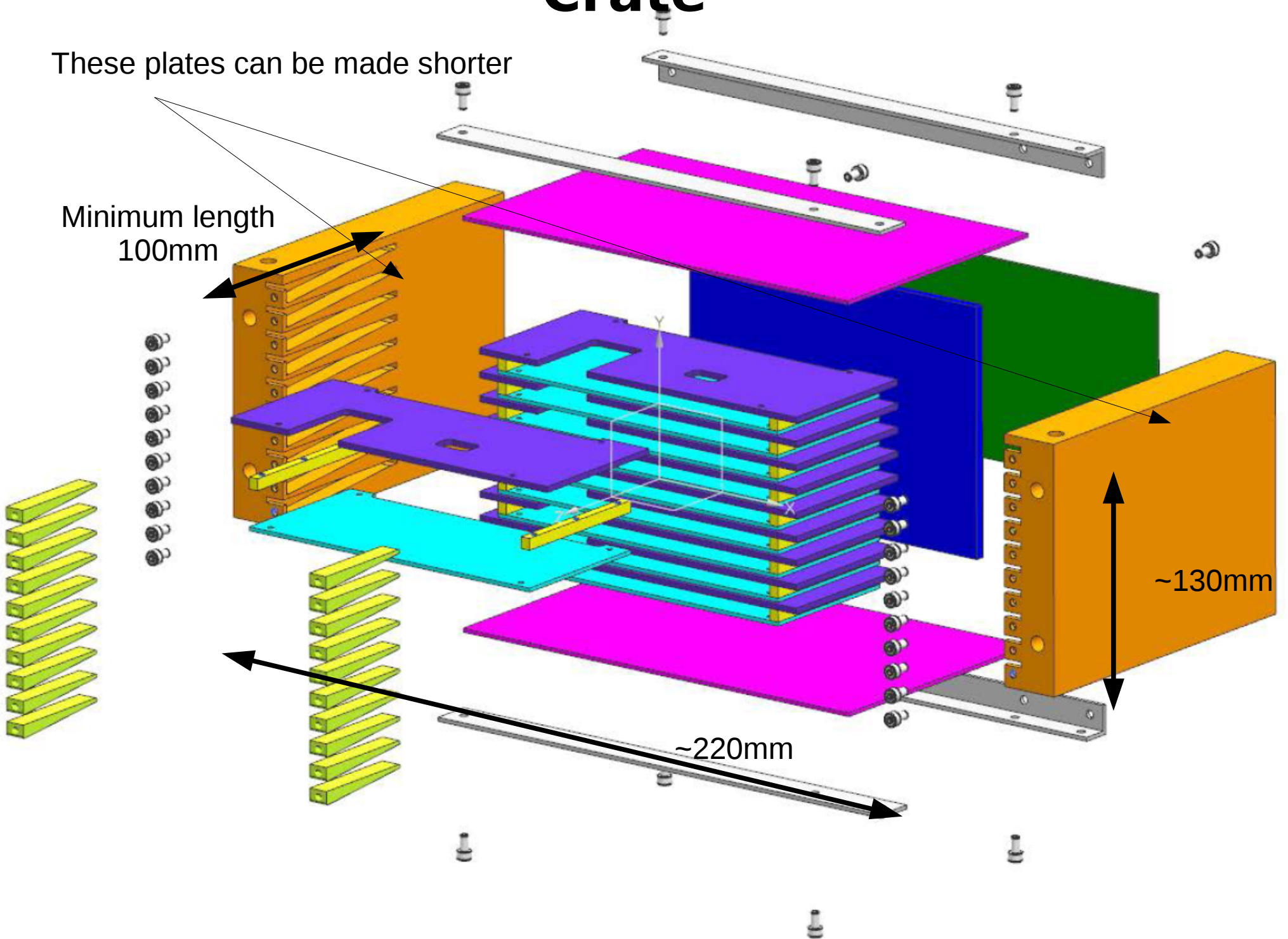
Data link (DC → EB):

- Unidirectional Ethernet

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

Crate


These plates can be made shorter
Minimum length
100mm
~130mm
~220mm