PASTTREC: A New 8-channel ASIC for STT & FT

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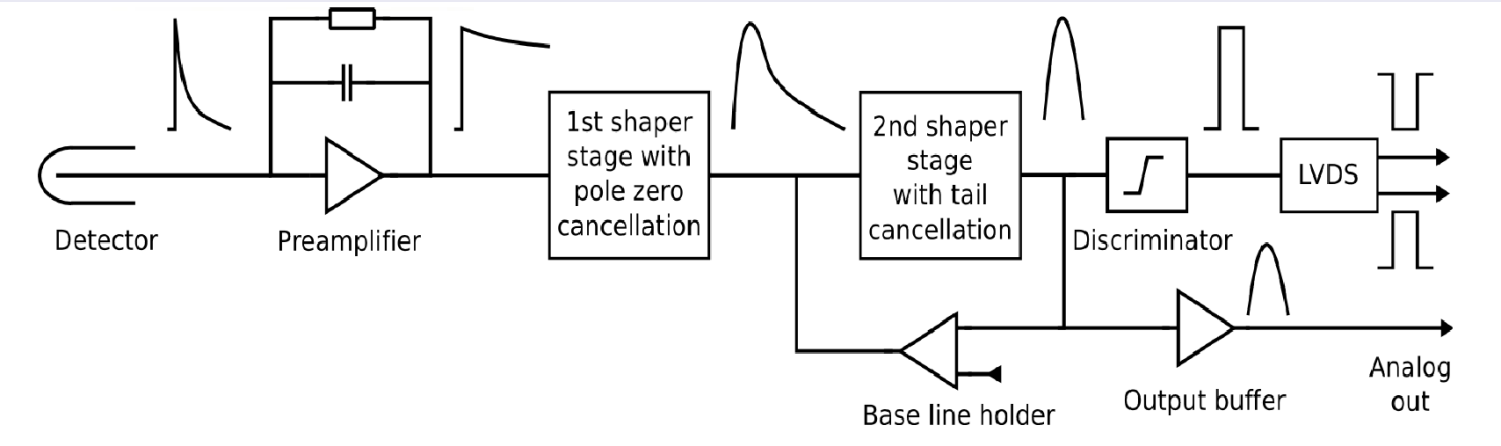
Outline

1st prototype of front–end ASIC for straw tubes

Specification

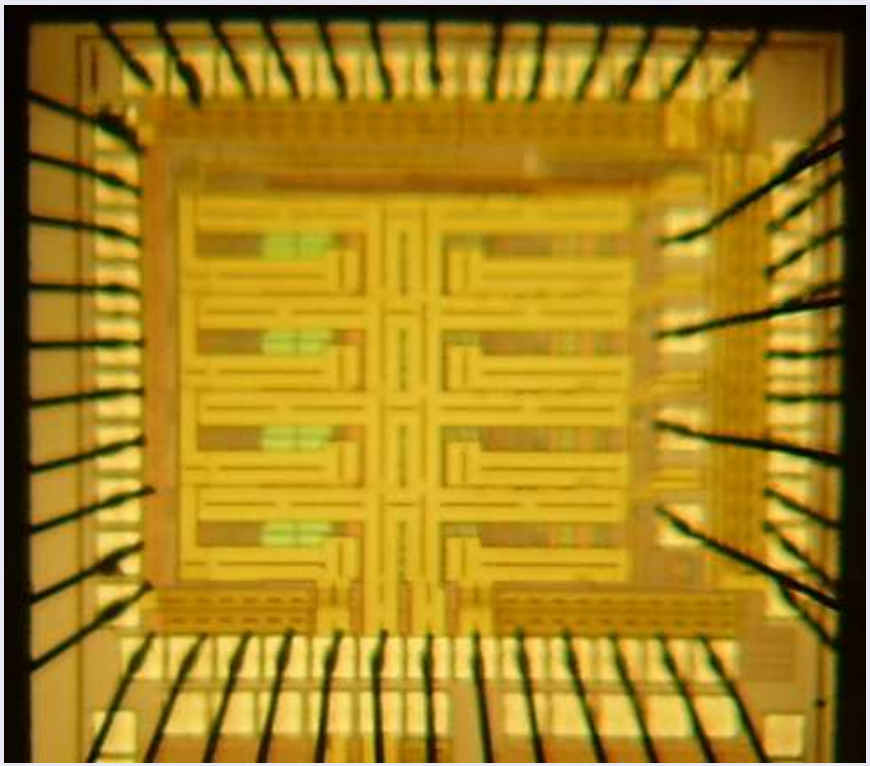


Features

- CSP with variable gain and time constant
- CR–RC^2 shaper with variable peaking time
- Ion tail cancellation circuit with trimming
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time and ToT measurements
- Fast LVDS output
- Buffered analog output

1st prototype of front–end ASIC for straw tubes
Results

Chip size 1.5 *times* 1.2 mm^2



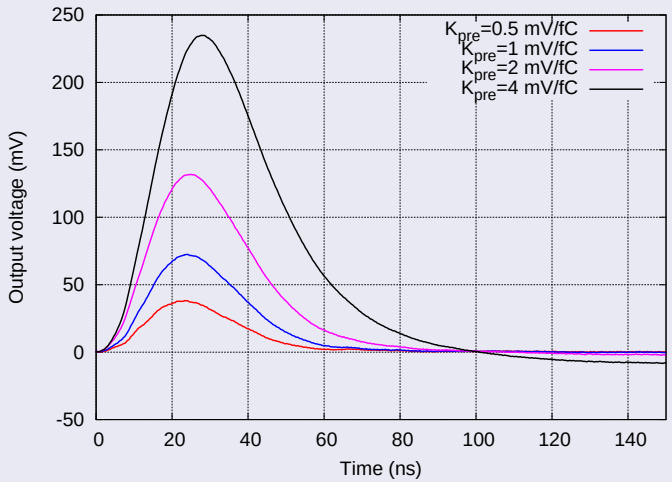
Basic data

- AMS 0.35 μm CMOS process
- Four channels
- Channel size: 200 $\times$ 1130 μm^2
- Power consumption ~28 mW/ch
- Lack of peripherals – biasing and thresholds setting externally
- Succesfully used in few testbeams

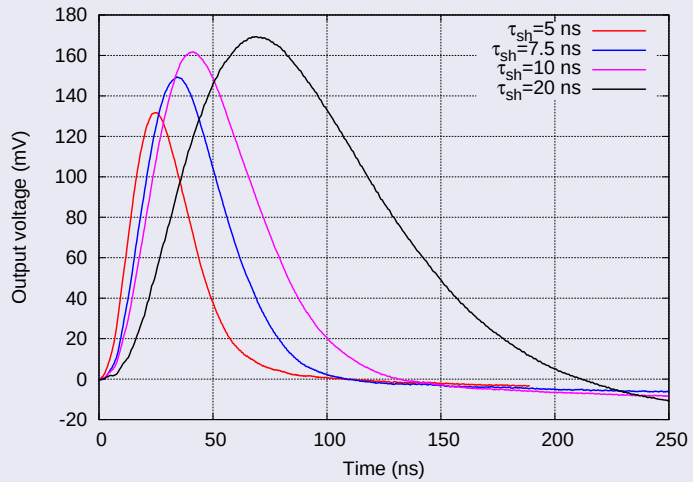
1st prototype of front–end ASIC for straw tubes

Results – pulses

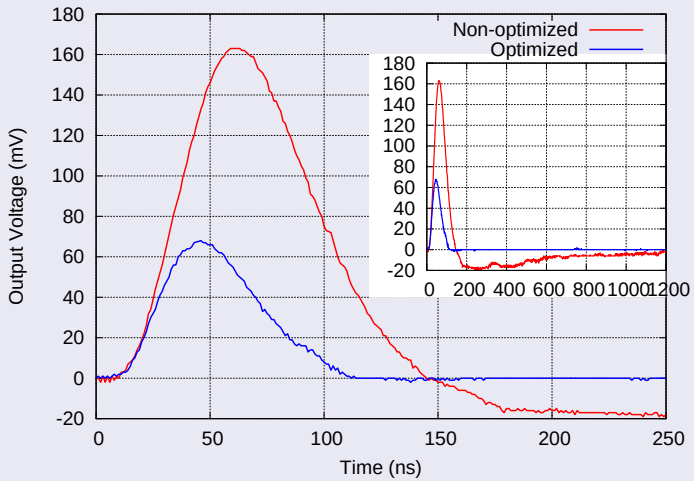
Pulses for various gain (4 – 24 mV/fC)



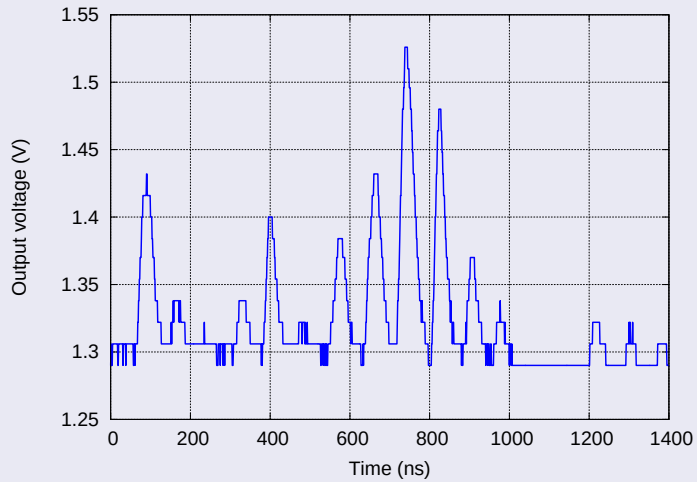
Pulses for various T_P (25 – 67 ns)



Response for ^{55}Fe X–rays (TC settings affects gain)



High rate



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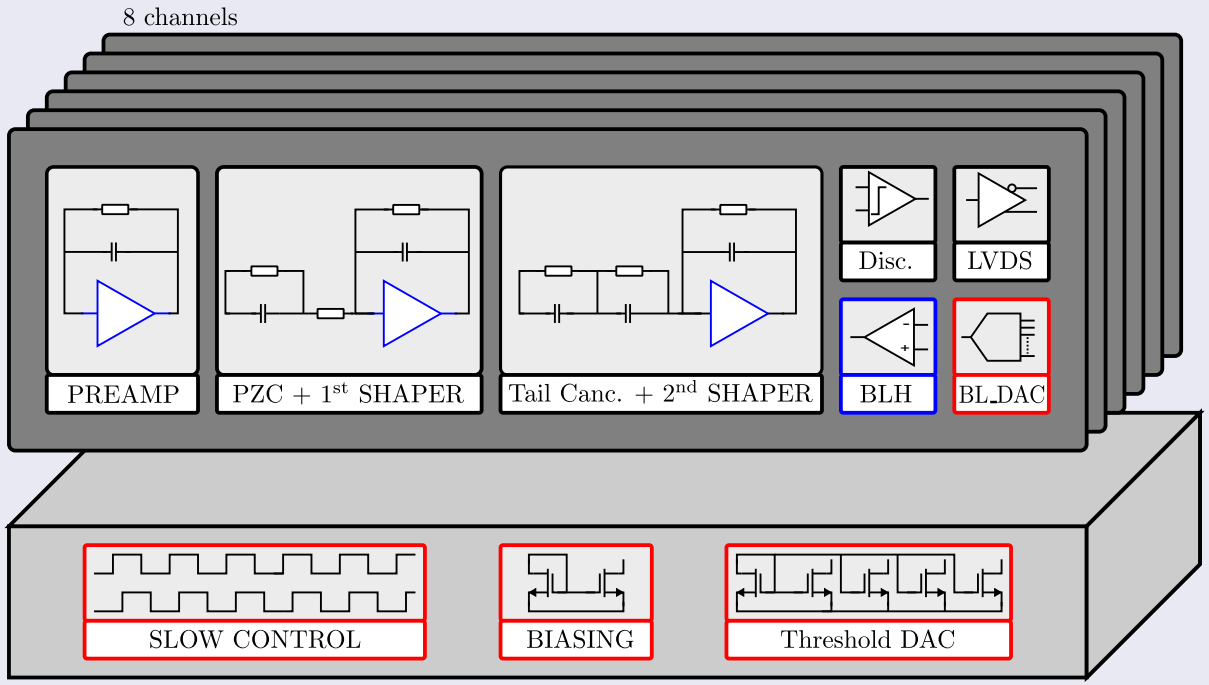
Block diagram



- New added features:
  - Internal biasing
  - Global DAC for threshold
  - Trimming DACs for each ch.
  - Slow control responsible for communication and settings
- 8 channels
- Fabricated in Oct 2014
- Under tests now (see Paweł's talk)

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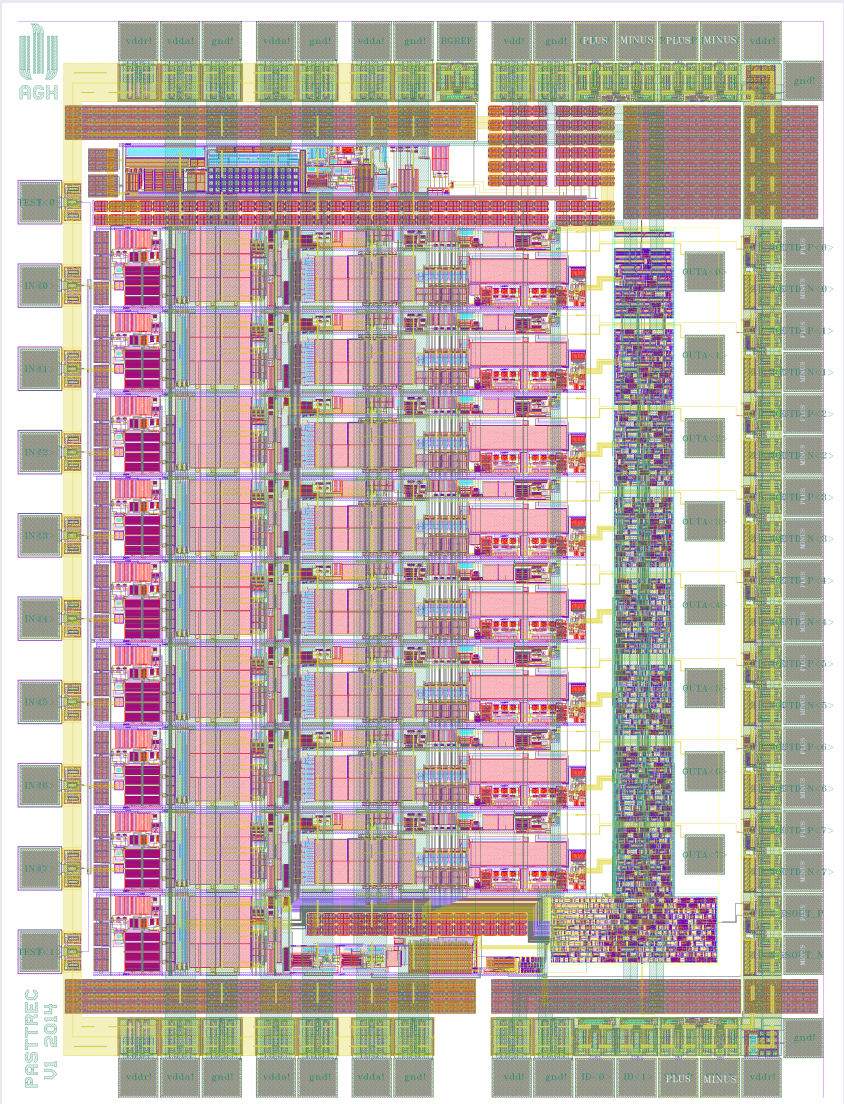
Layout – 1.95 × 2.6 mm^2



Improvements

- New faster amplifiers
- Redesigned BLH circuit: Baseline dispersion below 35 mV_{p-p}
- 5 bit DACs added to trimm baseline (2 mV accuracy)

Performance

- Total power 34.2 mW/ch
- Gain in range of 1 to 7 mV/fC
- T_{peak} of ∼17, ∼23, ∼39 and ∼ 64 ns
- ENC below 3000 e^- for highest gain and 25 pF of C_{in}.

Summary and plans

Summary

- The first prototype of PASTTREC chip was fabricated:
  - Slow Control circuitry and all peripherals implemented
  - Problem in 1^{st} FE of high baseline dispersion overcome
  - Only slight improvements in speed – best T_P is around 17 ns
- PASTTREC already bonded to 6 readout boards, next 10 boards in progress

Plans

- Due to chip complexity and limited time for design, optimization was not complete, some modifications of PASTTREC would be still usefull:
  - improve speed to achieve 10 ns of T_P
  - increase range of possible gain values
- If we manage with the design, the PASTTREC_v2 submission could be planned for 26 May or 27 July