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GIESSEN

panda

PASTA Chip Status

Valentino Di Pietro
and Alberto Riccardi

PANDA LII. Collaboration Meeting, Gießen March 2015

Contents

- PASTA Chip
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  - Building blocks
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- Back to December
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PANDA STrip ASIC

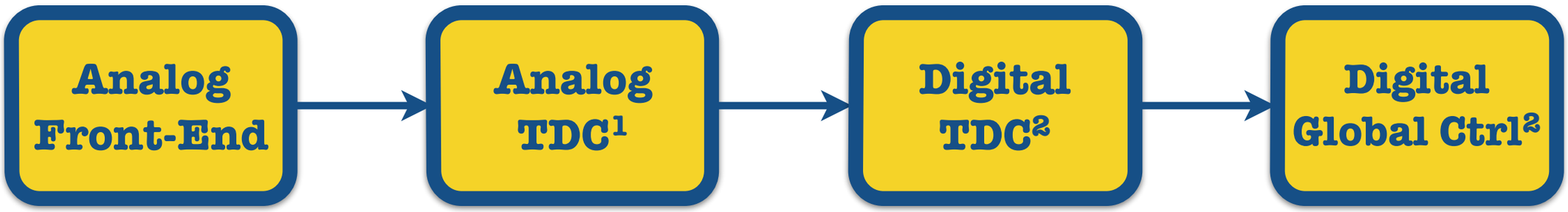
Specifications

- Event rate up to 40kHz
- Detector capacitance (15 - 25)pF
- Input charge (1 - 40)fC

Goals

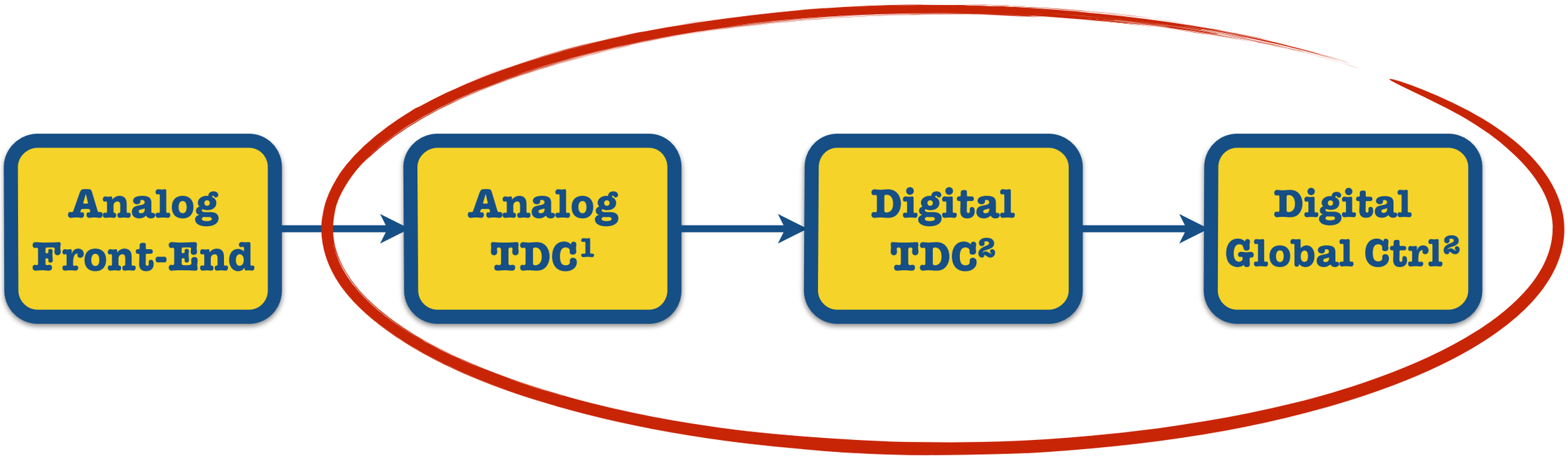
- Linear time measurement with input charge
- Noise < 1500 e^-
- Power consumption ~ 4mW per channel

PASTA Chip



1: Alberto Riccardi
2: André Goerres

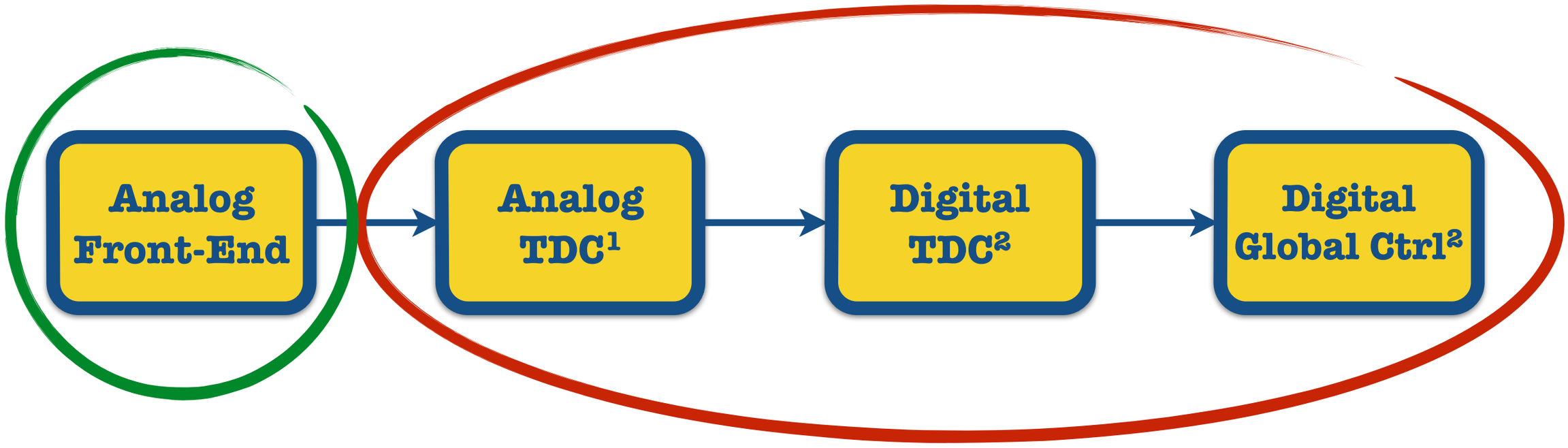
PASTA Chip



Based on TOF-PET

1: Alberto Riccardi
2: André Goerres

PASTA Chip



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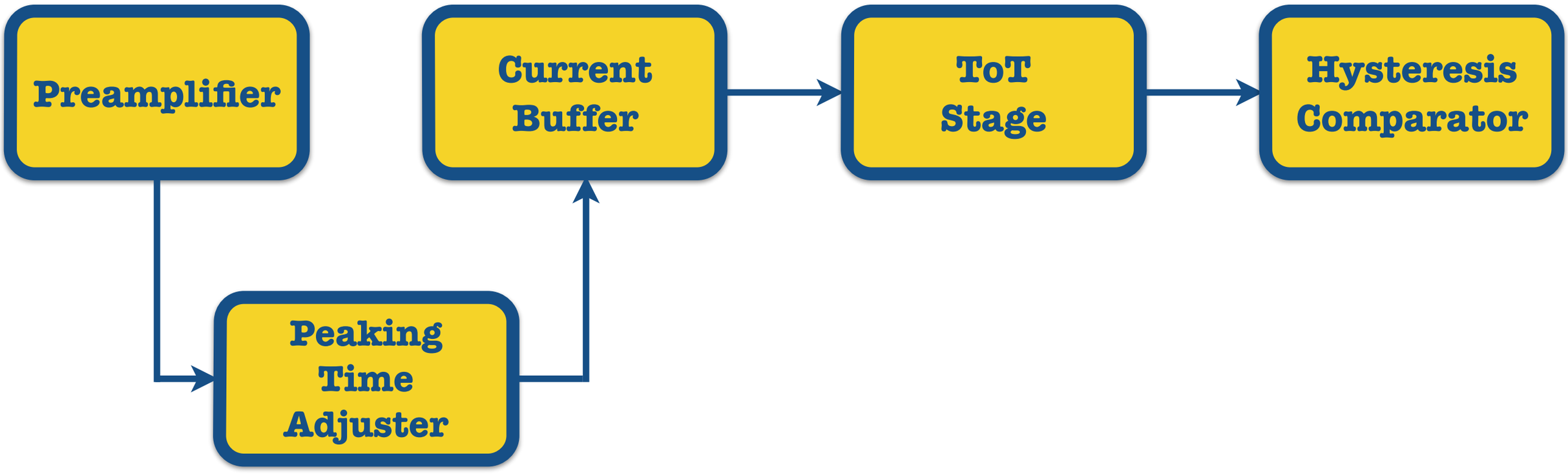
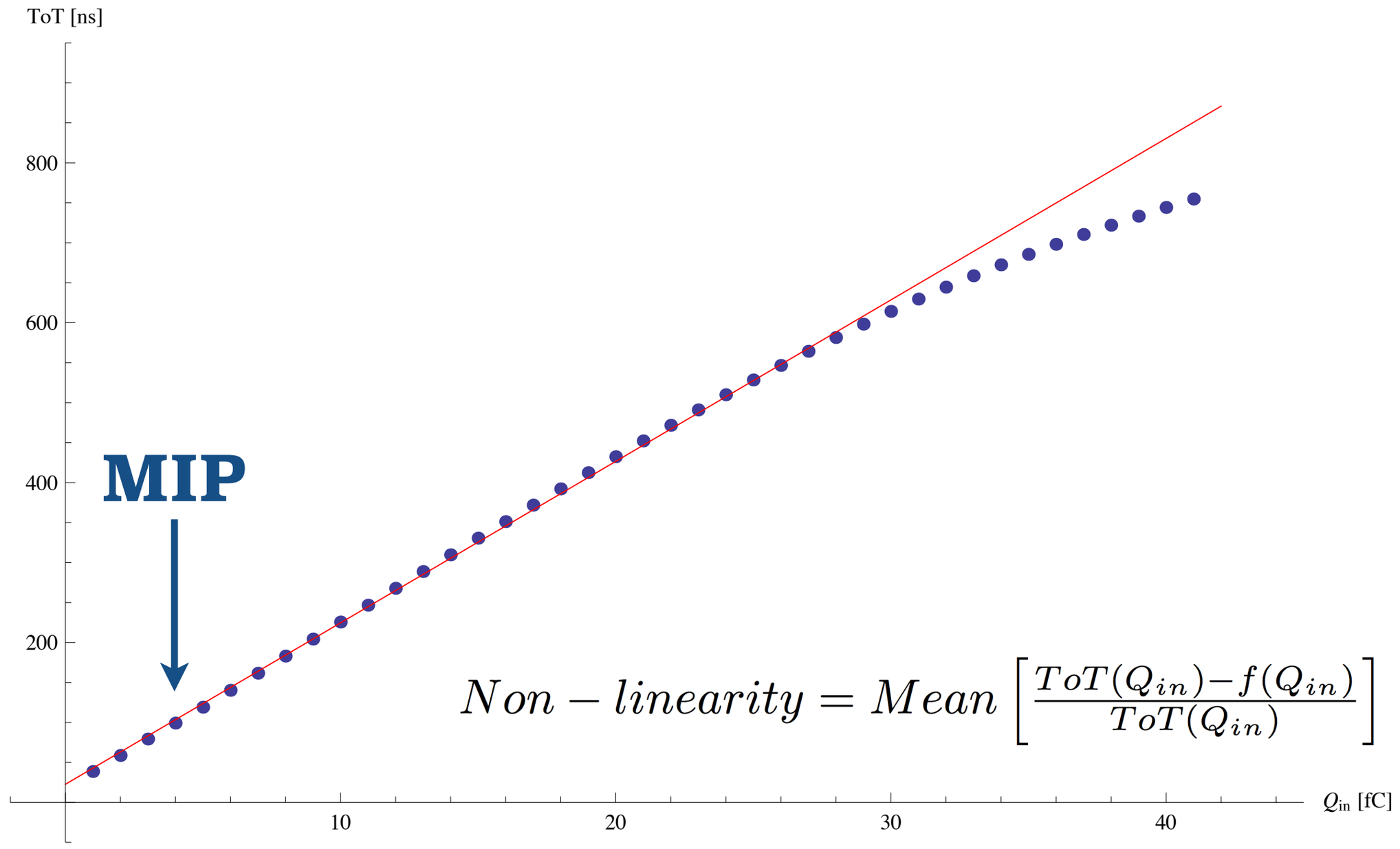
PASTA Analog FE



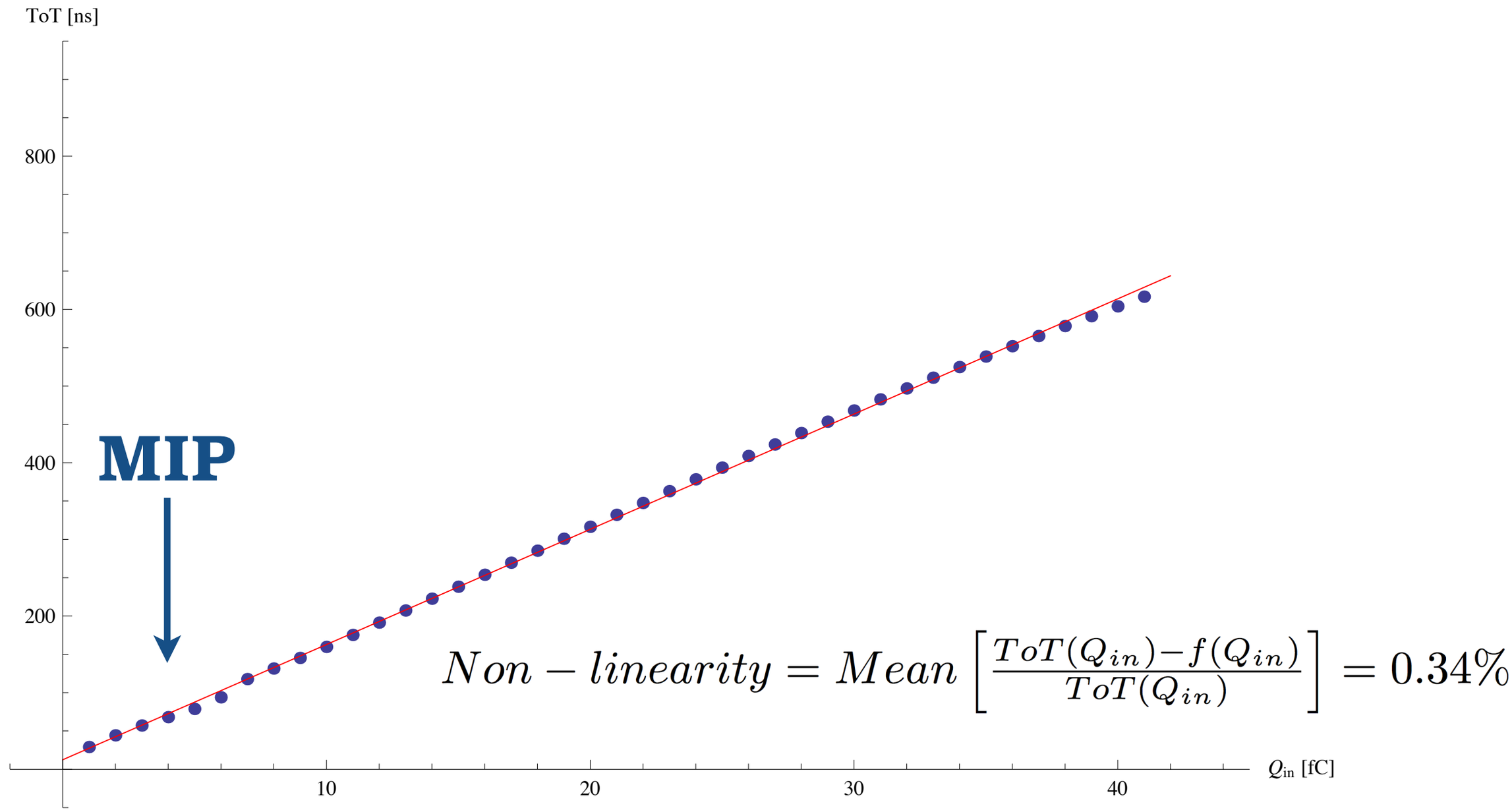
$\sim 10ns \rightarrow \sim 30ns$

pSconf*: Linearity



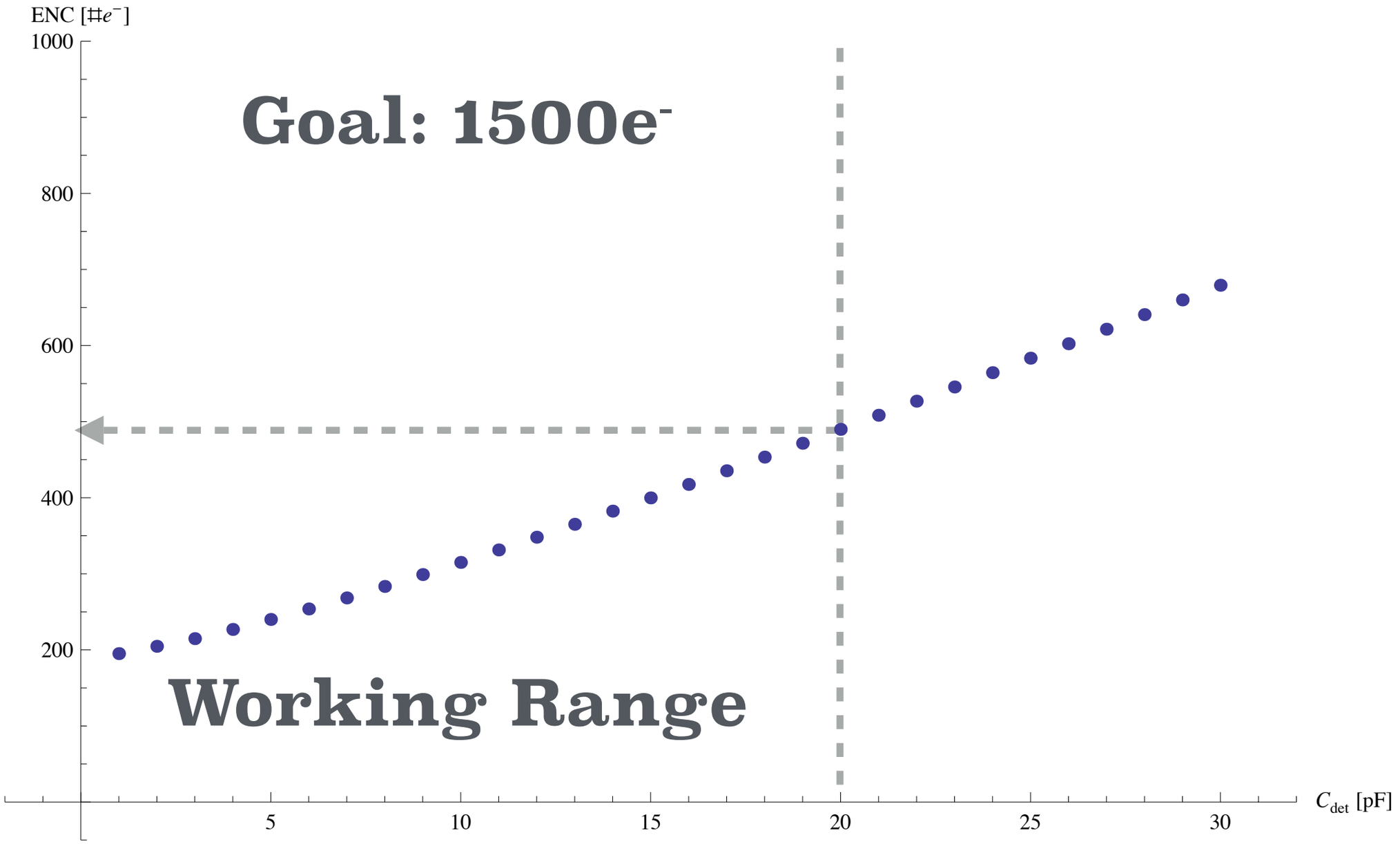
***pSconf: Configuration for the p-type Strips**

nSconf*: Linearity

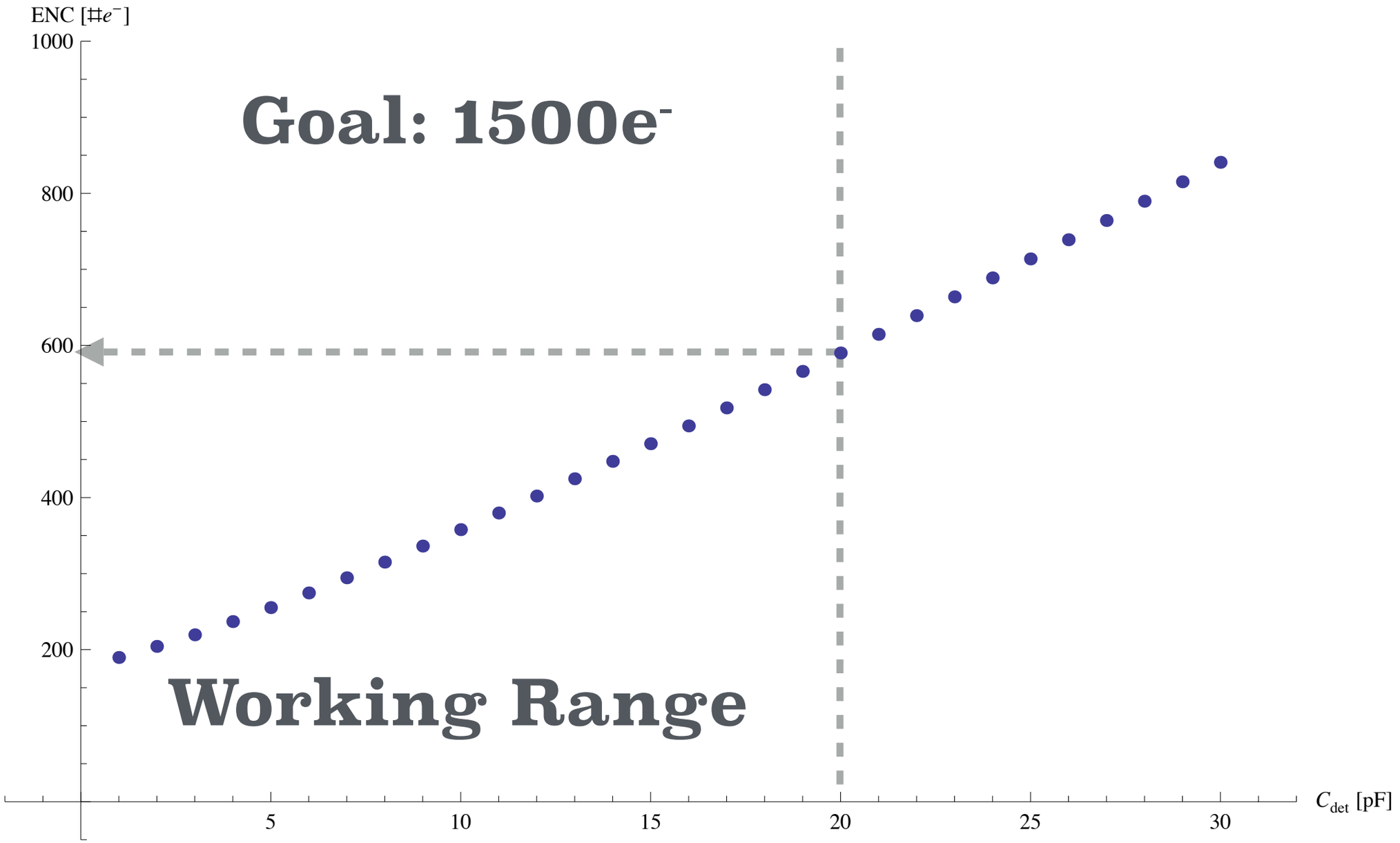


***nSconf: Configuration for the n-type Strips**

pSconf: ENC


ENC [#e^-]
1000
800
600
400
200
Goal: 1500e-
Working Range
5
10
15
20
25
30
C_{det} [pF]

nSconf: ENC


ENC [#e^-]
1000
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Goal: 1500e-
Working Range
5
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C_{det} [pF]

Back to December

- Layout completed with no PAD Ring
- GCTRL no DRC and LVS clean
- Post-integration and post-layout simulations started (FE + ATDC + TDC_CTRL)

- Estimation for **power consumption**

Estimation!

front-end	TDC	TDC ctrl.	global ctrl.	drivers	total
1 mW/ch	0.4 mW/ch	0.25 mW/ch	60 mW	4x 8.5 mW	**3.12 mW/ch**

André Goerres, December 2014 update

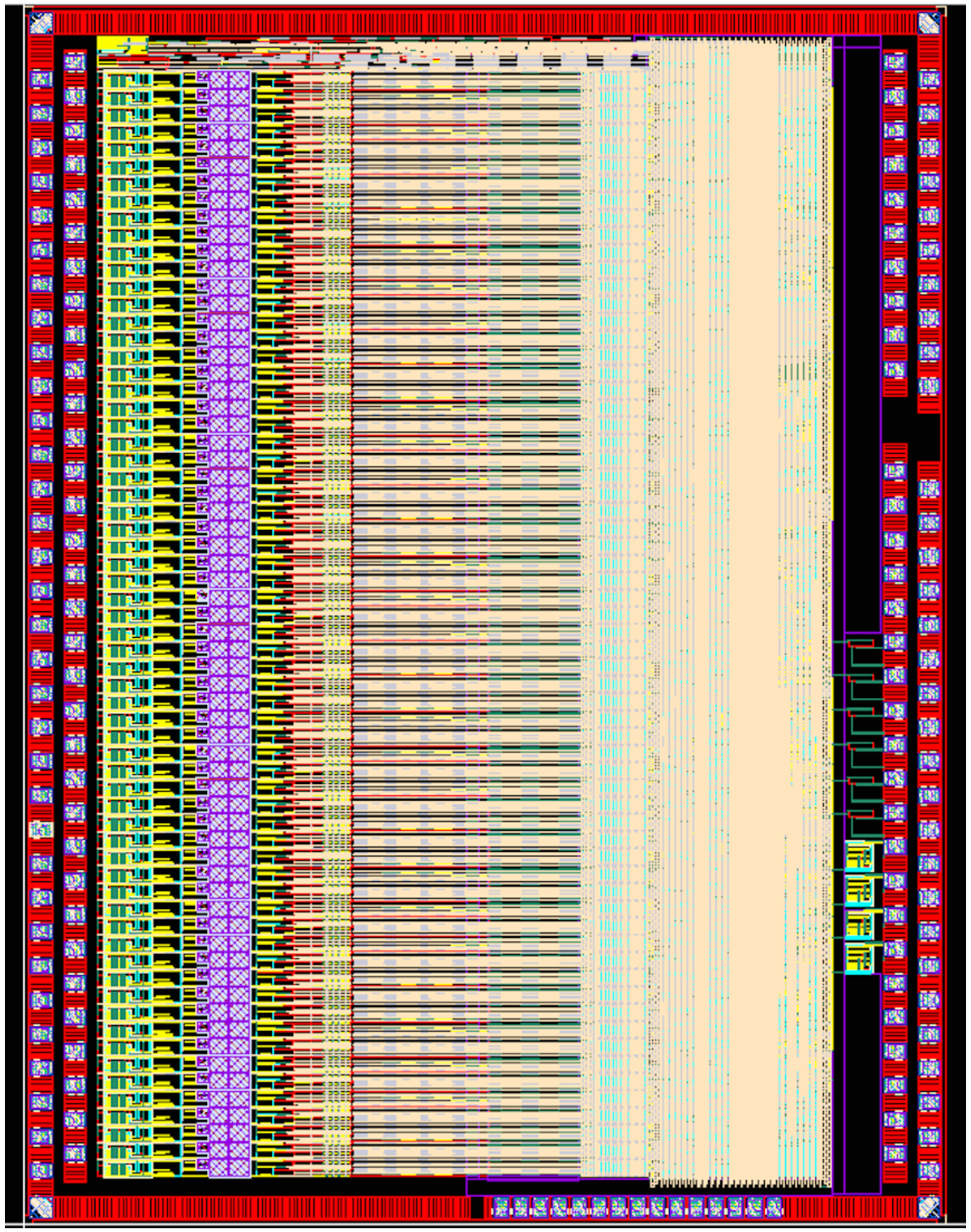
Updates

- Layout completed with no PAD Ring
- GCTRL no DRC and LVS clean
- Post-integration and post-layout simulations started (FE + ATDC + TDC_CTRL)

- PAD Ring DRC and LVS clean
- GCTRL DRC and LVS clean
- Simulations ongoing

Full Chip Layout

3.4mm



4.5mm

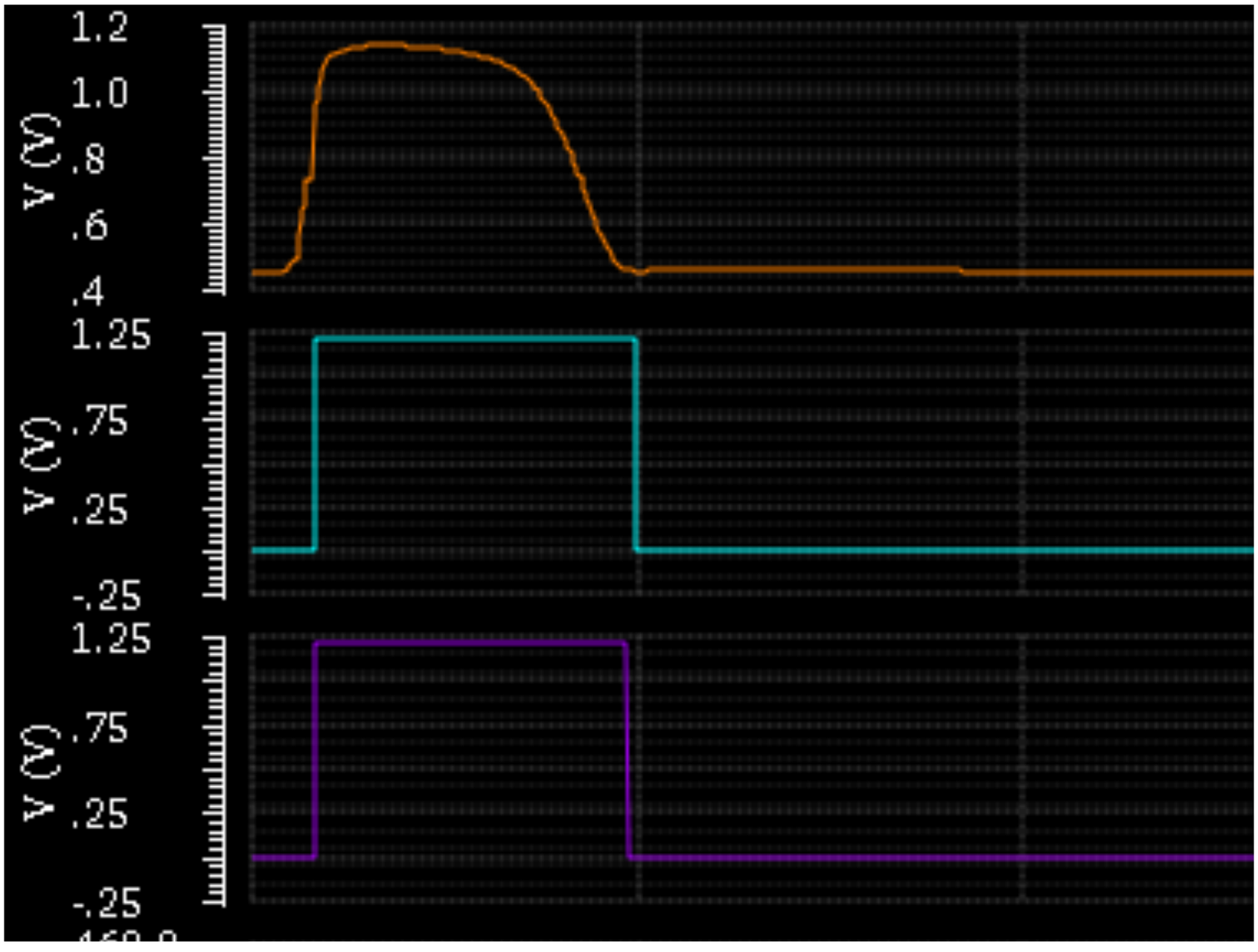
Simulations

Done

- 64 Channels + Bias (schematic)
- Full Analog Channel (post-layout)
- Antenna Check

Post-integration Simulations

1 Channel + Bias

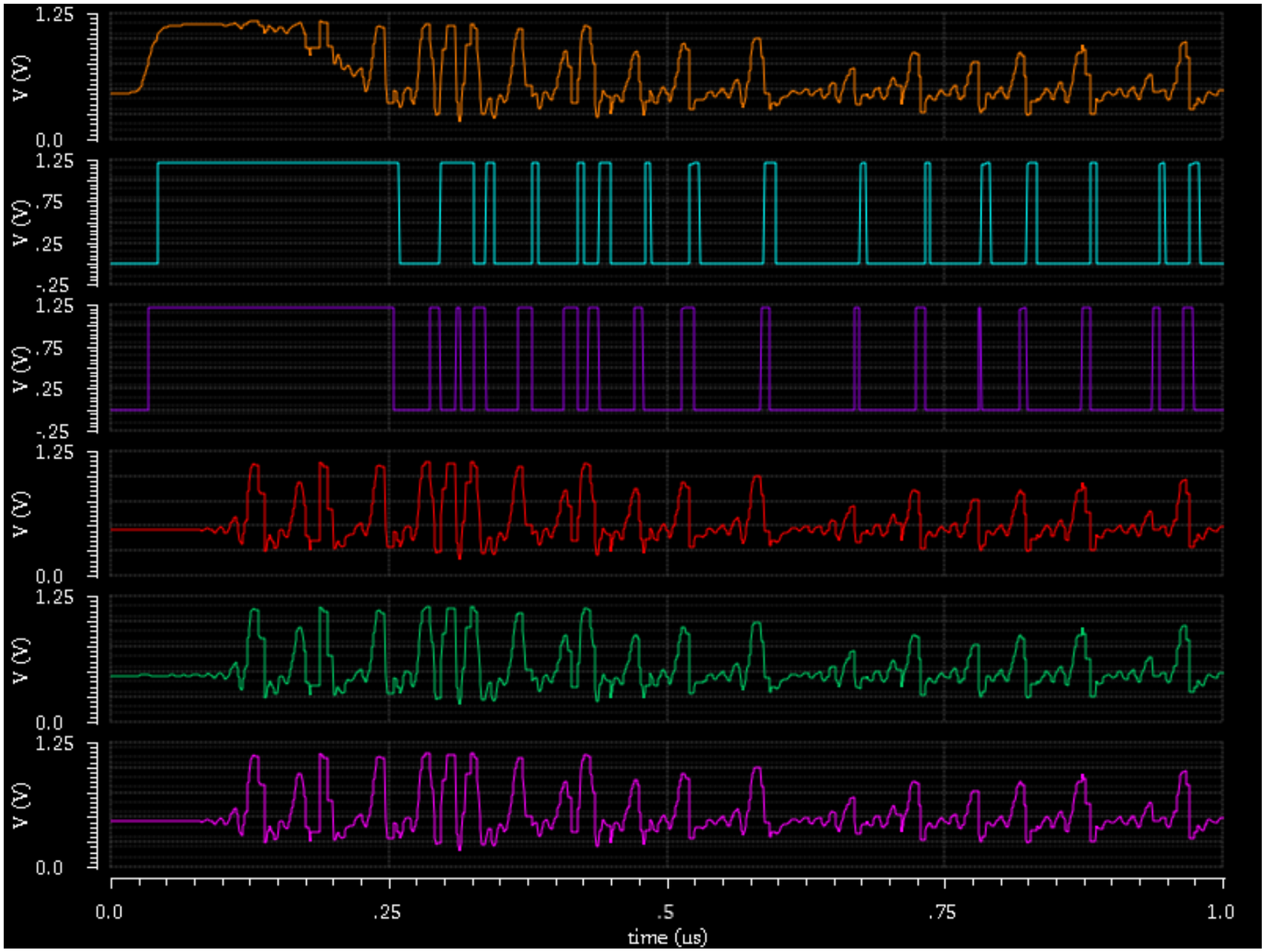


Q_{in} = 16fC

- 2 Channels ✔
- 4 Channels ✔
- 8 Channels ~
- 16 Channels ✘

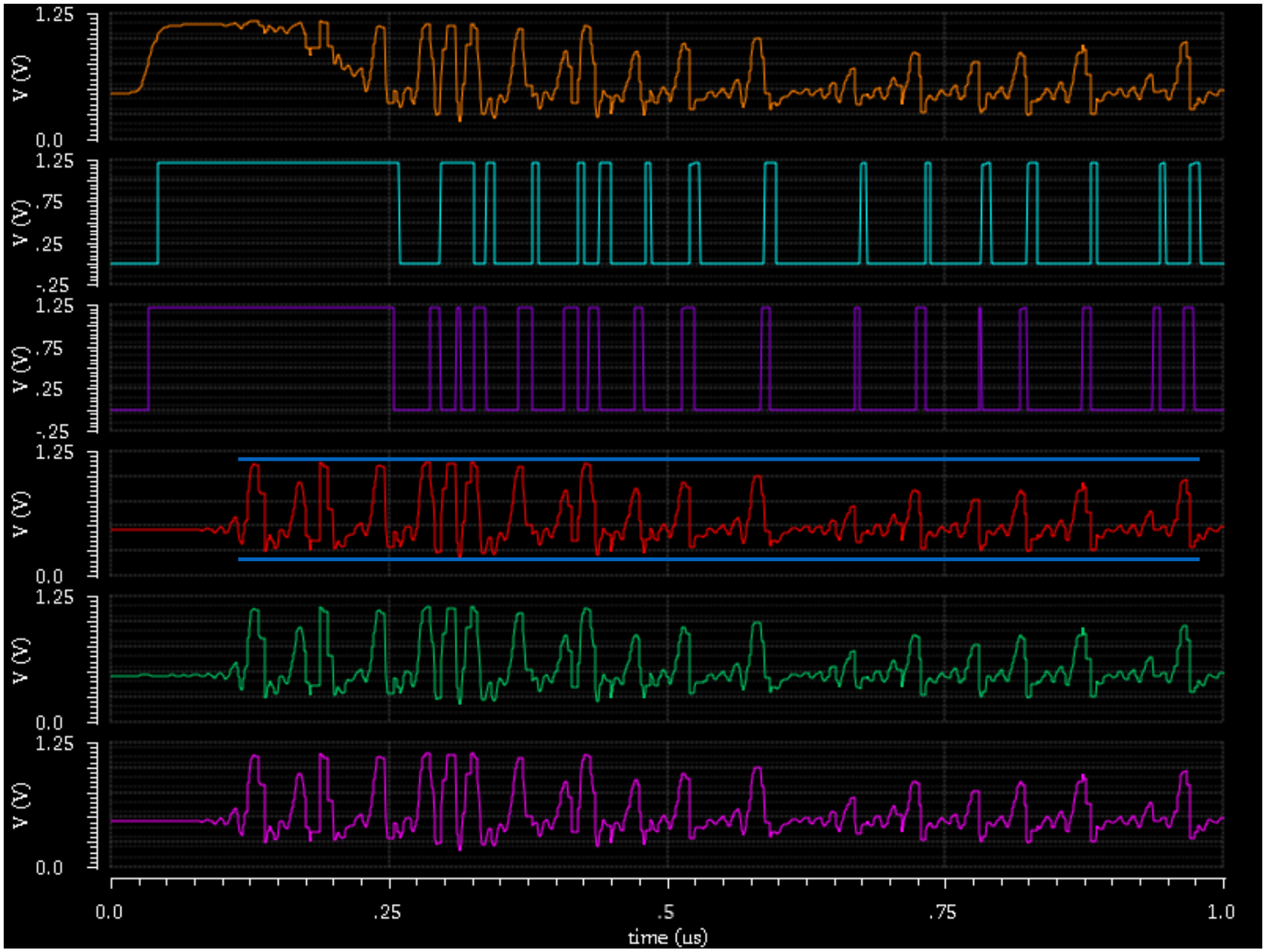
Results

16 Channels + Bias



Results

16 Channels + Bias



1.2V

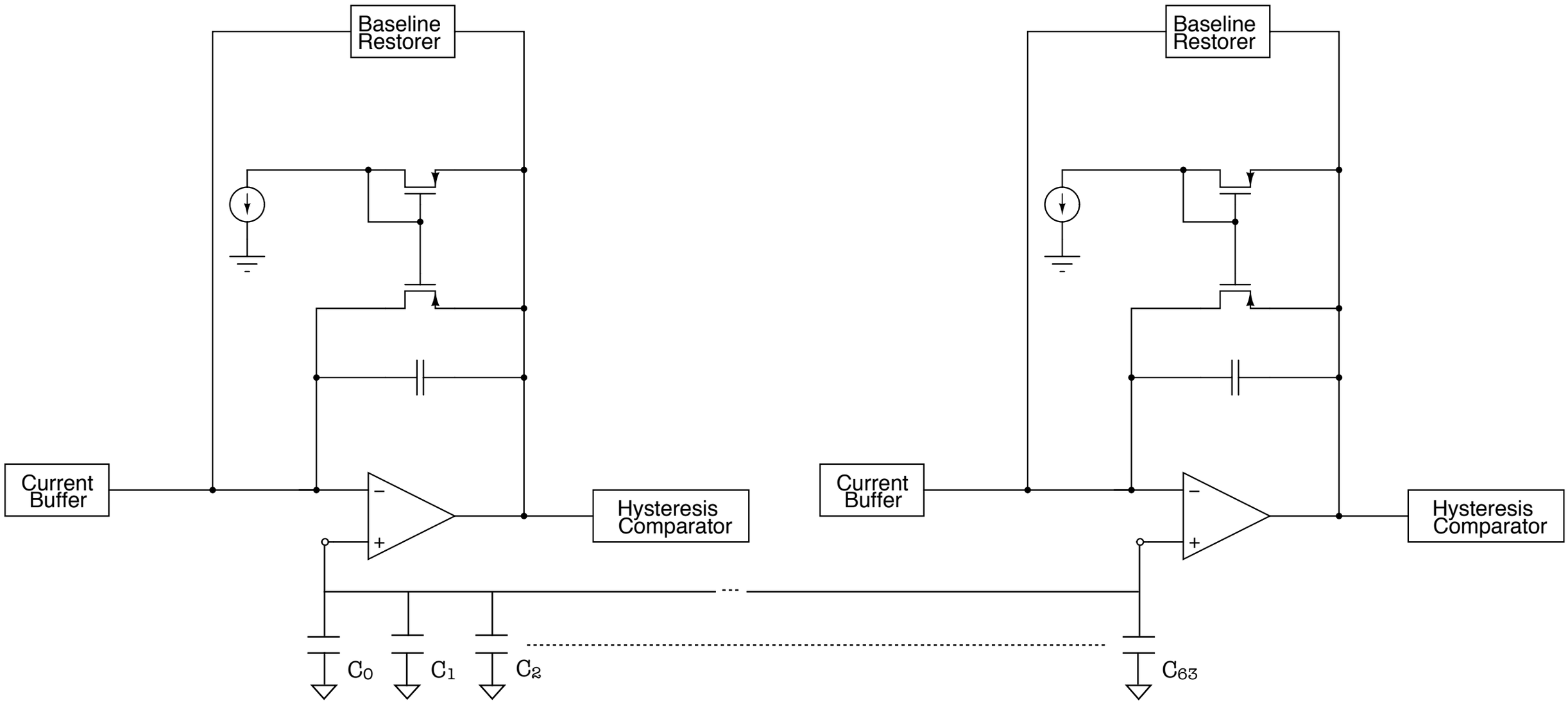
1.2V

1.2V

Issue detected

Channel 0

Channel 63



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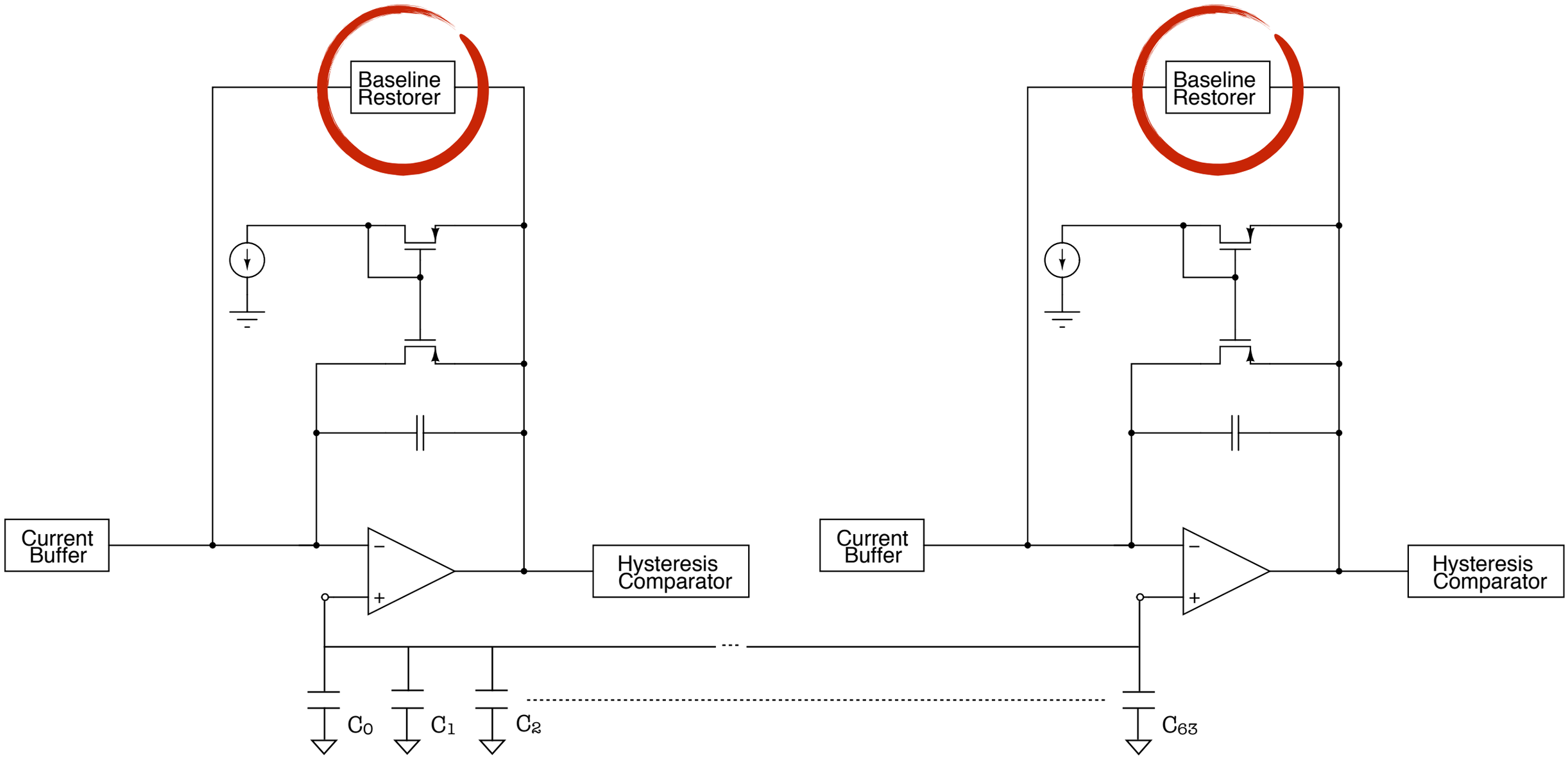

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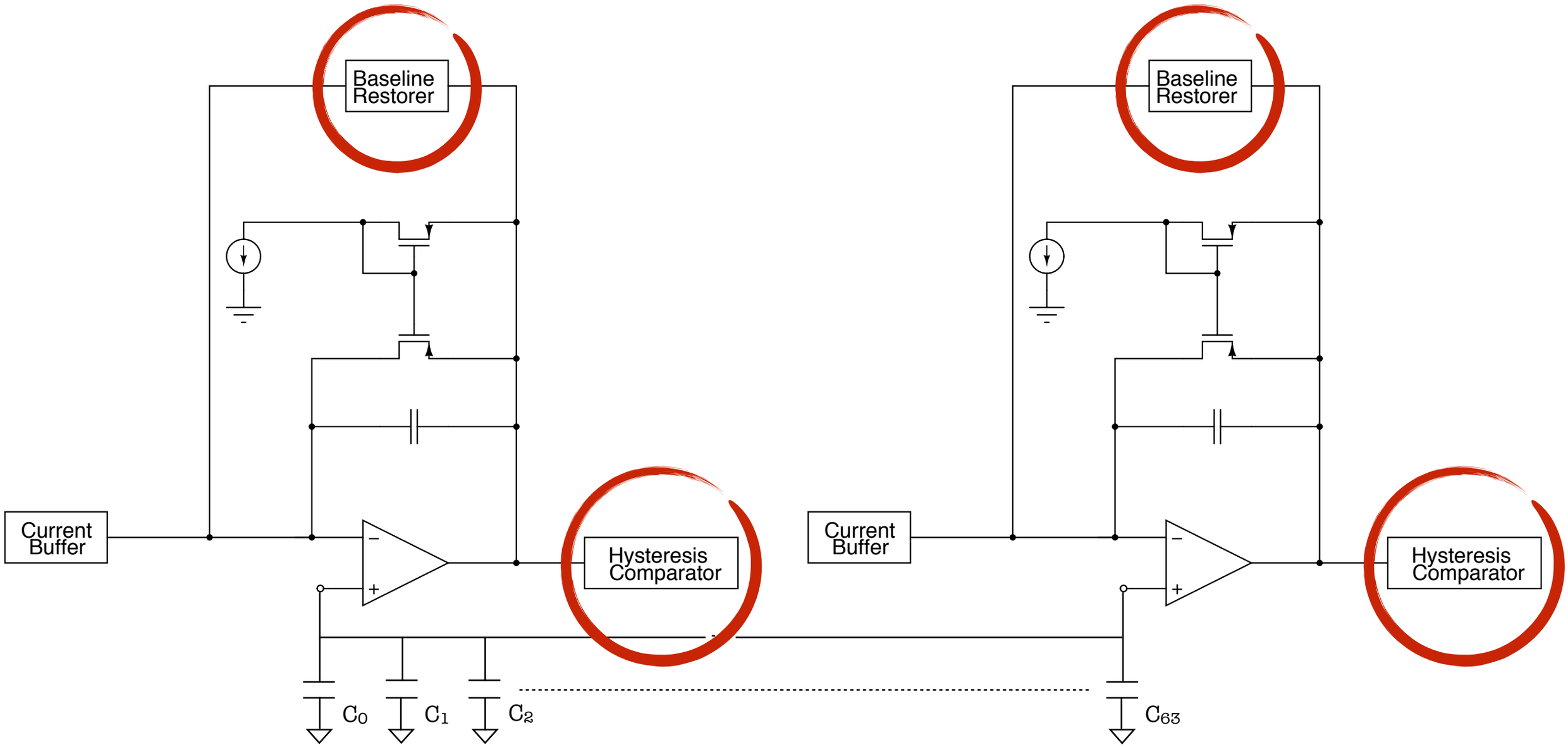
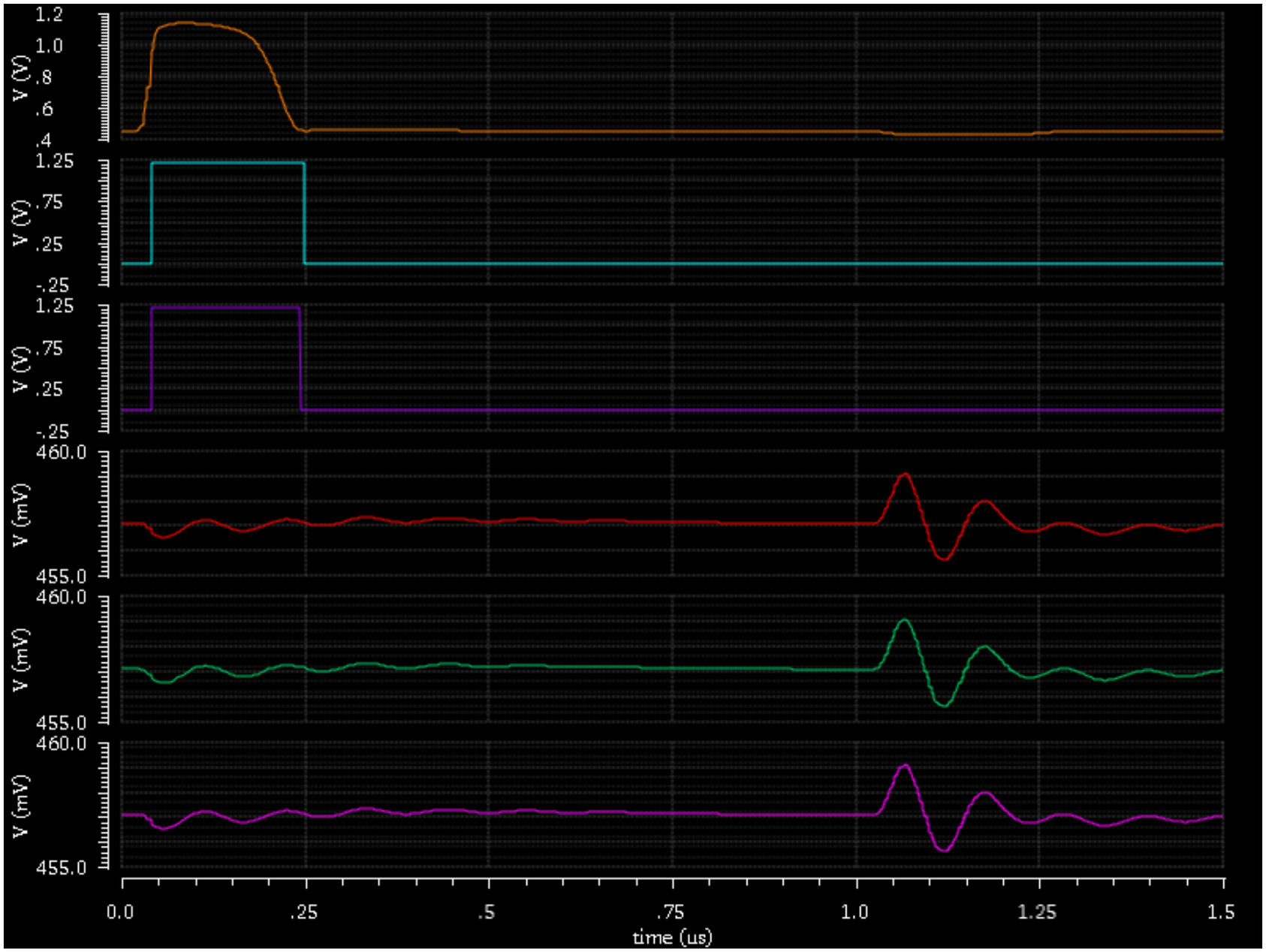


Results (post fixing)

64 Channels + Bias



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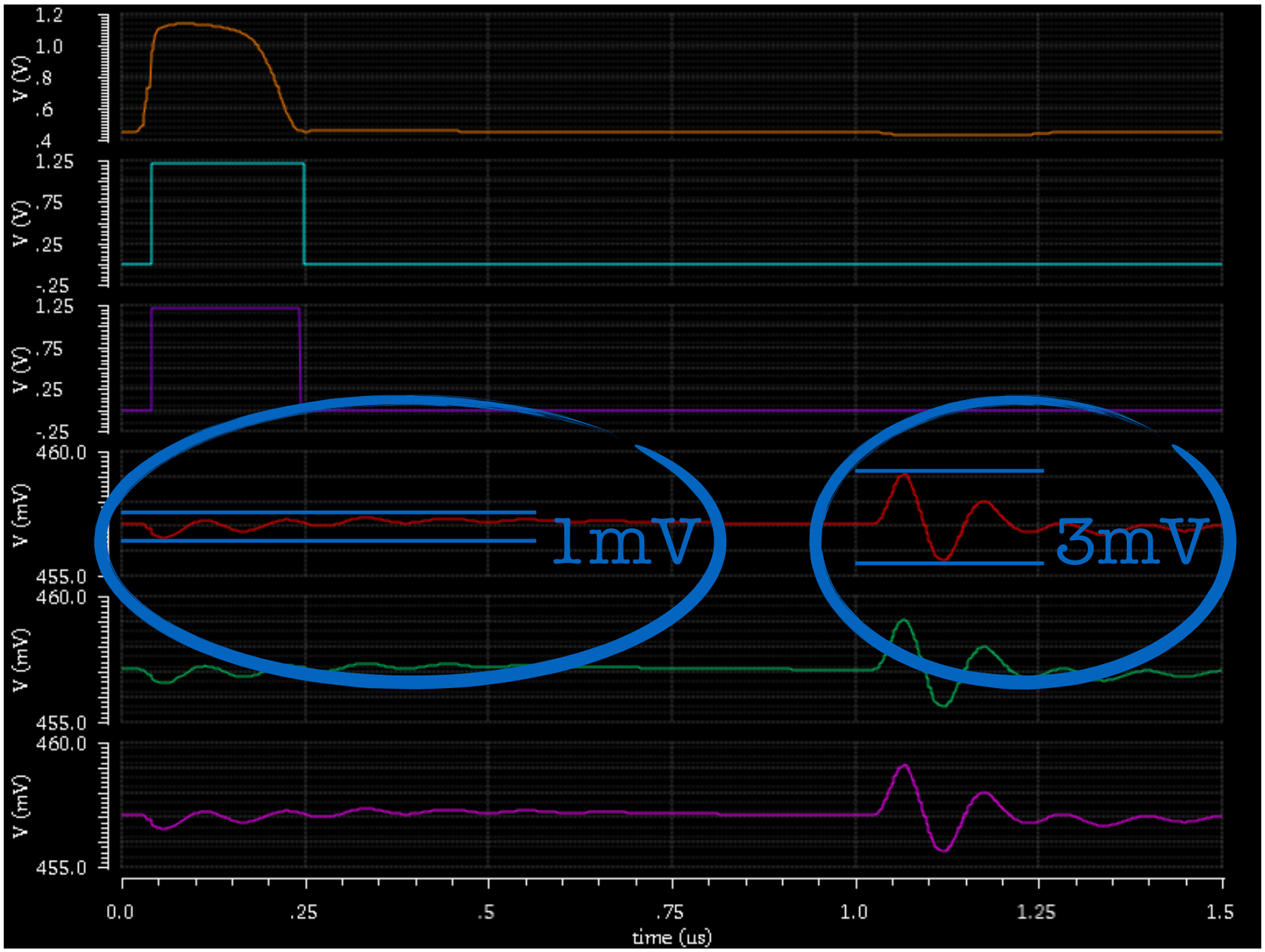


1.2V

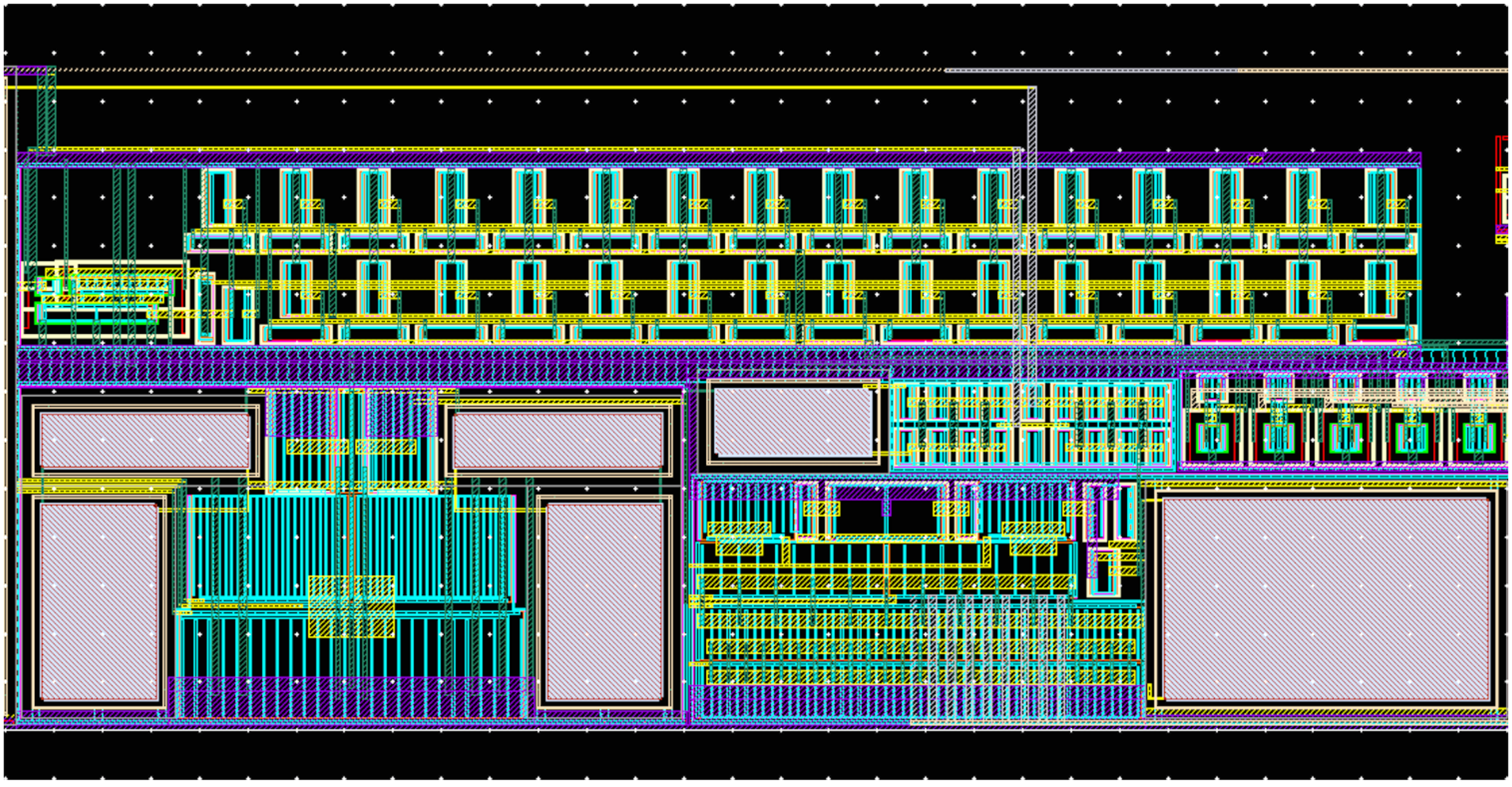
1.2V

Residual bias pickup

Cross-talk

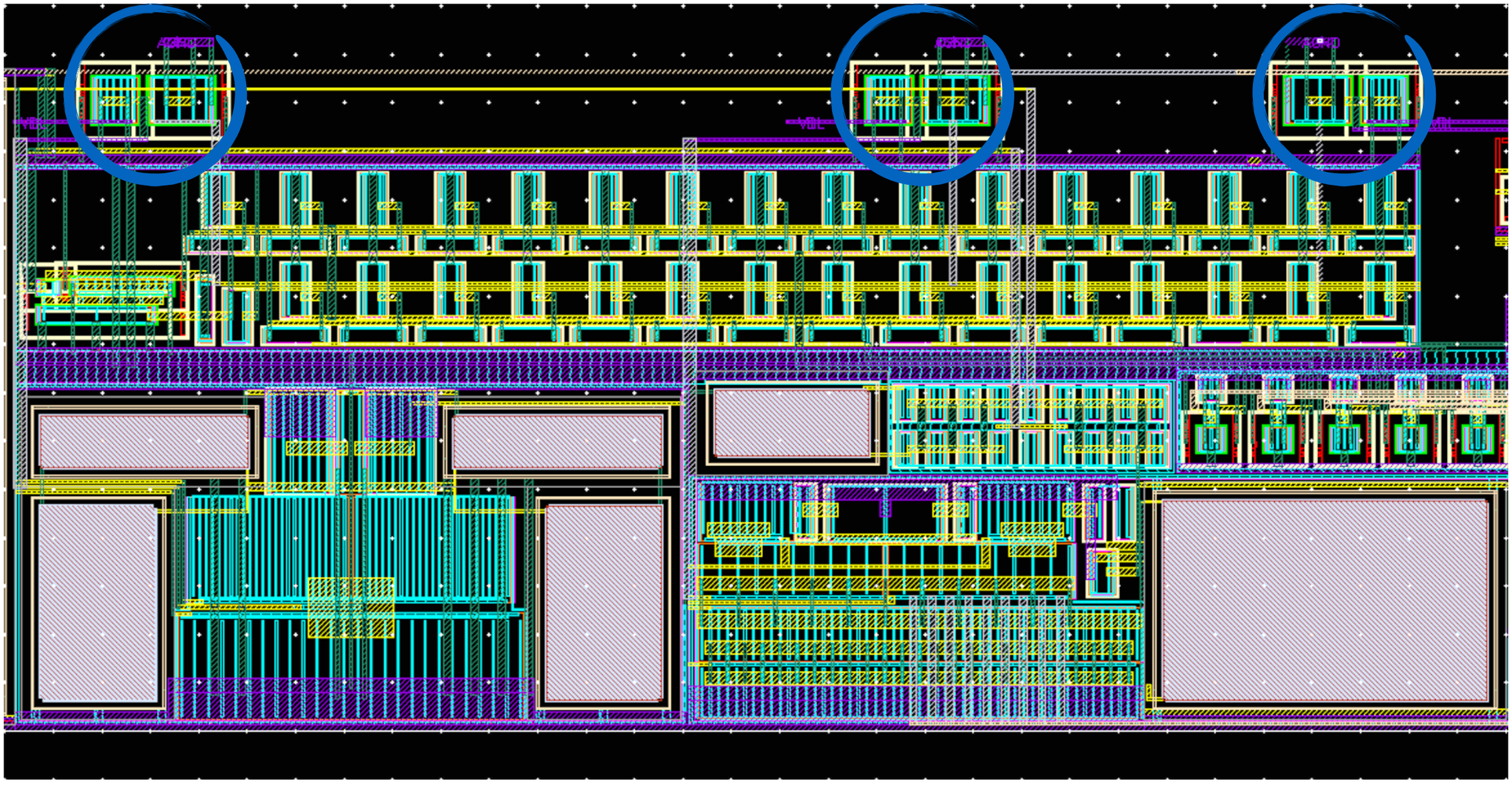
Fixing

Before



Fixing

After



Power consumption increased by 100μW

Simulations

Planned checks

- PAD Ring + 64 Analog Channels + Bias (schematic)
- PAD Ring + 64 Analog Channels + Bias + Power Grid (post-layout dc analysis)
- Further refinement on channels decoupling
- TDC conversion (schematic) [to verify what seen in September]

Perspectives

- Complete the fixing of the issues detected by post-integration simulations
- Implement the modifications into the layout
- Submit the project to the foundry on April 20th

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Special thanks to Angelo Rivetti and Manuel Rolo for the great help provided

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- Implement the modifications into the layout
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Thank You

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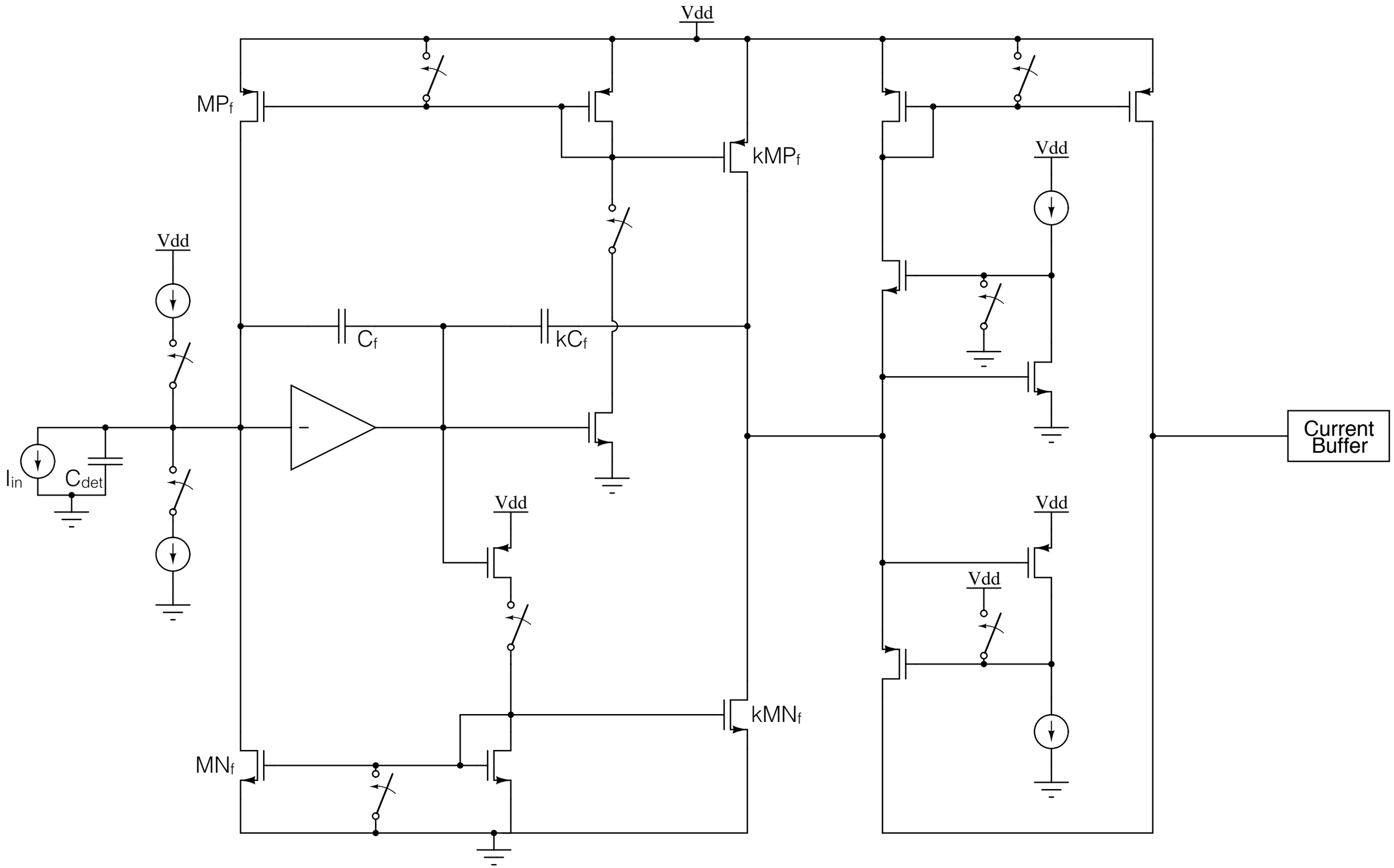
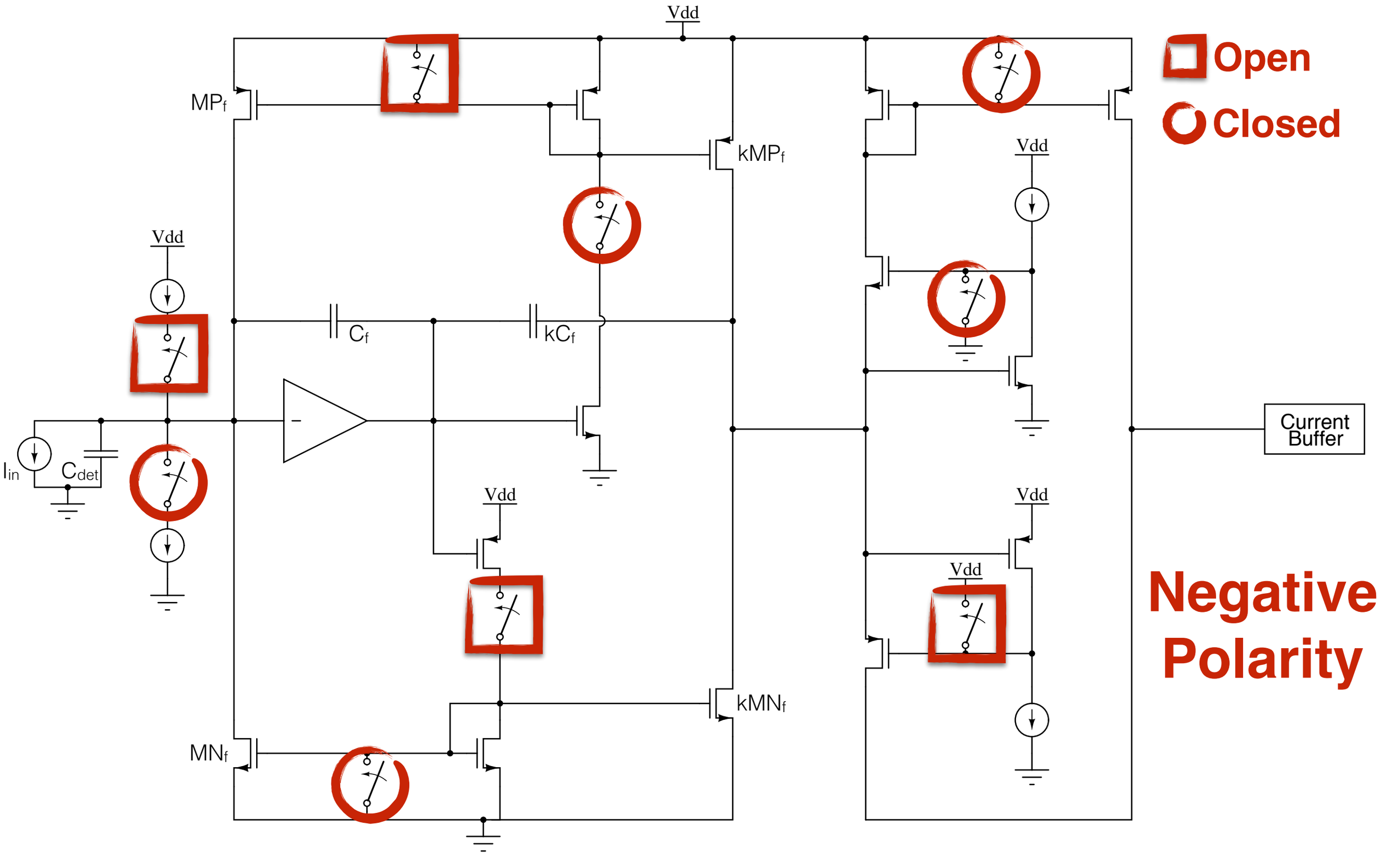
Backup Slides

Preamplifier



Preamplifier



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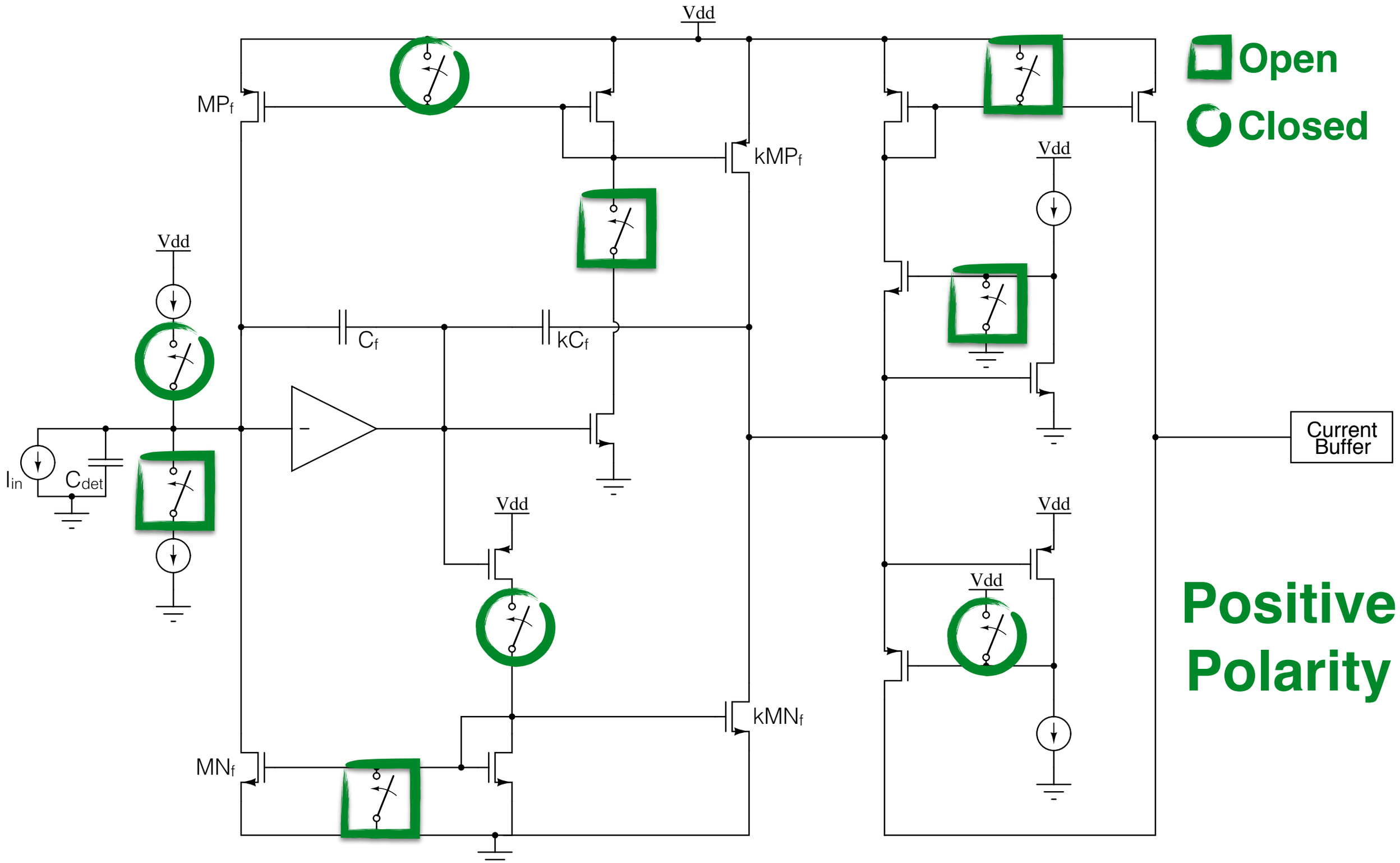
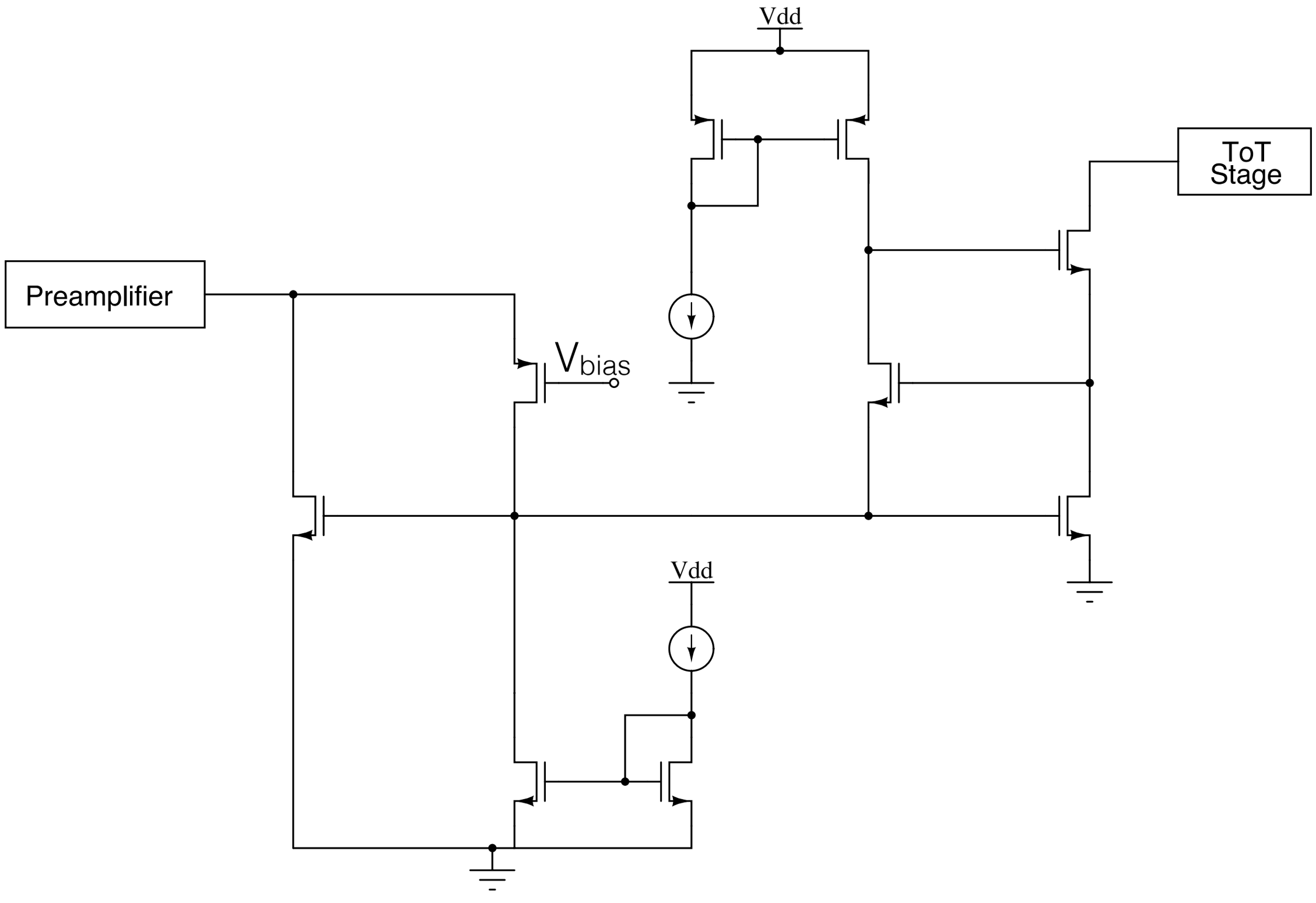
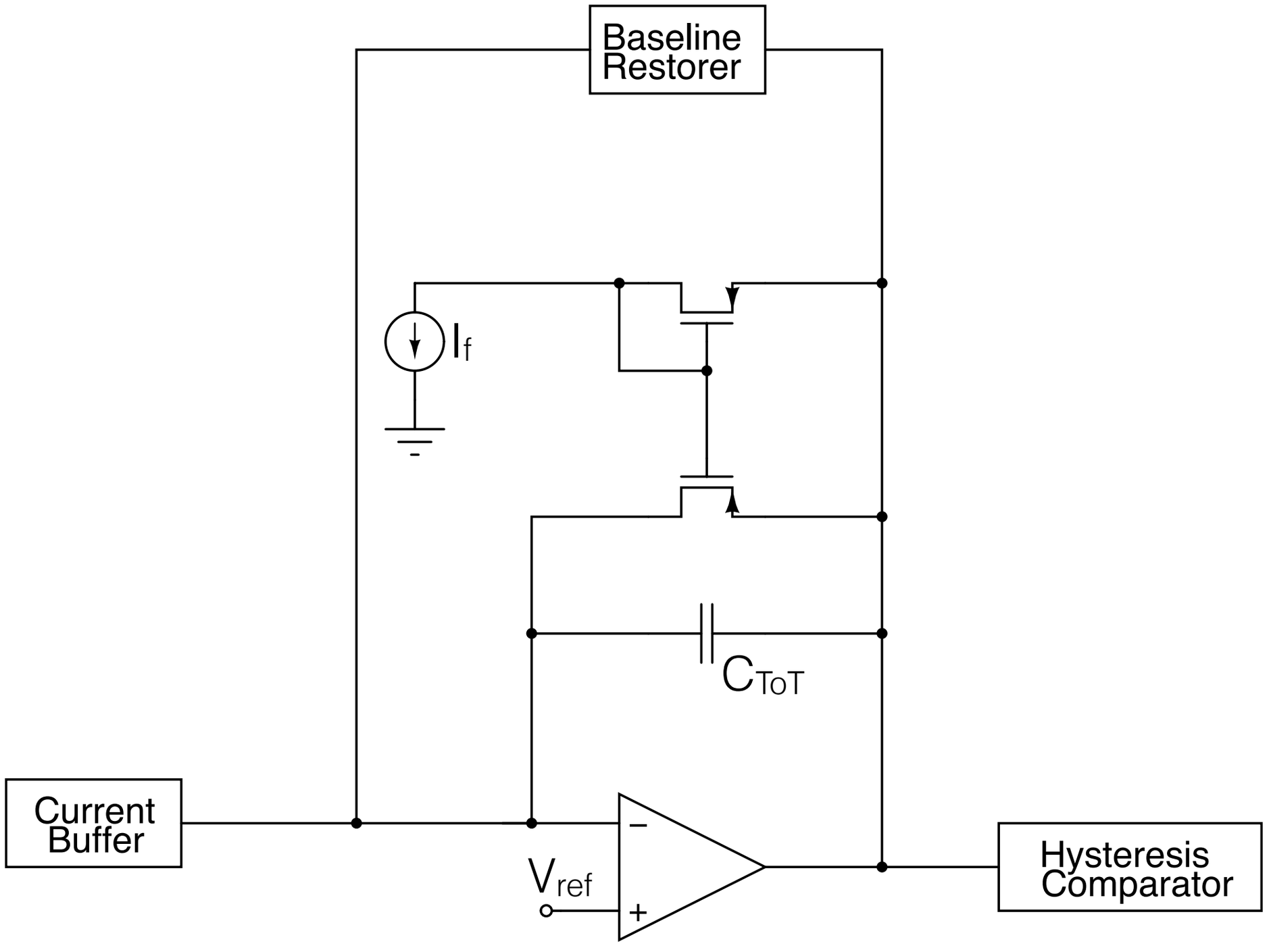


Current Buffer



ToT Stage


Baseline Restorer
I_f
C_{ToT}
Current Buffer
V_{ref}
−
+
Hysteresis Comparator