# Jülich Beam Test Results

# L. Zotti



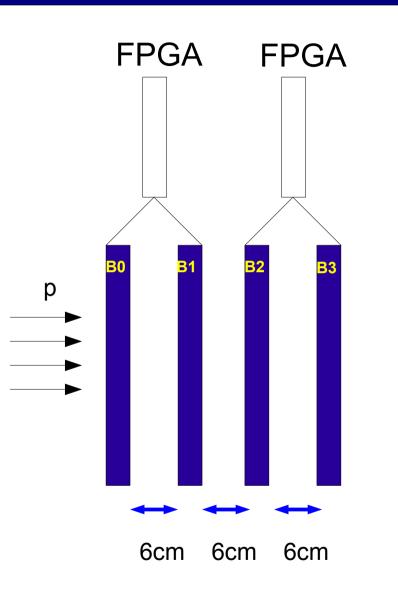


LII Collaboration Meeting, 16-20<sup>th</sup> March 2015

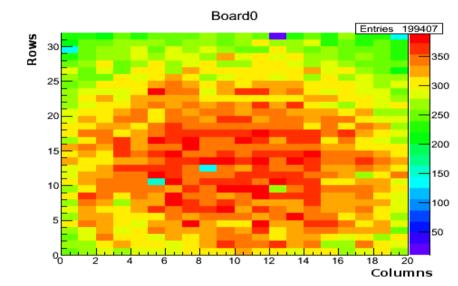
1

# Jülich Beam Test @ COSY (November2014)

p@2.9 Gev/c



- 4 Assemblies:
- Topix4
- Epitaxial Silicon Sensor (2x3.2 mm<sup>2</sup>)



- Clock Frequency Scan
- Theshold Scan
- Bias Scan
- Freeze Scan

LI Collaboration Meeting -December 2014

2

# Jülich Beam Test @ COSY DAQ & DATA FORMAT

Position

39:38

37:26

25:18

17:6

5:0

# bits

2

12

8

12

6

Data

Header (01 for FH)

Chip address

Frame counter

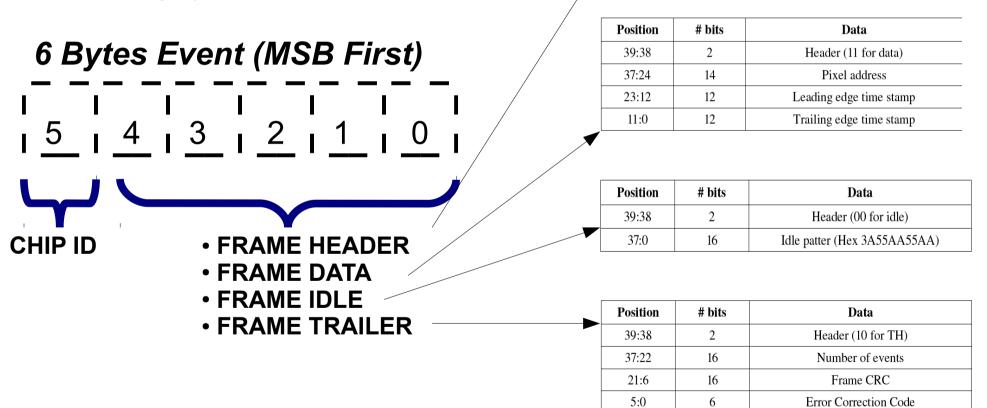
Not used (set to Hex 5A5)

Error Correction Code

### DAQ - LabView (R.Wheadon)

### 8 Bytes Long Packet Header with

- Packet Numbers
- # Following Bytes



**Dummy Events:** LE or TE = 2730 or 2729

# Jülich Beam Test @ COSY FACING TIMESTAMP....

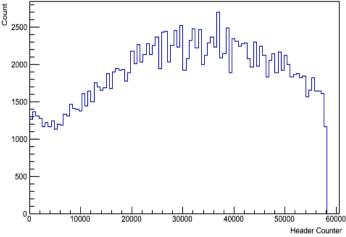
TIMESTAMP = 8bit (FRAME\_COUNTER) + 12bit (LEADING\_EDGE) .....but @ 50 MHz: 20 ms  $\rightarrow$  with a spill of ~20s: 1000 reset @ 160 MHz: 6.25 ms  $\rightarrow$  with a spill of ~20s: 3200 reset

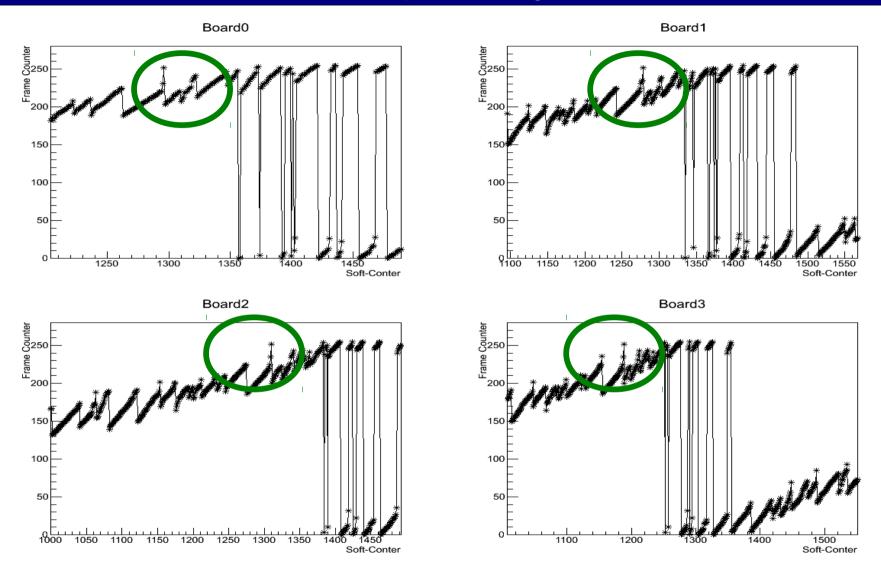
The standard timestamp matching procedure is not able at the moment to find time match....

• An additional 7bit counter was added, but has not been used in the timestamp matching procedure for alignment dubts...

• A software counter, labeling the header frame, was added but since empty frame are filtered out, no time reference is present at the moment...

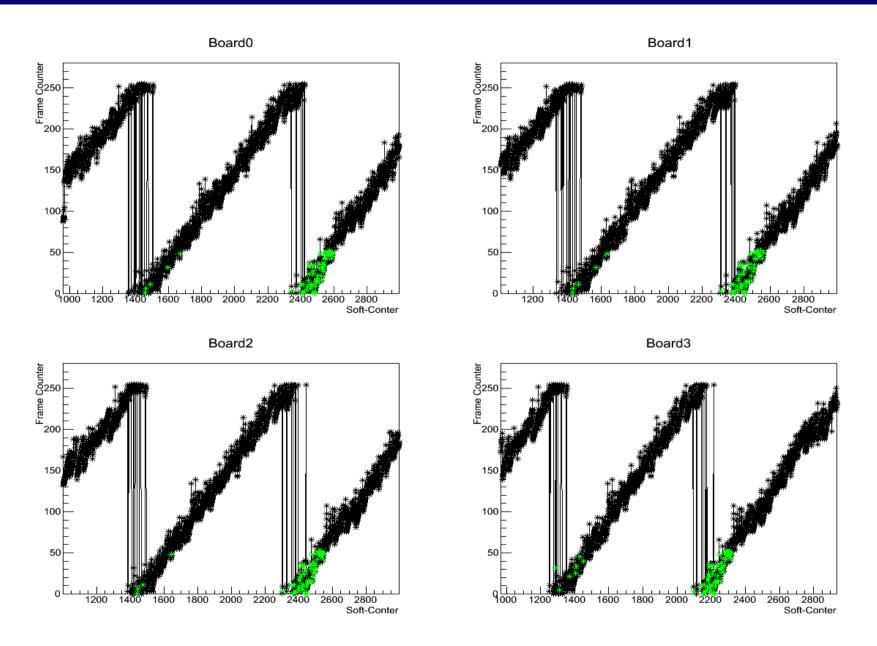
- Debug analysis of the acquisition performance
- Comparison of the frame counter behaviour





A new code was developed to find match between data set with the same frame counter taking into account disalignment between header counter

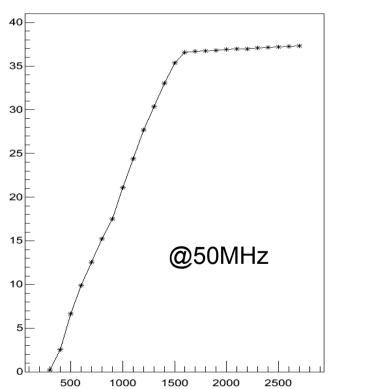
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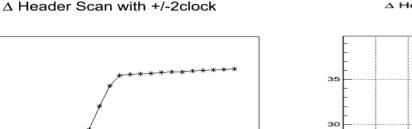


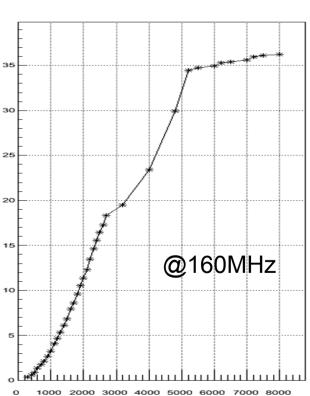
6

The new timestamp matching procedure should take into account different possible disalignment between boards:

- Clock Range: clock synchronization, comparator delay
- Header Counter disalignment







∆ Header Scan with +/-7clock

#### @50MHz

- $\rightarrow$  Track Selection +/- 2 clock cycle (40ns)
- $\rightarrow$  Header Delta 1600
- $\rightarrow$  Cluster Finding +/- 2\*5 clock cycle (200ns)

#### @160MHz

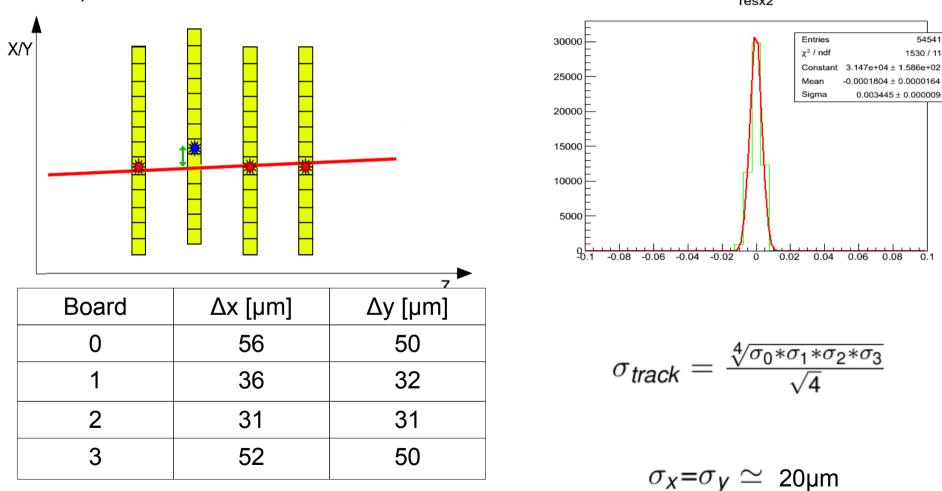
- $\rightarrow$  Track Selection +/- 7 clock cycle (~43ns)
- $\rightarrow$  Header Delta 5200
- $\rightarrow$  Cluster Finding +/- 7\*5 clock cycle (200ns)



# Jülich Beam Test @ COSY Alignment

Alignment performed on the 50MHz data set.

Residual method: with one fixed board (either B3 and B0 have been evaluated giving similar results) resx2



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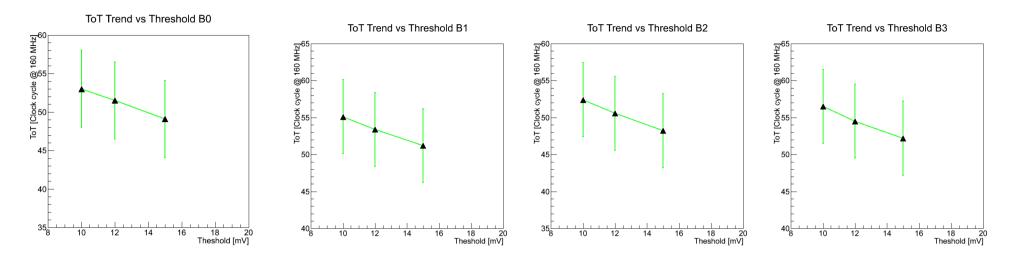
54541

1530 / 11

0.08

0.1

# Jülich Beam Test @ COSY Threshold Scan



#### Analog Gain [mV/fC]

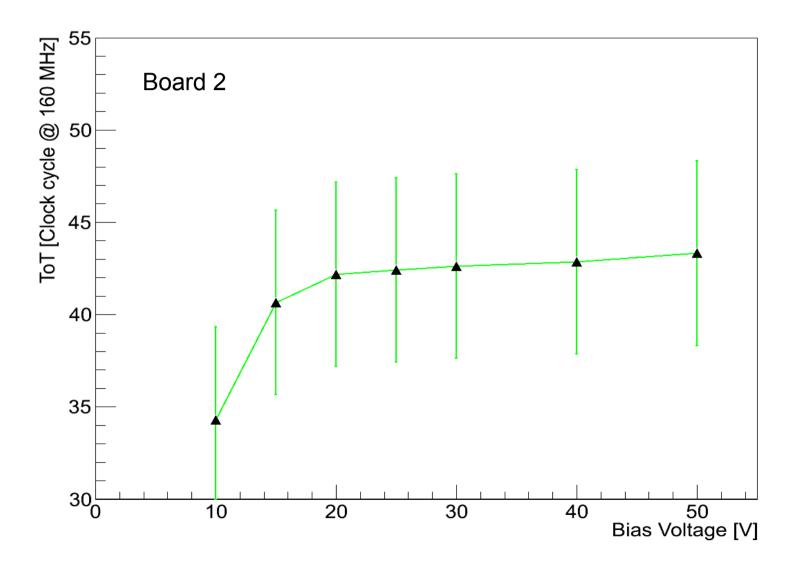
#### by Olave Jonhatan

B0			B1			B2			B3		
79 ±	10	88	±	11	91	±	11	85	±	15	

∨th	Voltage Threshold [e-]								
[m∨]	B0	I B1	I B2	B3					
10 12 15 20 22	$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$					

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# Jülich Beam Test @ COSY Bias Scan



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# Conclusions

# DONE:

 $\rightarrow$  new timestamp matching procedure developed to face the absence of time reference

- $\rightarrow$  offline alignment performed
- $\rightarrow$  analysis of different scan data sets

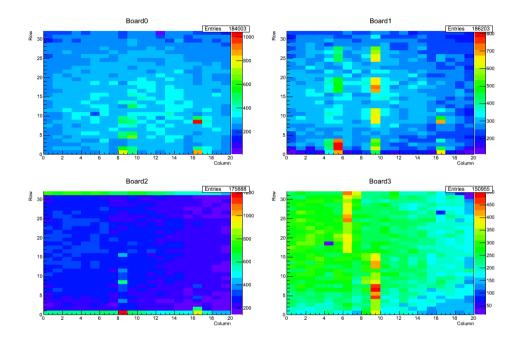
WORK IN PROGRESS:

- $\rightarrow$  Efficiency evaluation as a function of Bias and Threshold Scan
- $\rightarrow$  Evalutation of the ToT in term of electrons

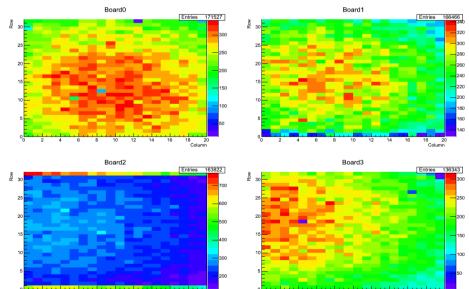


# **BACKUP SLIDES**

# Julich Beam Test @ COSY



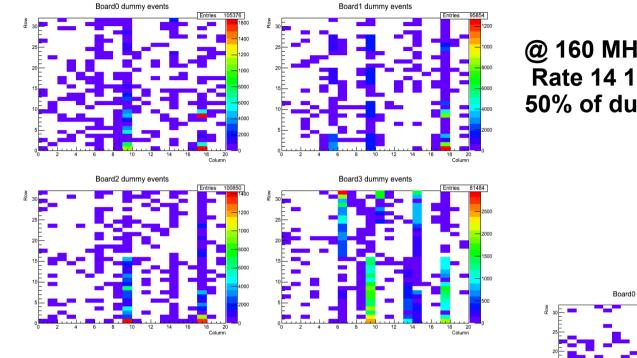
@ 160 MHz
Rate 14 10<sup>3</sup> (~22hit per pixel/s)
50% of dummy



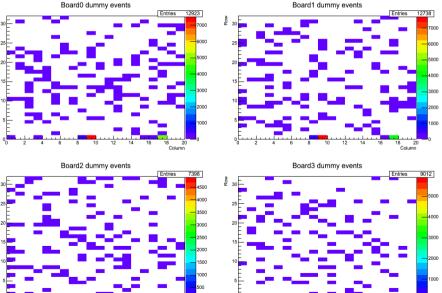
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@ 50 MHz
Rate 9 10<sup>3</sup> (~14hit per pixel/s)
8% of dummy

### Julich Beam Test @ COSY DUMMY EVENTS



@ 160 MHz
Rate 14 10<sup>3</sup> (~22hit per pixel/s)
50% of dummy



@ 50 MHz
Rate 9 10<sup>3</sup> (~14hit per pixel/s)
8% of dummy

