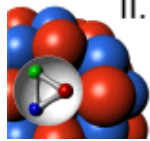
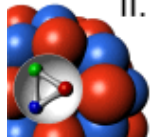


DCDC-Converters Tests and Options

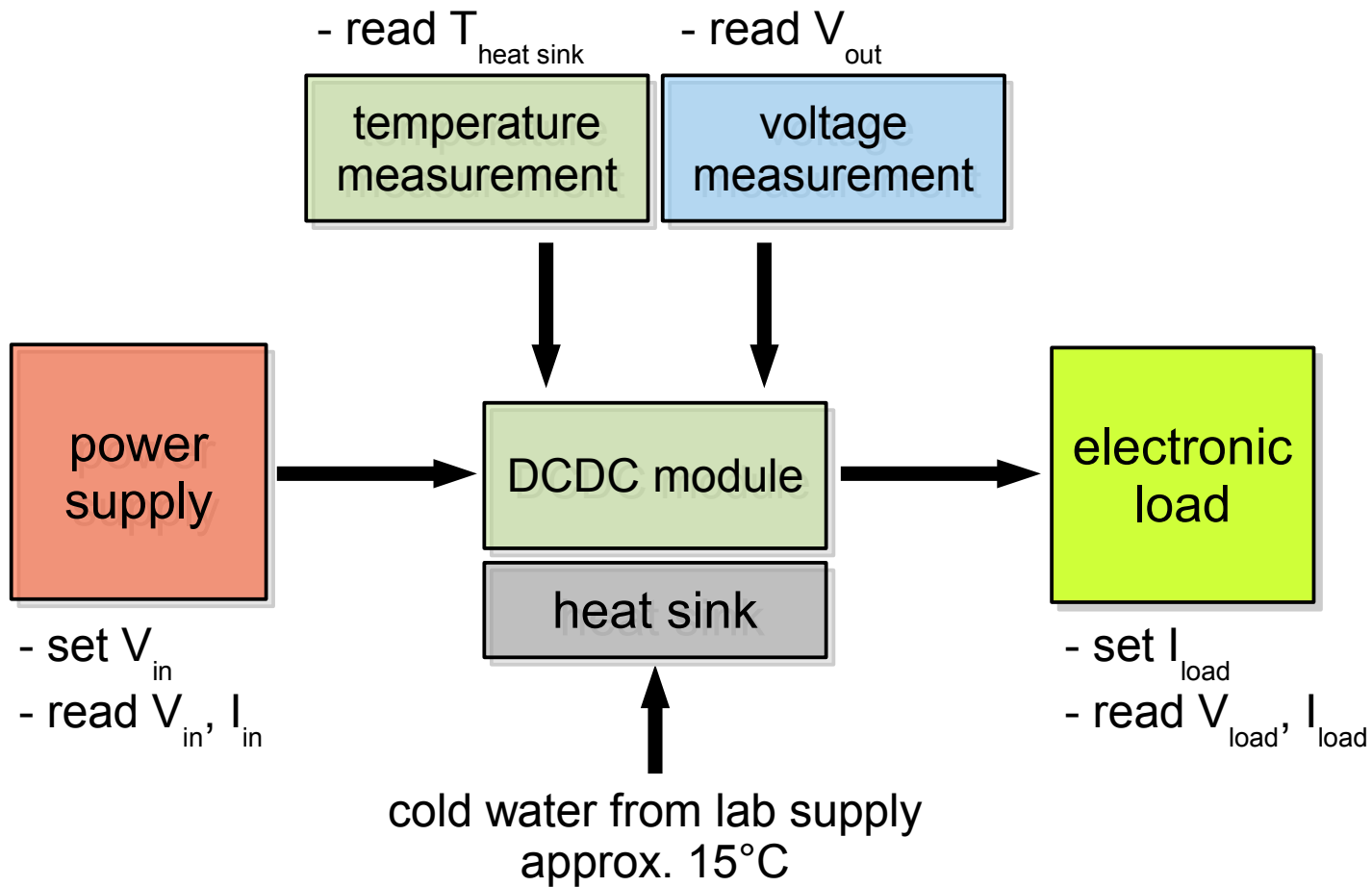


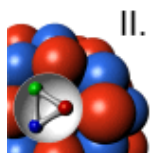
Test Bench

- Testing bench for DCDC regulator modules
- "Modular" (so far FEASTMP, soon PIX_V13)
 - 4 instruments connected to PC via RS232
 - power supply (Hameg HM8143)
 - electric load (Gossen 32EL 150R30)
 - Multimeter – Voltage (Tektronix DMM4020)
 - Multimeter – Temperature (Keithley 2000)
 - Module connected to water-cooled heat sink
 - approx. 15°C
 - Controlled via GUI
 - set and read instruments manually
 - automated scans

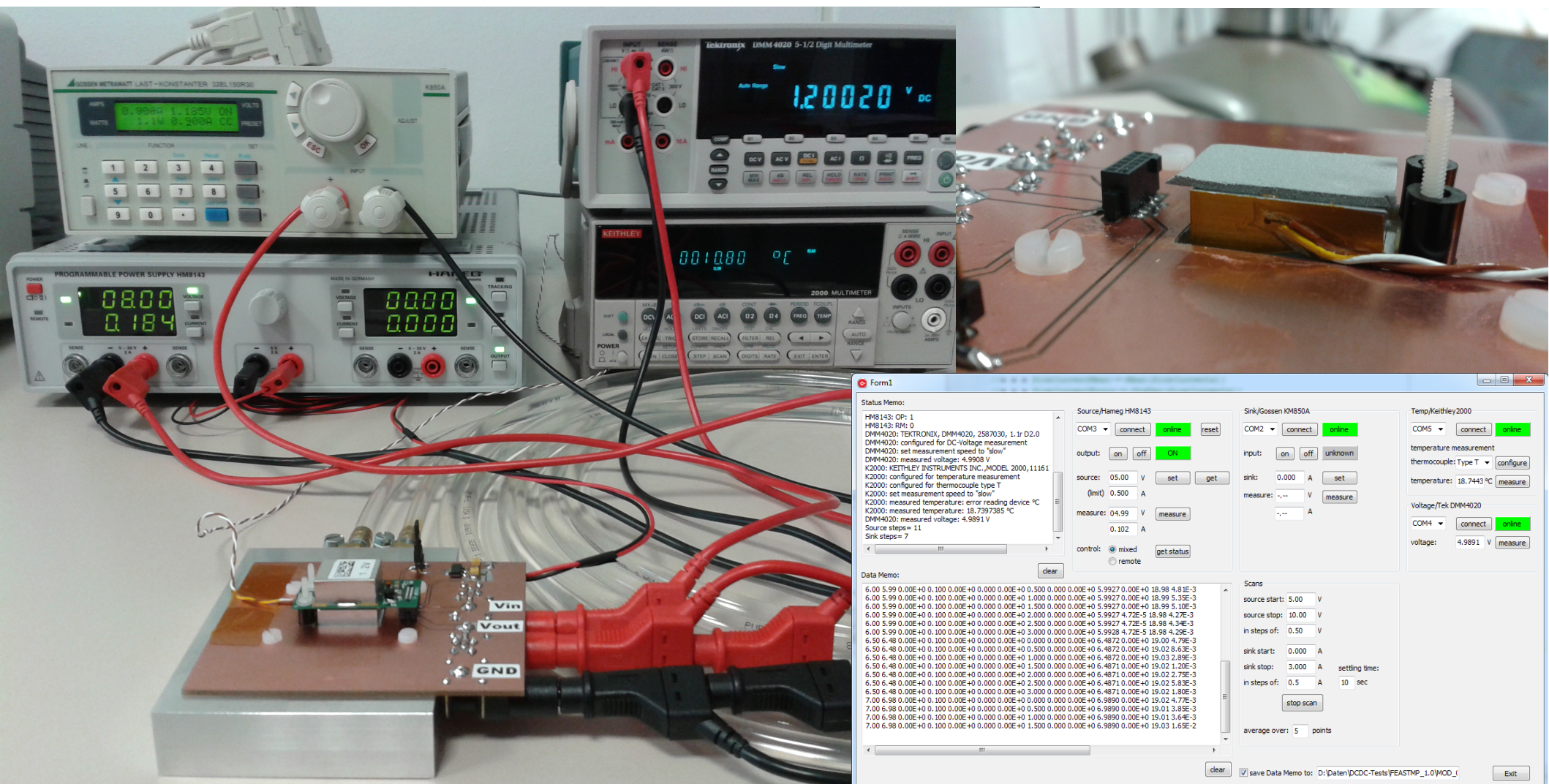


Test Bench - Setup





Test Bench - Setup



Form1

Status Memo:

HMB143: OP: 1
HMB143: RM: 0
DMM4020: TEKTRONIX, DMM4020, 2587030, 1.1r D2.0
DMM4020: configured for DC-voltage measurement
DMM4020: set measurement speed to "slow"
DMM4020: measured voltage: 4.9908 V
K2000: KEITHLEY INSTRUMENTS INC., MODEL 2000, 11161
K2000: configured for temperature measurement
K2000: configured for thermocouple type T
K2000: set measurement speed to "slow"
K2000: measured temperature: error reading device °C
DMM4020: measured voltage: 4.9891 V
Source steps= 11
Sink steps= 7

Source/Hameg HMB143

COM3

output:

source: 05.00 V

(limit) 0.500 A

measure: 04.99 V

0.102 A

control: mixed remote

Sink/Gossen KM850A

COM2

input:

sink: 0.000 A

measure: --- V

--- A

Temp/Keithley 2000

COM5

temperature measurement

thermocouple: Type T

temperature: 18.7443 °C

Voltage/Tek DMM4020

COM4

voltage: 4.9891 V

Scans

source start: 5.00 V

source stop: 10.00 V

in steps of: 0.50 V

sink start: 0.000 A

sink stop: 3.000 A setting time: 10 sec

in steps of: 0.5 A

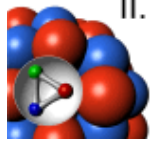
average over: 5 points

save Data Memo to: D:\Daten\DCDC-Tests\FEASTMP_1.0\WOD\

Data Memo:

```

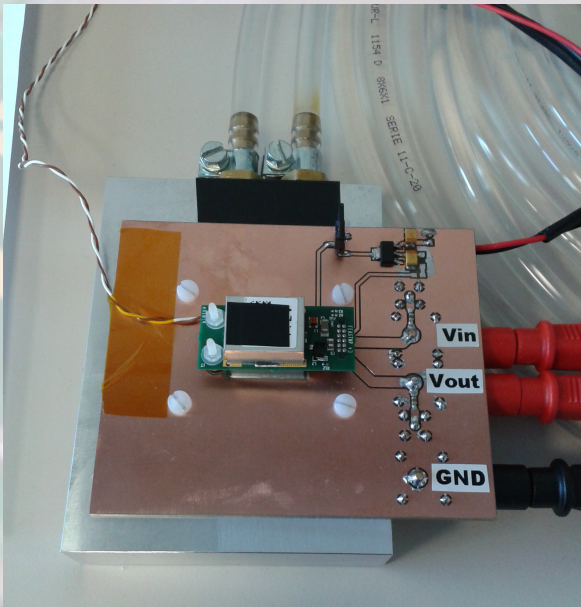
6.00 5.99 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 0.500 0.000 0.00E+0 5.9927 0.00E+0 18.99 4.81E-3
6.00 5.99 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 1.000 0.000 0.00E+0 5.9927 0.00E+0 18.99 5.35E-3
6.00 5.99 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 1.500 0.000 0.00E+0 5.9927 0.00E+0 18.99 5.10E-3
6.00 5.99 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 2.000 0.000 0.00E+0 5.9927 4.72E-5 18.98 4.27E-3
6.00 5.99 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 2.500 0.000 0.00E+0 5.9927 4.72E-5 18.98 4.34E-3
6.00 5.99 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 3.000 0.000 0.00E+0 5.9928 4.72E-5 18.98 4.29E-3
6.50 6.48 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 0.500 0.000 0.00E+0 6.4872 0.00E+0 19.02 6.43E-3
6.50 6.48 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 1.000 0.000 0.00E+0 6.4872 0.00E+0 19.03 2.89E-3
6.50 6.48 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 1.500 0.000 0.00E+0 6.4871 0.00E+0 19.02 1.20E-3
6.50 6.48 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 2.000 0.000 0.00E+0 6.4871 0.00E+0 19.02 2.75E-3
6.50 6.48 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 2.500 0.000 0.00E+0 6.4871 0.00E+0 19.02 5.83E-3
6.50 6.48 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 3.000 0.000 0.00E+0 6.4871 0.00E+0 19.02 1.80E-3
7.00 6.98 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 0.000 0.000 0.00E+0 6.9890 0.00E+0 19.02 4.77E-3
7.00 6.98 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 0.500 0.000 0.00E+0 6.9890 0.00E+0 19.01 3.85E-3
7.00 6.98 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 1.000 0.000 0.00E+0 6.9890 0.00E+0 19.01 3.64E-3
7.00 6.98 0.00E+0 0.100 0.00E+0 0.000 0.00E+0 1.500 0.000 0.00E+0 6.9890 0.00E+0 19.03 1.65E-2
    
```

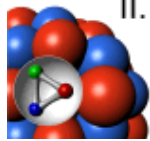


Test Bench - Results

- MOD_00233_1V2
- $T_{amb} \approx 21.5^{\circ}\text{C}$
- $T_{heat\ sink} \approx 15.5^{\circ}\text{C}$
- $Q \approx 1\ \text{l/min}$

V_{in} / V	I_{in} / A	V_{out} / V	I_{out} / A	$T_{shield} / ^{\circ}\text{C}$	Efficiency/%
8.0	0.203	1.198	1.0	17.7	73.8
8.0	0.403	1.180	2.0	20.2	73.2
8.0	0.634	1.162	3.0	23.5	68.7
8.0	0.902	1.144	4.0	28.2	63.4
8.0	1.218	1.127	5.0	34.9	57.8

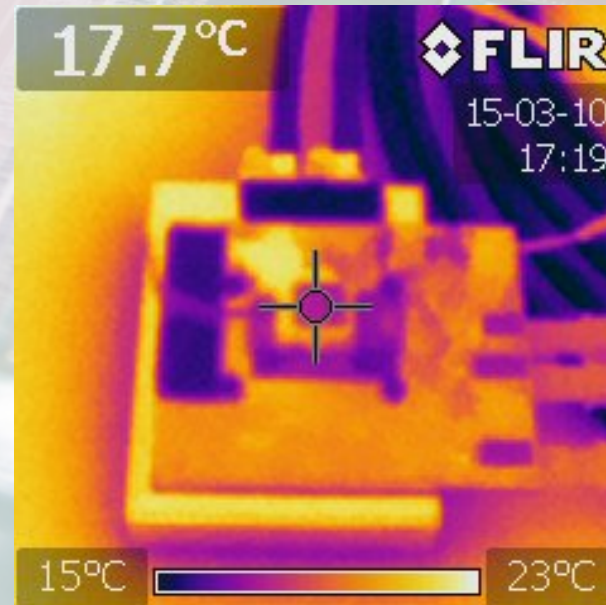
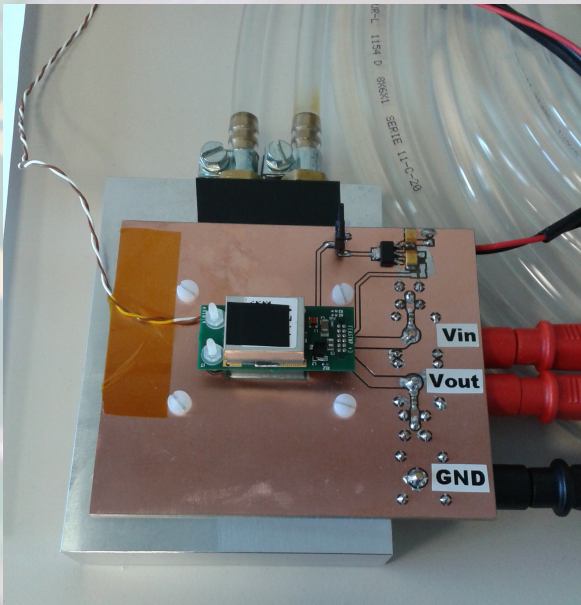


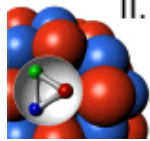


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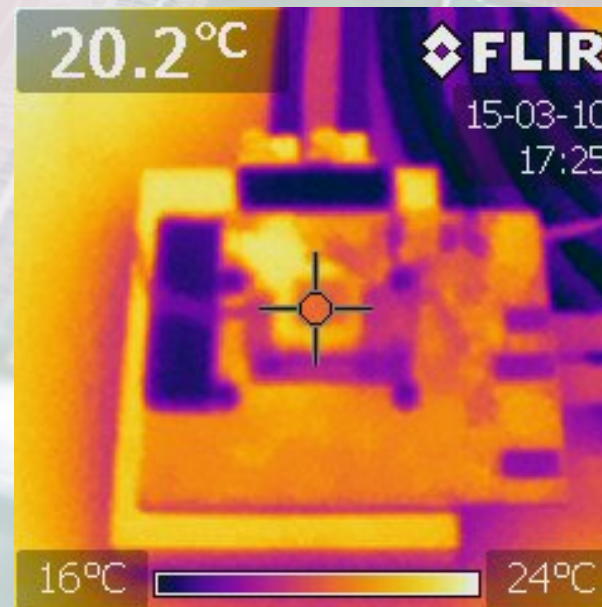
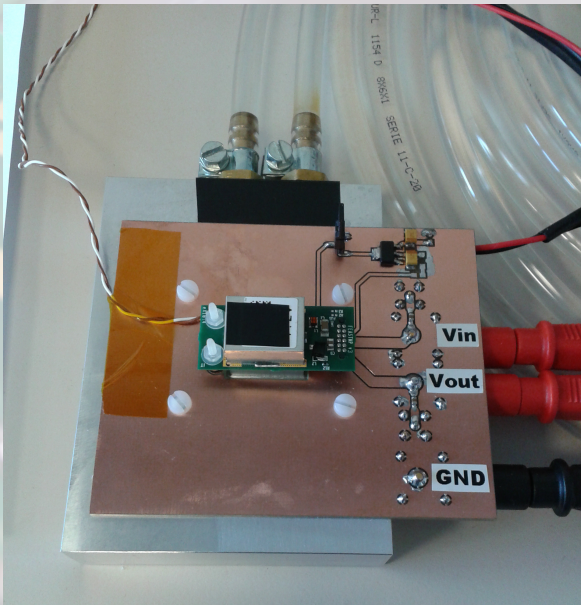


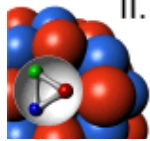


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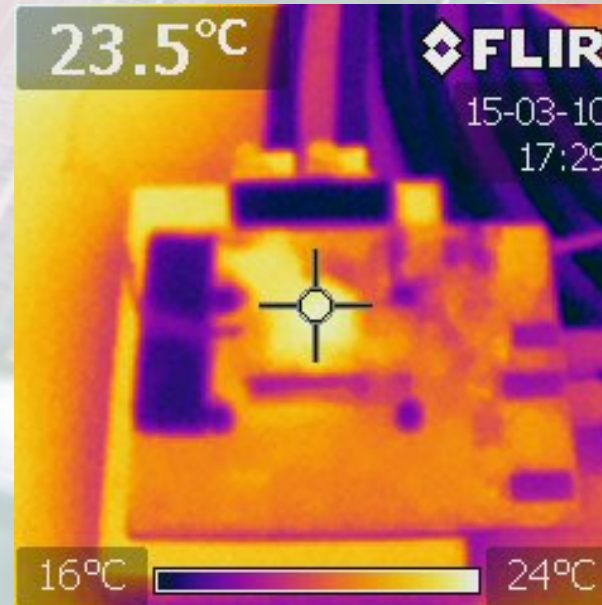
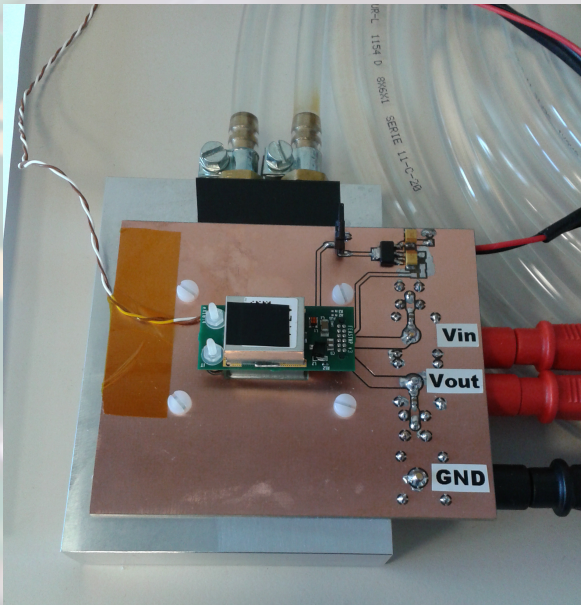


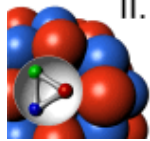


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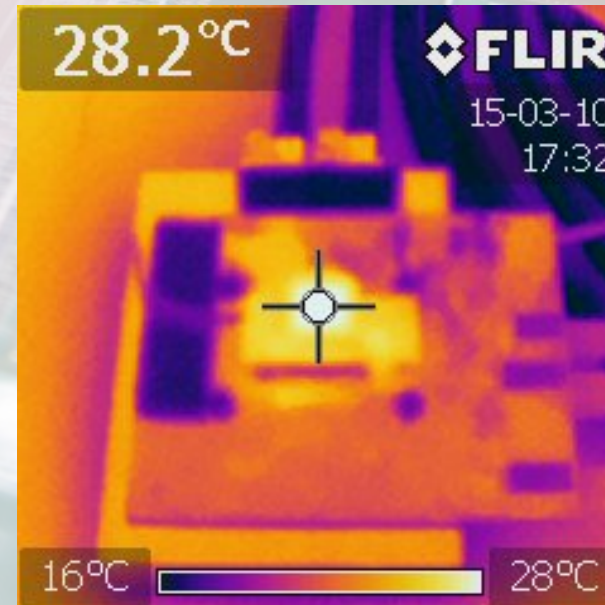
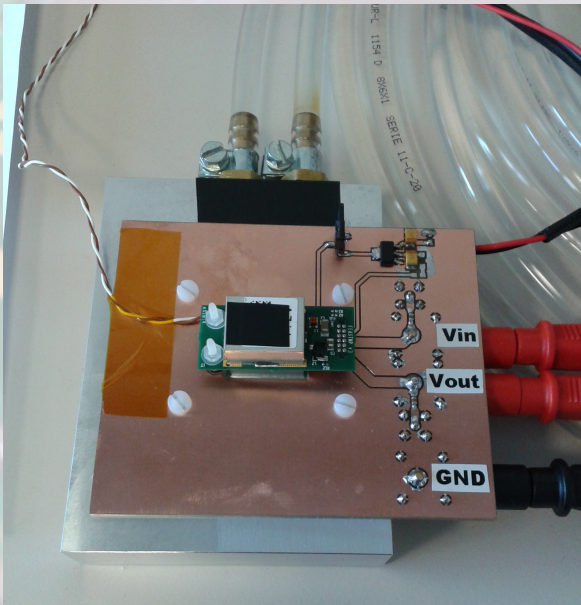


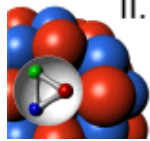


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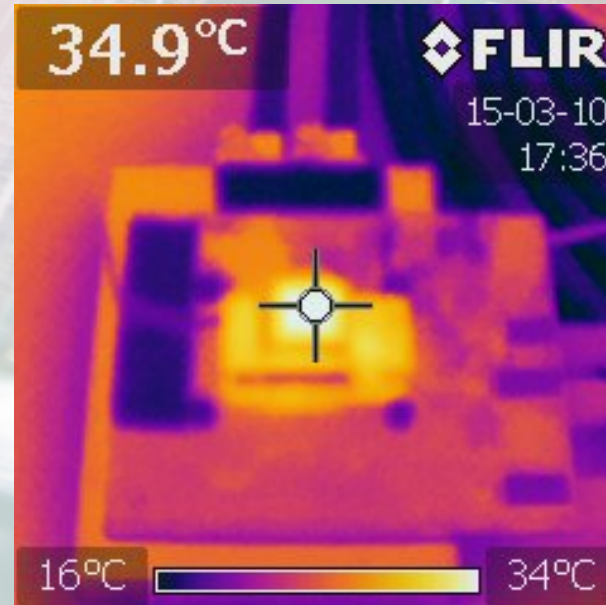
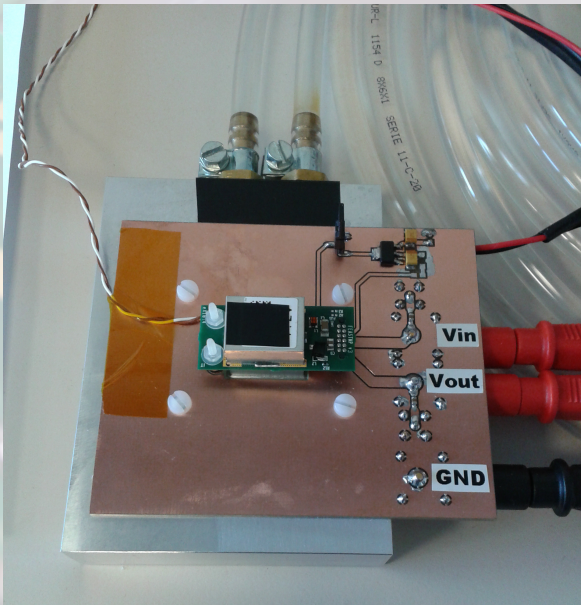


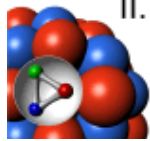


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Test Bench - Results

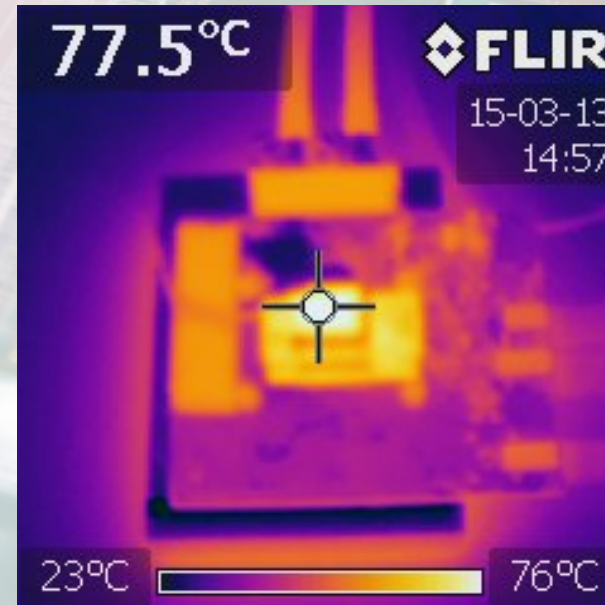
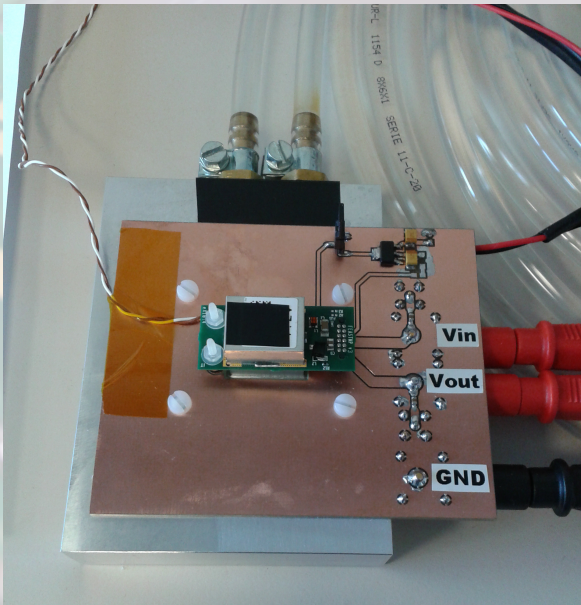
- MOD_00233_1V2

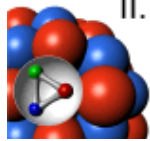
- $T_{\text{amb}} \approx 21.5^{\circ}\text{C}$

- **NO COOLING!**

- $V_{\text{in}} = 8.0 \text{ V}, I_{\text{out}} = 6.0 \text{ A}$

attempt to trigger over-temperature shut-off failed
→ thermal contact to heat sink almost too good
heat sink temperature: $49,5^{\circ}\text{C}$





Test Bench - Results

- MOD_00233_1V2

- $T_{amb} \approx 21.5^\circ\text{C}$

- $T_{heat\ sink} \approx 15.5^\circ\text{C}$

- $Q \approx 1\ \text{l/min}$

• Voltage

- 5 V – FEASTMP min. operating voltage
- 8 V – max. voltage Wiener MPV8008LI

• PASTA (approx./from simulations)

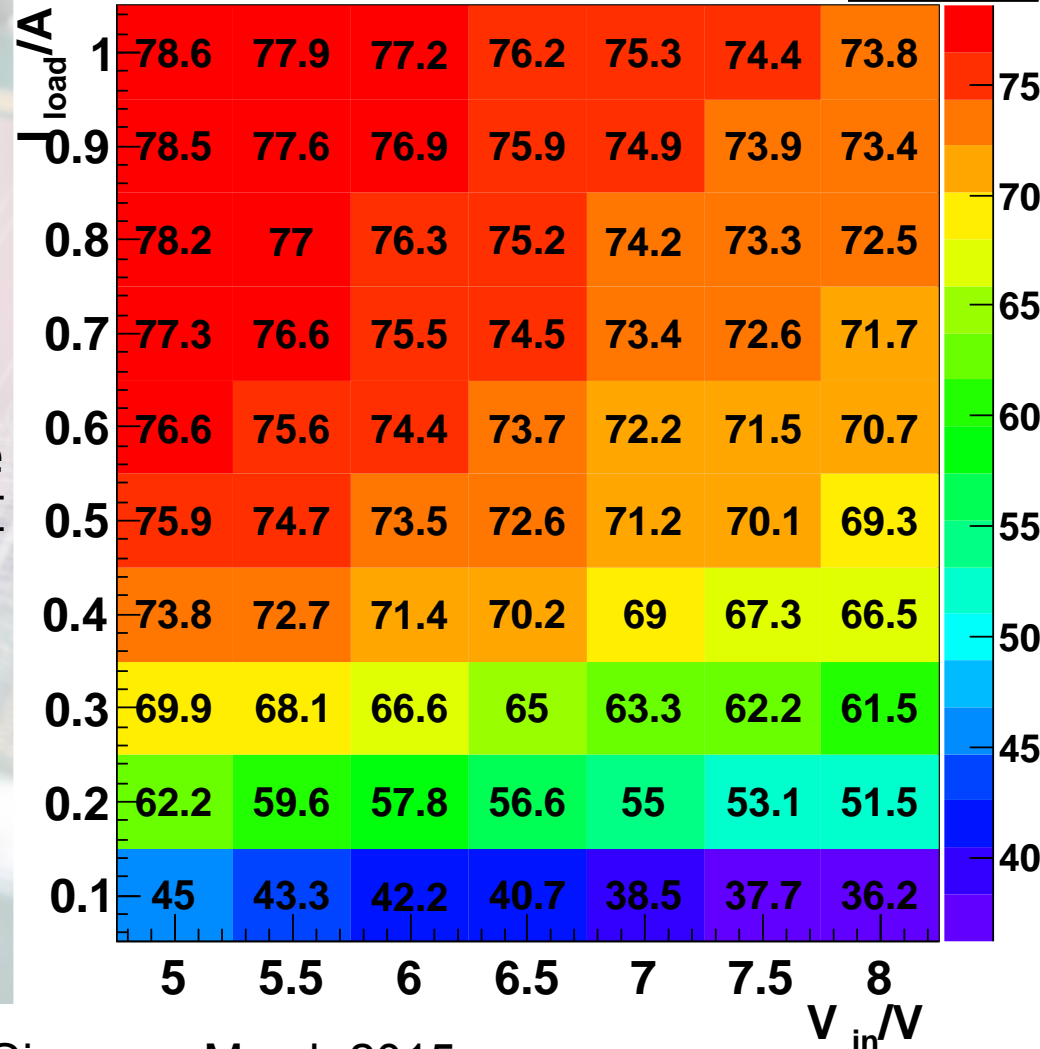
- 100mA analog supply
- 100mA digital supply

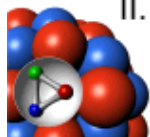
- p-side (7 chips) → **0.7 A** +MDC(0.2A)

- n-side (4 chips) → **0.4 A**

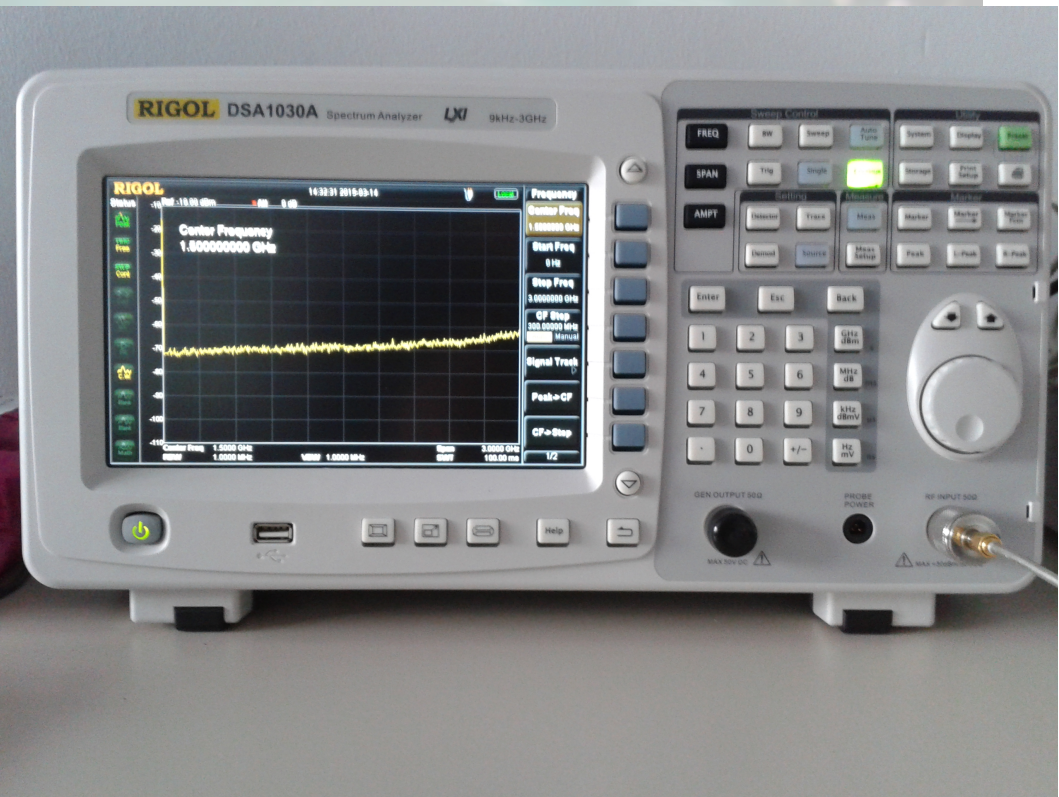
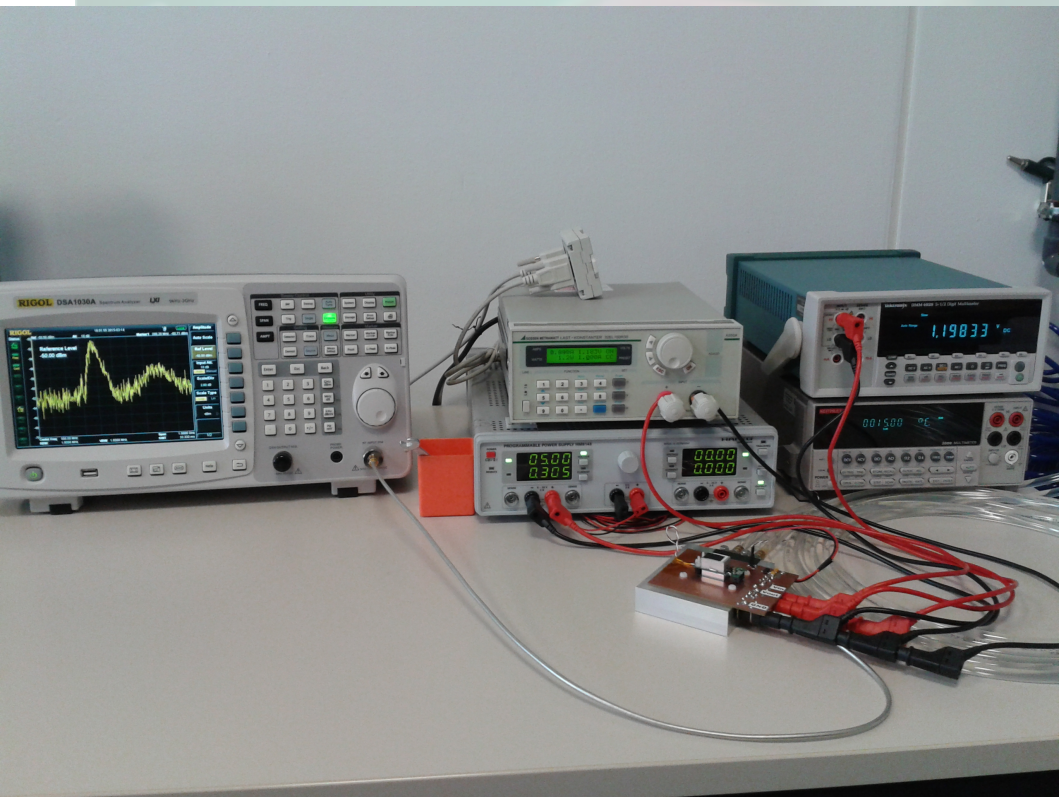
Efficiency Map MOD_00233_1V2

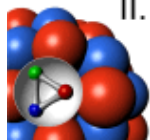
Eff
Entries 70





Test Bench - RF



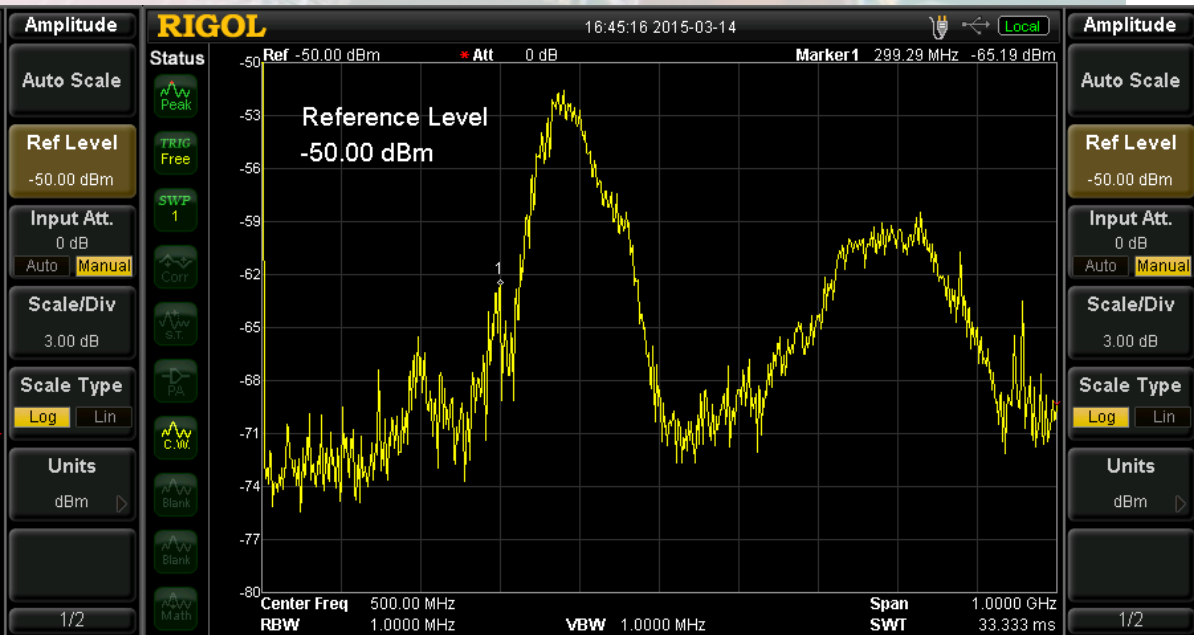
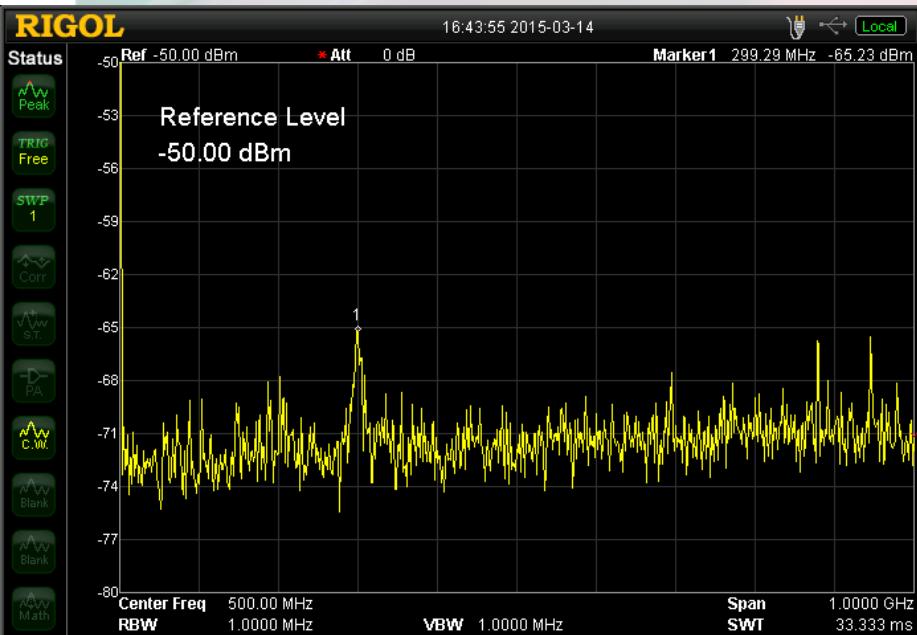


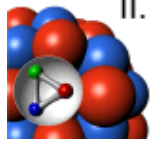
Test Bench - RF

- MOD_00233_1V2
- $V_{in} = 5.0 \text{ V}$
- $I_{out} = 1.0 \text{ A}$

enable = off

enable = on

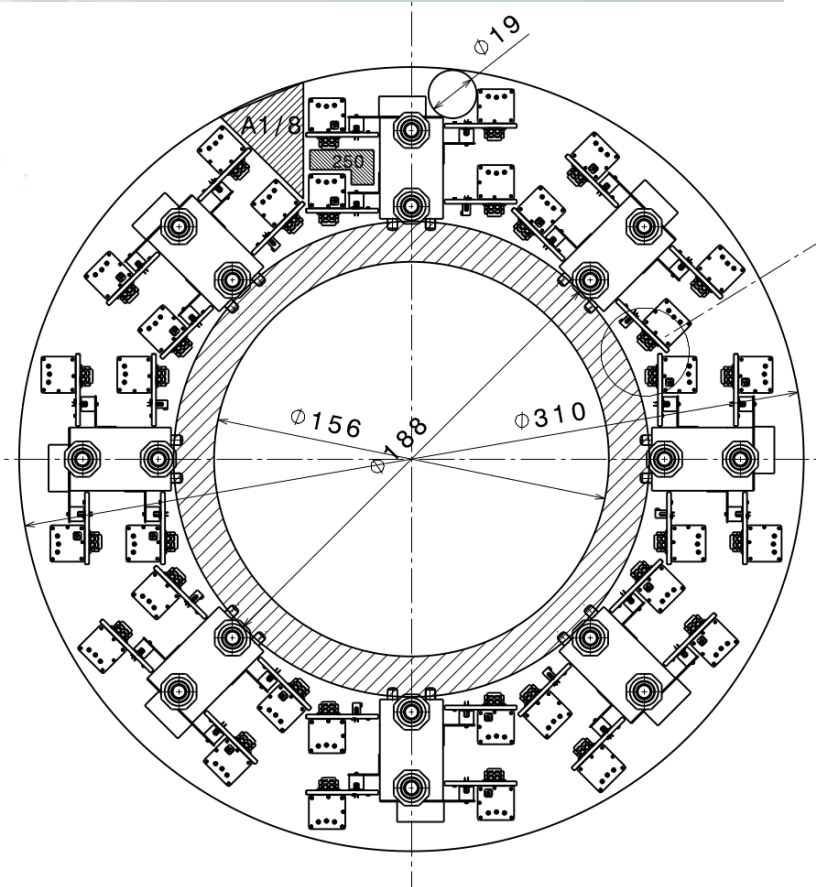
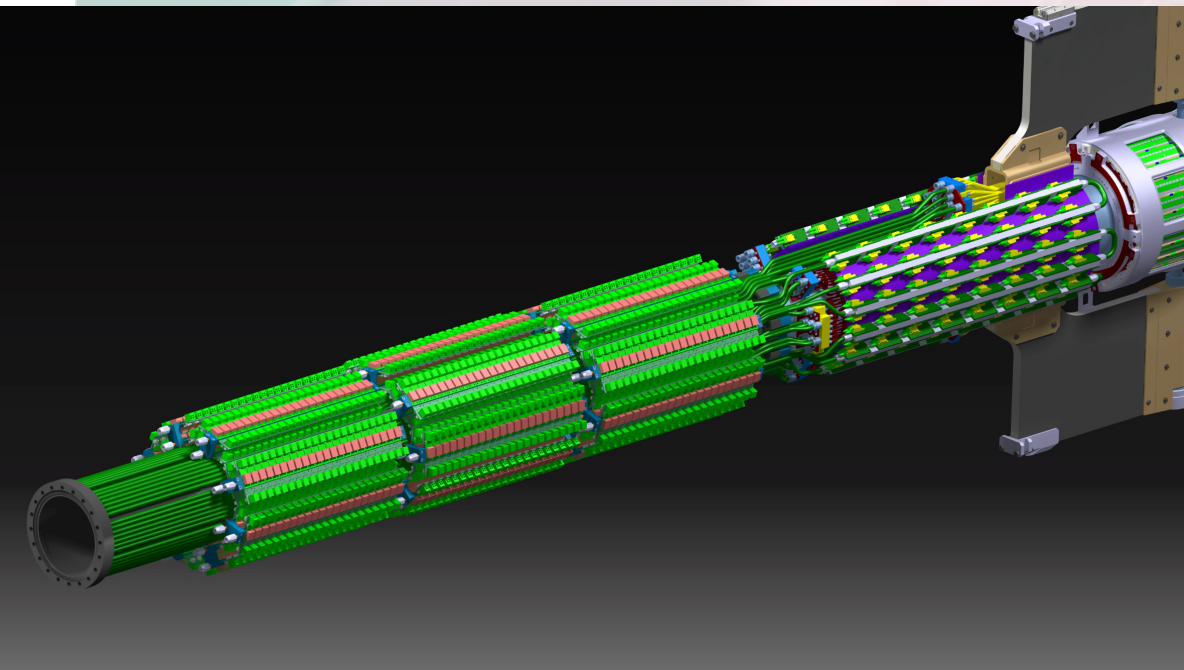


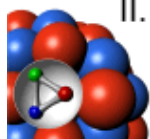


MVD services - DCDC

- Vast amount of DCDC regulators needed
- 1184 already for the strip part

**Not enough space
for cable routing!**

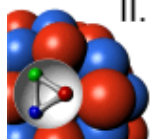




MVD services - DCDC

- Vast amount of DCDC regulators needed
 - 1184 already for the strip part
 - FEASTMP
 - DCDC module chosen to be used in the MVD
 - CERN developed
 - module design "spacious"
(PCB area, component spacing, ...)
- **Smaller DCDC module favorable**

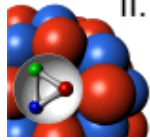




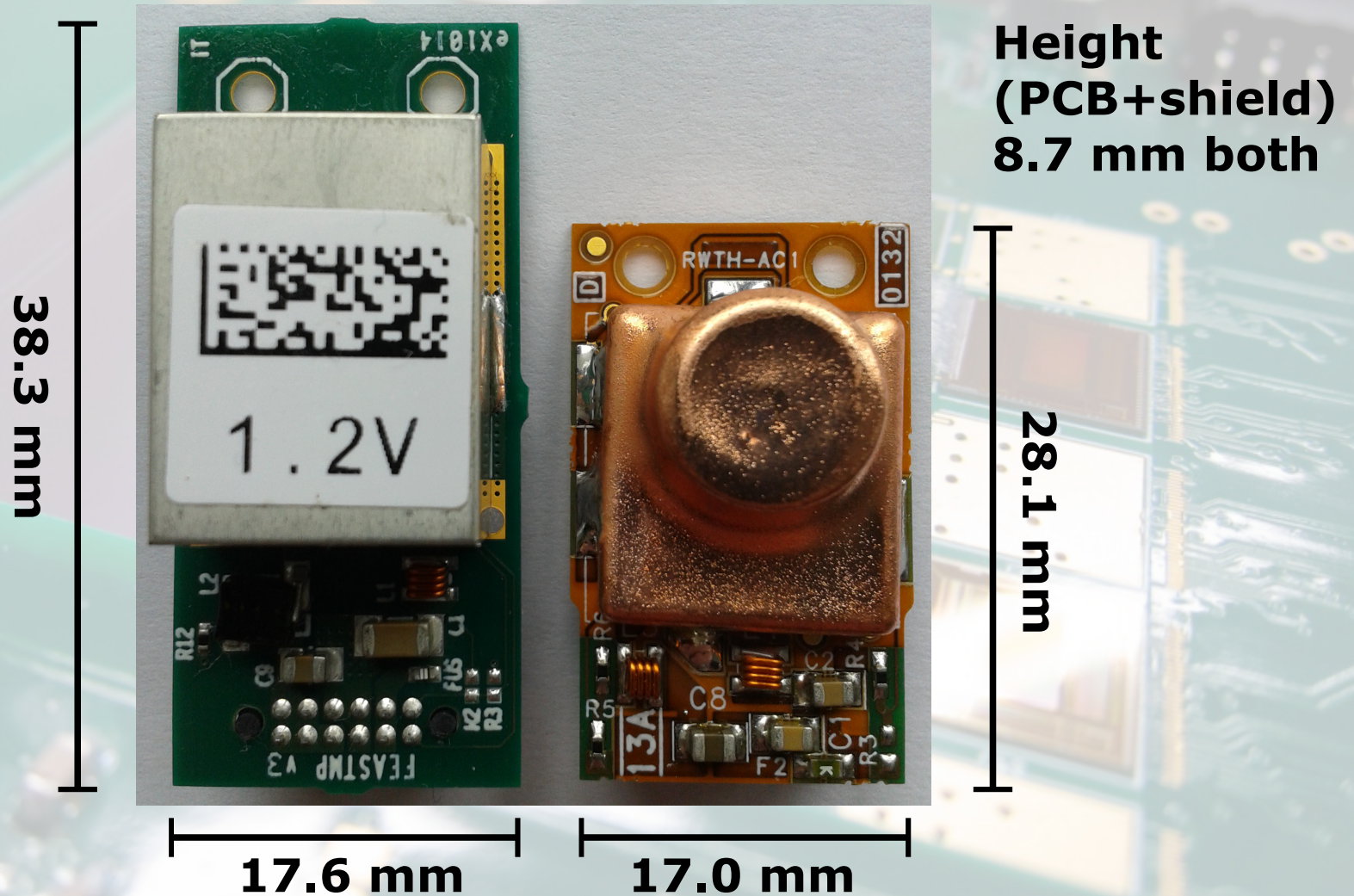
MVD services - DCDC

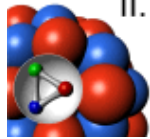
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 - DCDC module chosen to be used in the MVD
 - CERN developed
 - module design "spacious"
(PCB area, component spacing, ...)
- **Smaller DCDC module favorable**
- Possible option: PIX_V13
 - developed at RWTH Aachen for CMS Phase-1 Pixel Upgrade
 - employs CERN FEAST ASIC as well
 - smaller module outline
 - design could be adopted for the MVD





FEASTMP vs PIX_V13

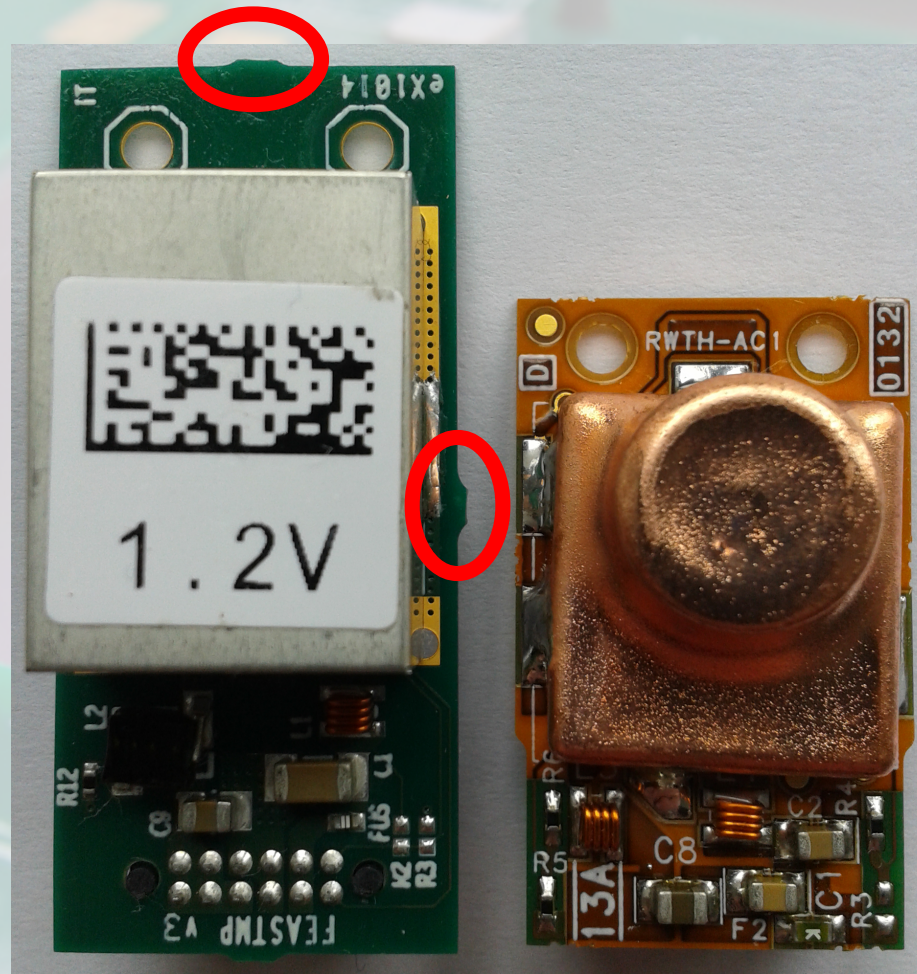




FEASTMP vs PIX_V13

Deviation from nominal size caused by the remaining bridges from scoring of the PCB

38.3 mm

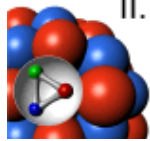


Height
(PCB+shield)
8.7 mm both

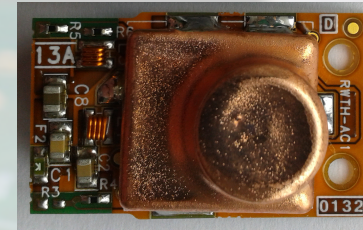
28.1 mm

17.6 mm

17.0 mm



FEASTMP vs PIX_V13



- "Commercial off-the-shelf"
 - acquire from CERN
 - modules are tested (temperature cycles)→ easy/safe option
- Same architecture as FEASTMP
- Design available from Aachen
- Needs work:
 - acquire FEAST ASIC from CERN
 - PCB production
 - PCB assembly
 - tests of all modules for the MVD
- Further optimization possible (size, thermal interface, connector, HalfSw, frequency, ...)