

First steps with the TOFPET ASIC

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Evaluation kit

Ethernet to PC

Xilinx ML605 evaluation kit
Virtex6 FPGA

2 mezzanine boards
each with 64 ch. ASIC

Power Adapter Board (PAB) with
16 ch. HV supply for SiPMs

PETsys TOFPET ASIC evaluation kit v1.0

First steps

- Documentation, firmware, demo programs, etc. provided by PETsys (GoogleDrive)
- Getting started with test routines and calibration
- Test functionality of ML605 board running a Build-In System Test
- Check the communication between the two boards (FPGA and TOFPET) by testing clock and HV

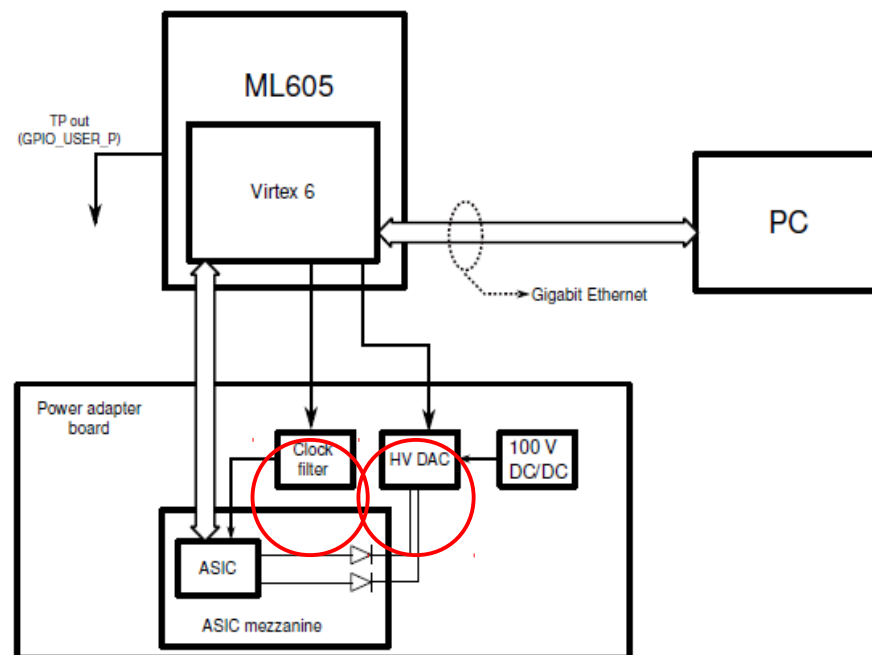


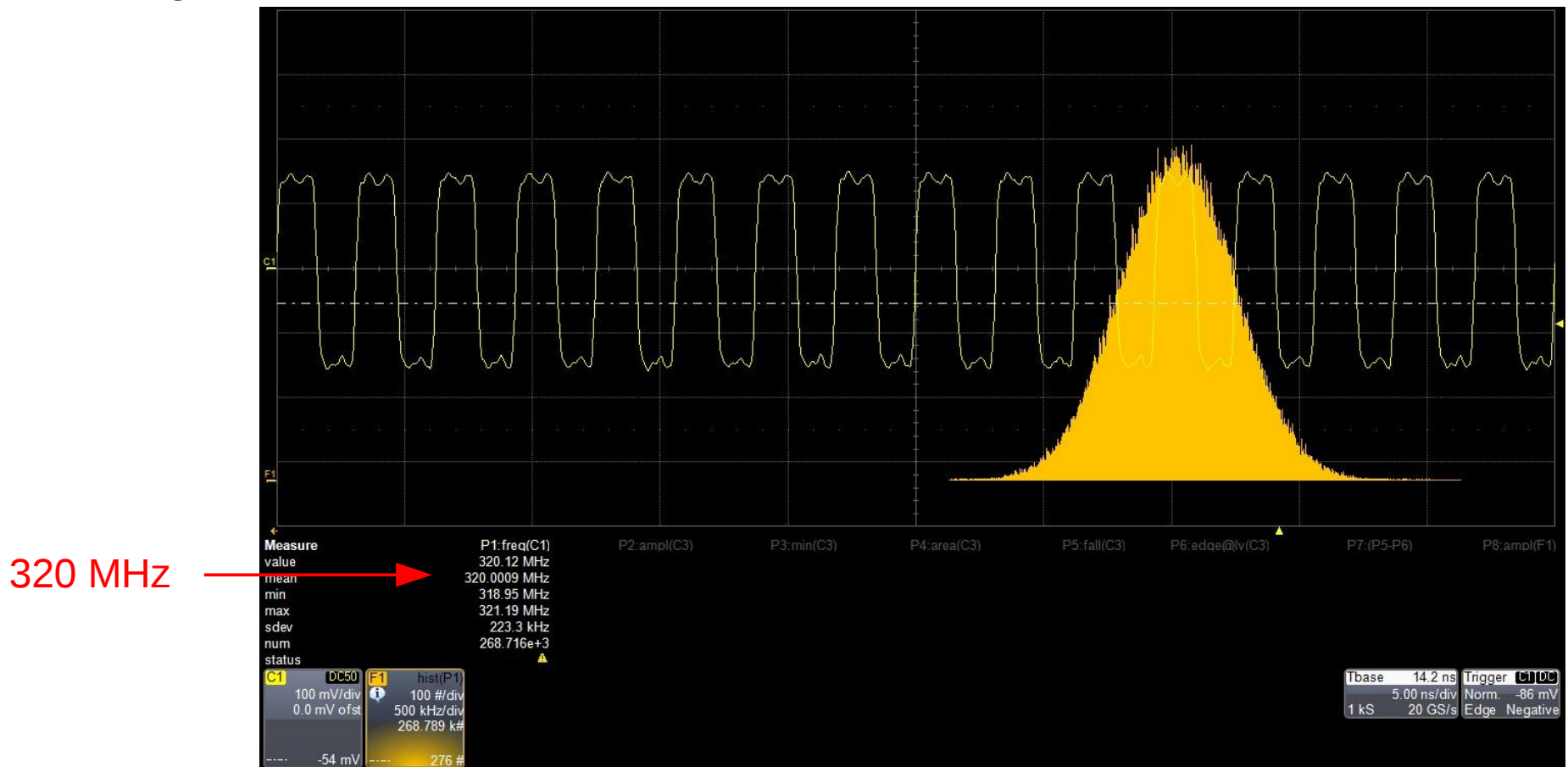
Figure 1.1: System diagram

TOFPET ASIC evaluation kit software user guide v3.1,
PETsys, March 2015

320 MHz clock

The PAB should receive a 320 MHz clock from the FPGA

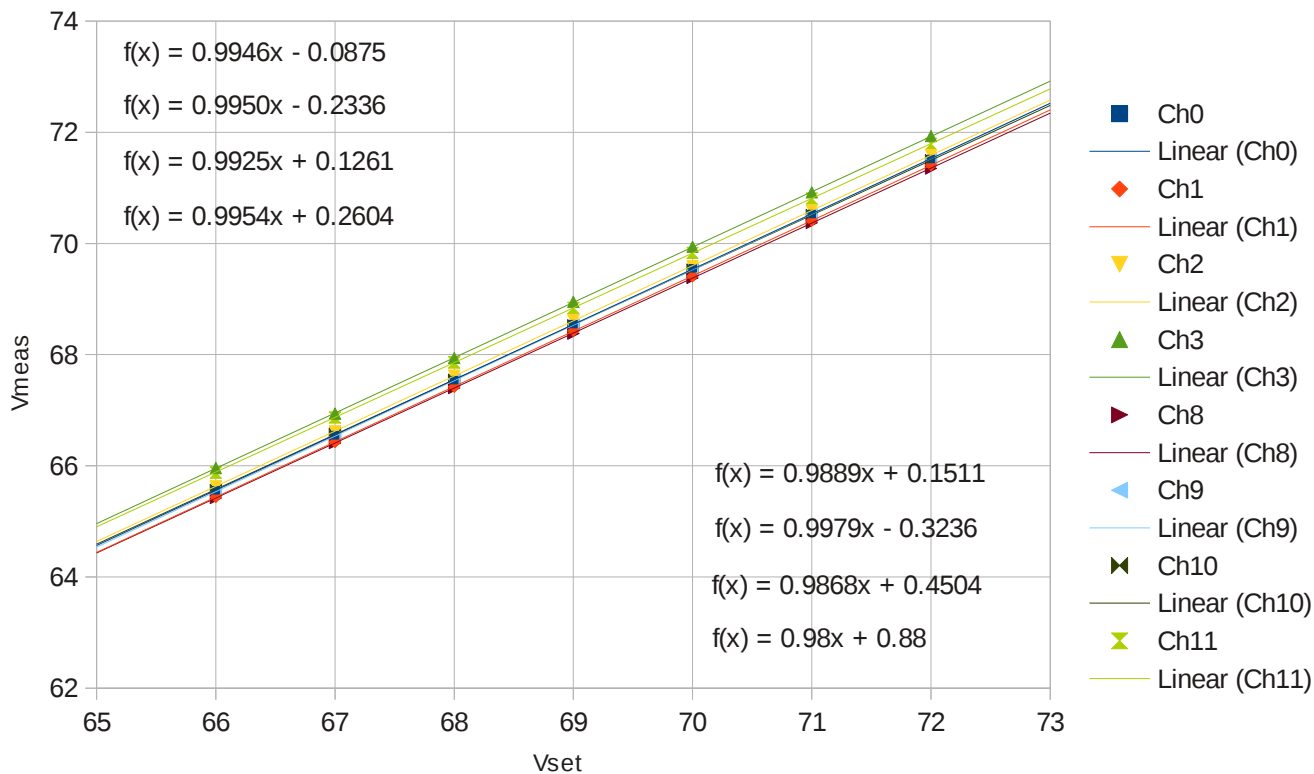
Clock signal measured at the PAB:



→ Communication between FPGA and TOFPET works

HV supply

- The PAB has an internal HV supply module which can be controlled via the FPGA
- The HV DAC has to be calibrated by comparing the set voltage (V_{set}) and the actual voltage (V_{meas}) at the output of the mezzanine boards
- Shows again that communication works



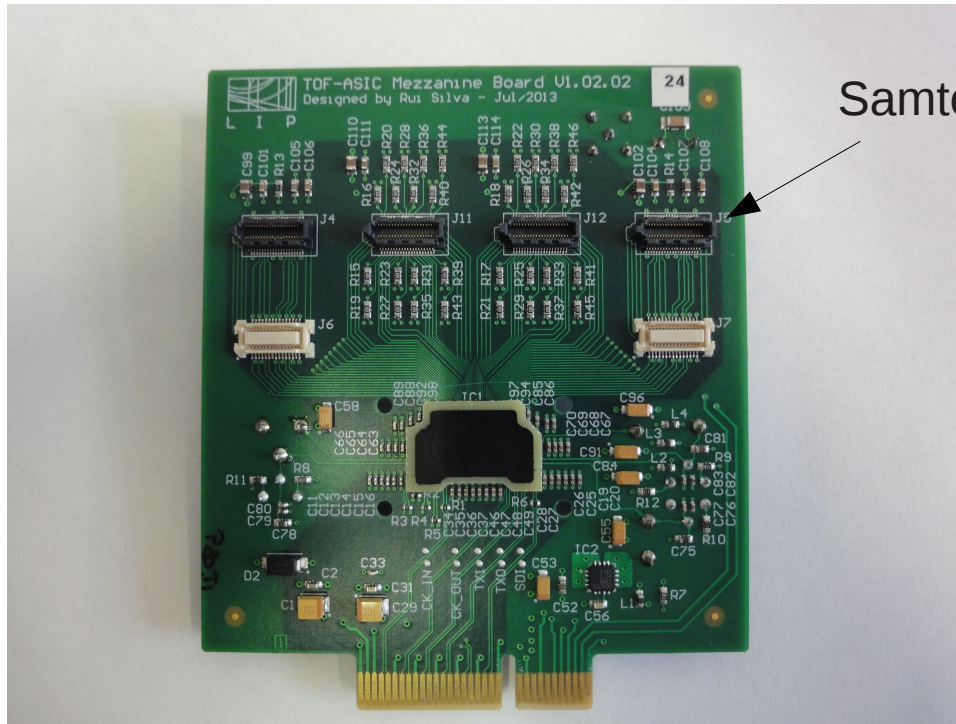
Simple linear regression:

$$V_{\text{meas}} = m \times V_{\text{set}} + b$$

Parameters m, b are used to produce a calibration file and calibrate the HV DAC.

Current work and next steps

- The mezzanine board connects to 4 Hamamatsu 16 channel arrays
- We need an adapter to connect single SiPMs



Samtec SS4 connector fits to ST4



We will prepare a printboard with ST4 on one side and connectors for SiPMs on the other side.

Next steps: read-out SiPM signals, determine time resolution, attach scintillator tile

Thank you !