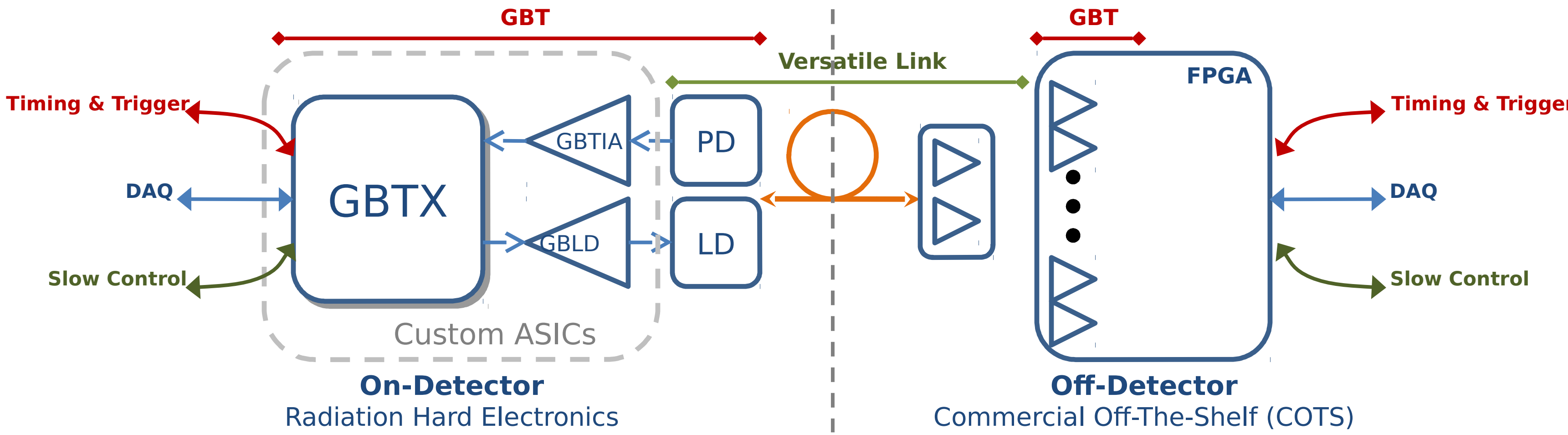
GBT Project Status

Paulo Moreira
On behalf of the GBT collaboration
2015 – 02 – 03

Radiation Hard Optical Link

Development of an high speed bidirectional radiation hard optical link:

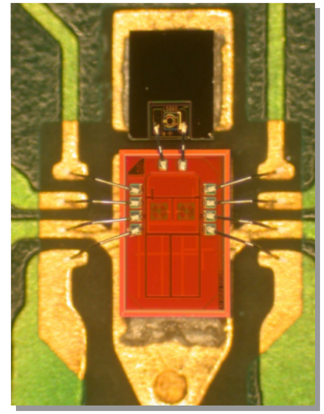
- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging
- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging



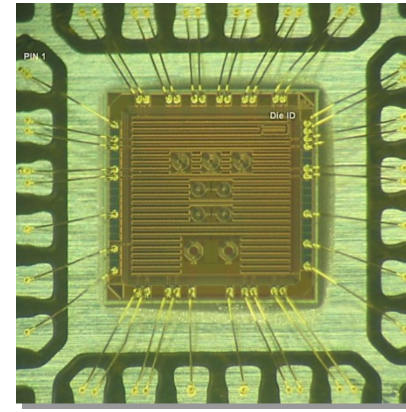
GBTX Chip Set

- The GBT chipset comprises:
  - GBTIA:
    - 4.8 Gb/s Transimpedance Amplifier
    - Amplifies the weak photo-current detected by the PIN diode
  - GBLD:
    - 4.8 Gb/s Laser Driver
    - Modulates laser current to achieve electro-optical conversion
  - GBTX:
    - 4.8 Gb/s Transceiver
    - Manages the communications between the counting room and the frontend modules
  - GBT – SCA
    - Slow Control Adapter
    - Experiment control and environment monitoring
- GBTIA, GBLD and GBTX:
  - Have been successfully prototyped
  - Radiation tolerance proved to > 100 Mrad
- GBT – SCA:
  - Prototypes currently being tested

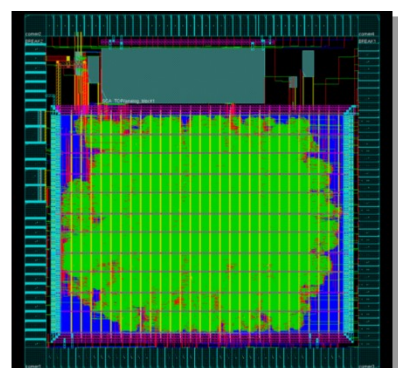
GBTIA



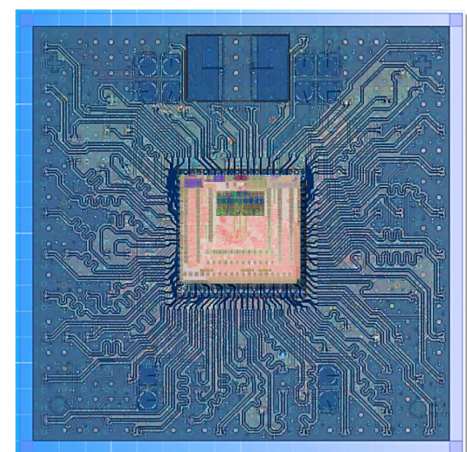
GBLD



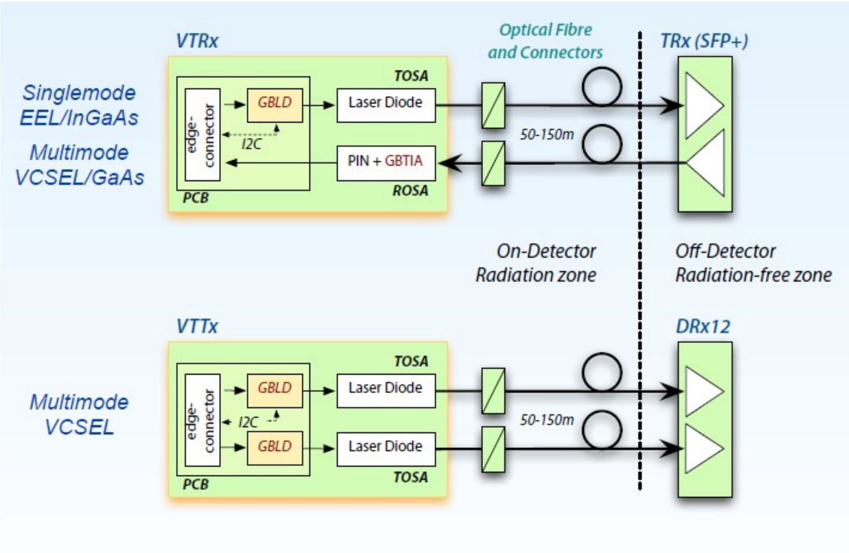
GBT – SCA

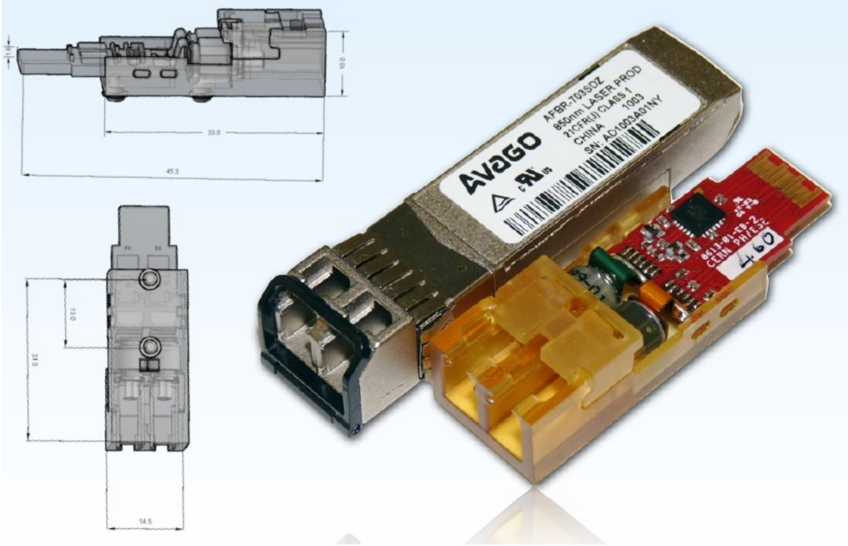


GBTX



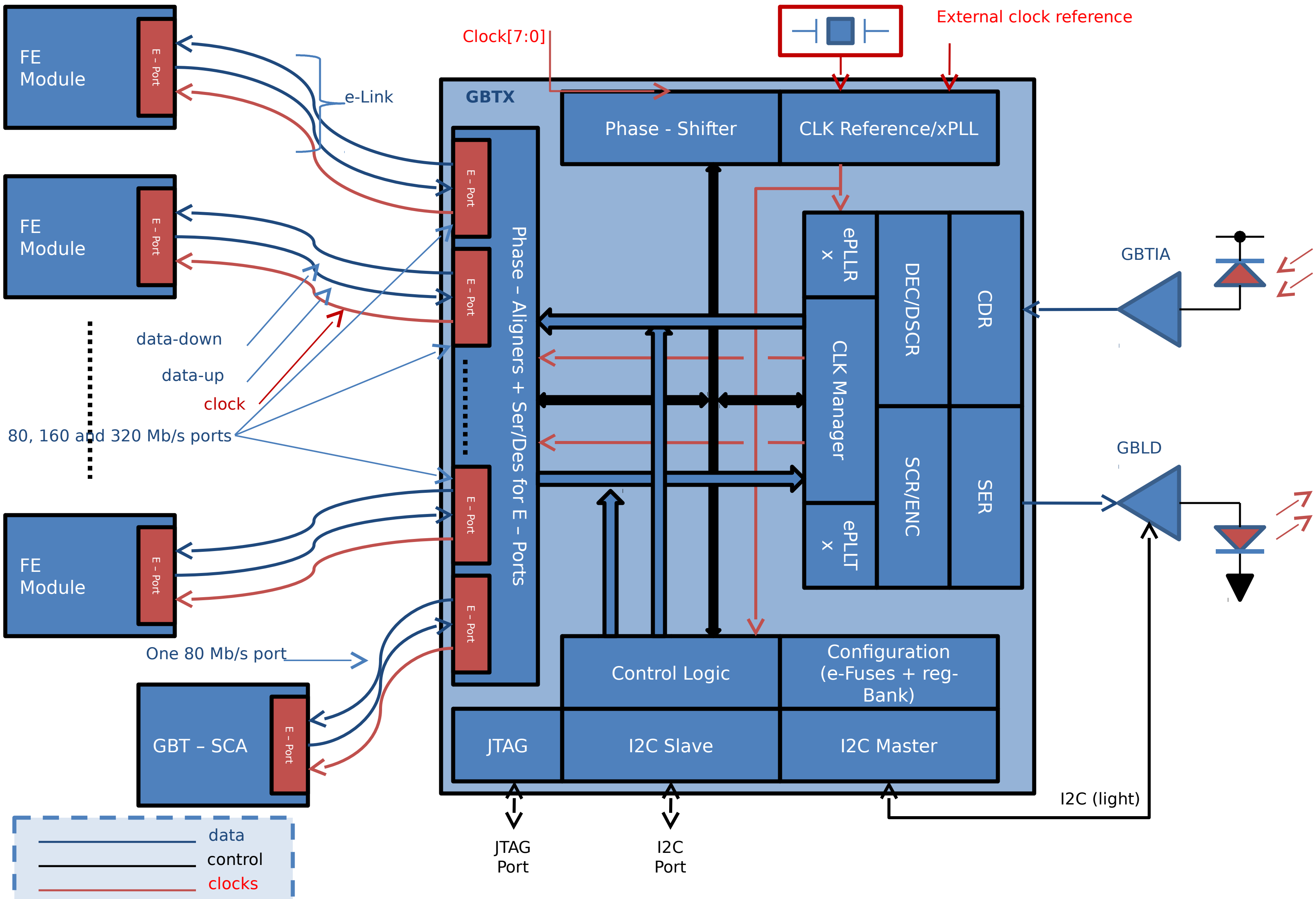
Versatile Link





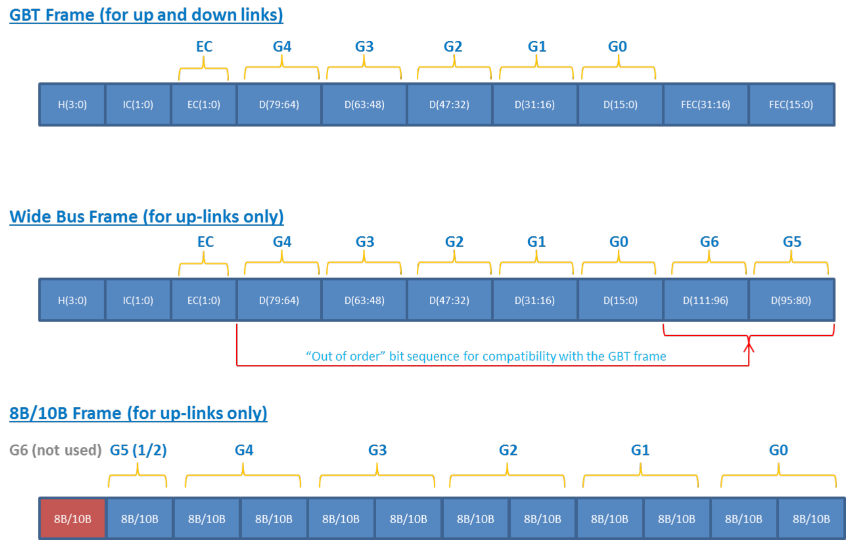
- Small Form Factor (SFP) Transceiver:
  - Data rate: 5 Gb/s
  - Wave length:
    - 850 nm, Multimode
    - 1310 nm, Single mode
  - Function:
    - Point-to-point
    - Point-to-multipoint
- Development of pluggable modules.
  - Two versions:
    - Transceiver (**VTRx**)
    - Double transmitter (**VTTx**)
  - Compatible with the commercial counterparts
  - LC connectors
  - Length reduced to 43.5 mm
  - Contains:
    - The GBTIA & GBLD
    - Radiation qualified PIN diodes and Lasers
  - Radiation tolerant:
    - 50 Mrad
    - 5 x 10^{14} n/cm^2
  - Prototyping phase concluded:
    - Prototypes available
    - Production planed for 2015
    - Target LS2 upgrades

The GBT System



GBTX Data Bandwidth

- The GBTX supports three frame types:
  - ***“GBT” Frame***
  - ***“Wide Bus” Frame***
  - ***“8B/10B” Frame***
- “GBT” Mode
  - User bandwidth: 3.28 Gb/s
    - Up/down-links
- “Wide Bus” and “8B/10B”frames are only supported for the uplink
  - The downlink always uses the “GBT” frame.
- “8B/10B” Mode
  - Downlink data 8B/10B encoded
  - No FEC
  - User bandwidth: 3.52 Gb/s
- “Wide Bus” Mode:
  - Uplink data scrambled
  - No FEC
  - User bandwidth: 4.48 Gb/s

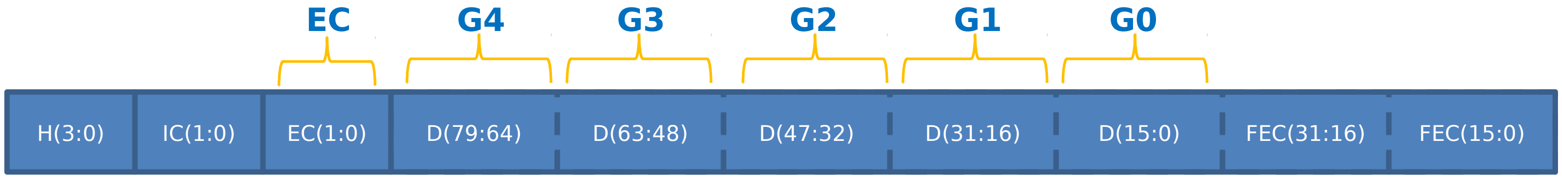


GBT Frame:

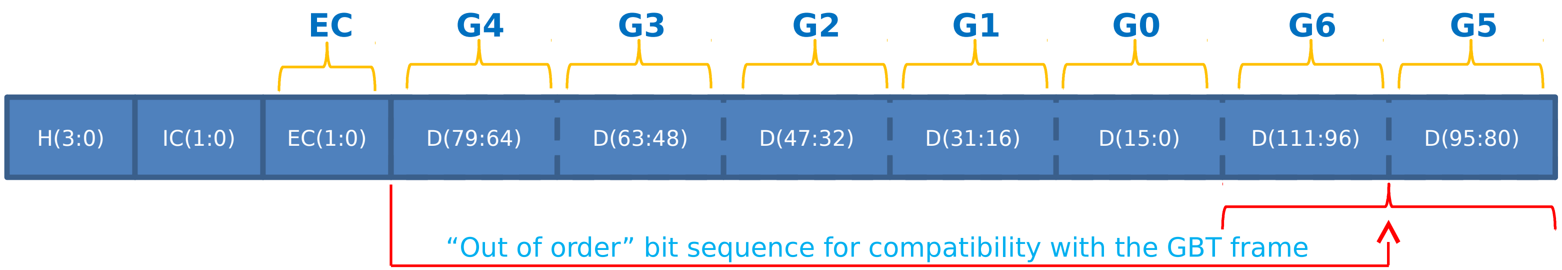
- Frame Synchronization:
  - DC balanced and “redundant” header
- Forward Error Correction:
  - Interleaved Reed-Solomon double error correction
  - 4-bit symbols (RS(15,11))
  - Interleaving: 2
  - Error correction capability:
    - 2 Interleaving × 2 RS = 4 symbols = 16-bits
  - Code efficiency: 88/120 = 73%

GBTX Frames

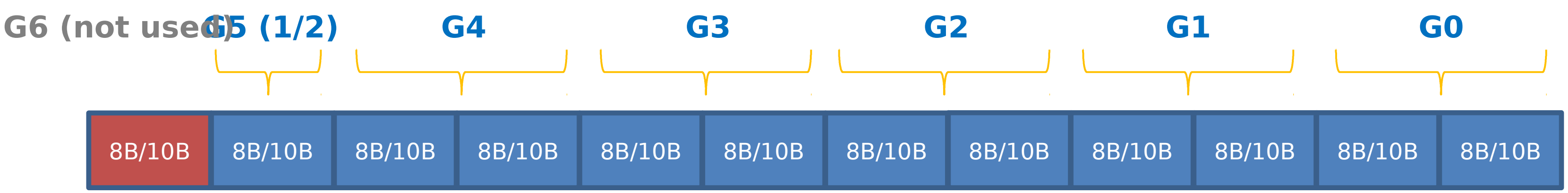
GBT Frame (for up and down links)



Wide Bus Frame (for up-links only)



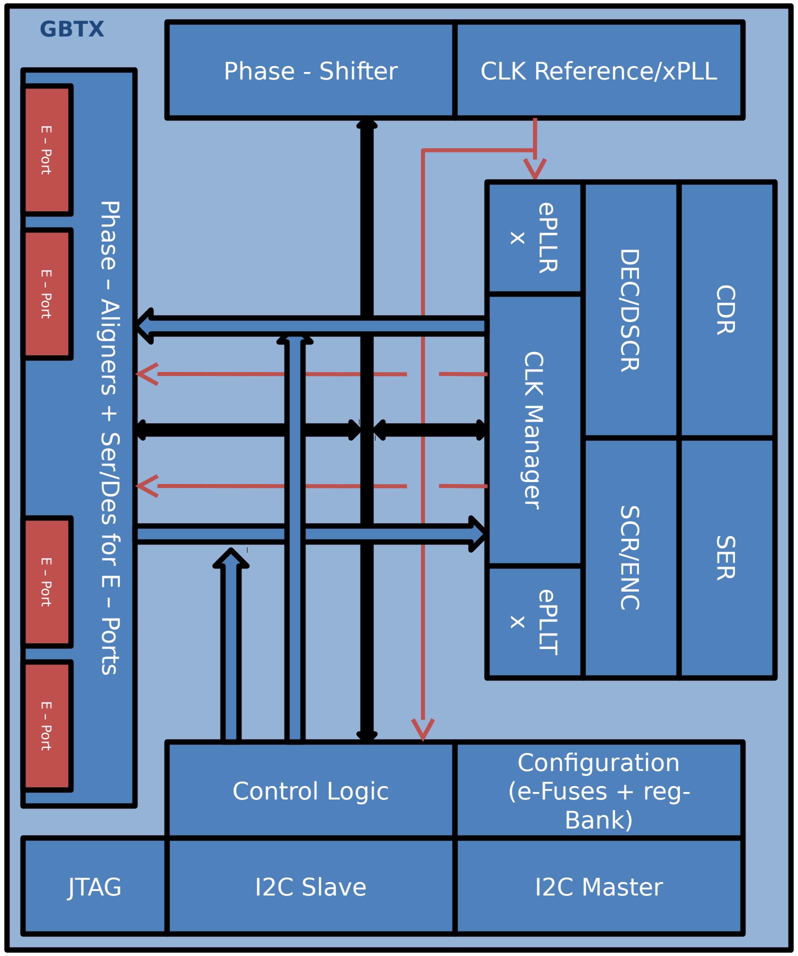
8B/10B Frame (for up-links only)



GBTX Functionality (1/4)

e-Links

- 40 bi-directional e-Links
  - Up to 40 @ 80 Mb/s
  - Up to 20 @ 160 Mb/s
  - Up to 10 @ 320 Mb/s
- e-Port data rate can be set independently for:
  - each group
  - Input / output ports
- 1 bi-directional e-Link:
  - 80 Mb/s
- 40 e-Link clocks (fixed phase) programmable in frequency:
  - 40/80/160/320 MHz (per group)
  - *(independently of the bit rate)*
- Automatic, semi-automatic or user controlled phase alignment of the incoming serial data embedded in the e-Ports
  - Automatic alignment
    - Tracks temperature and voltage variations
    - Transparent to the user
    - Works on any type of data:
      - DC balanced / un-balanced
      - A few “occasional” transition enough to ensure correct operation



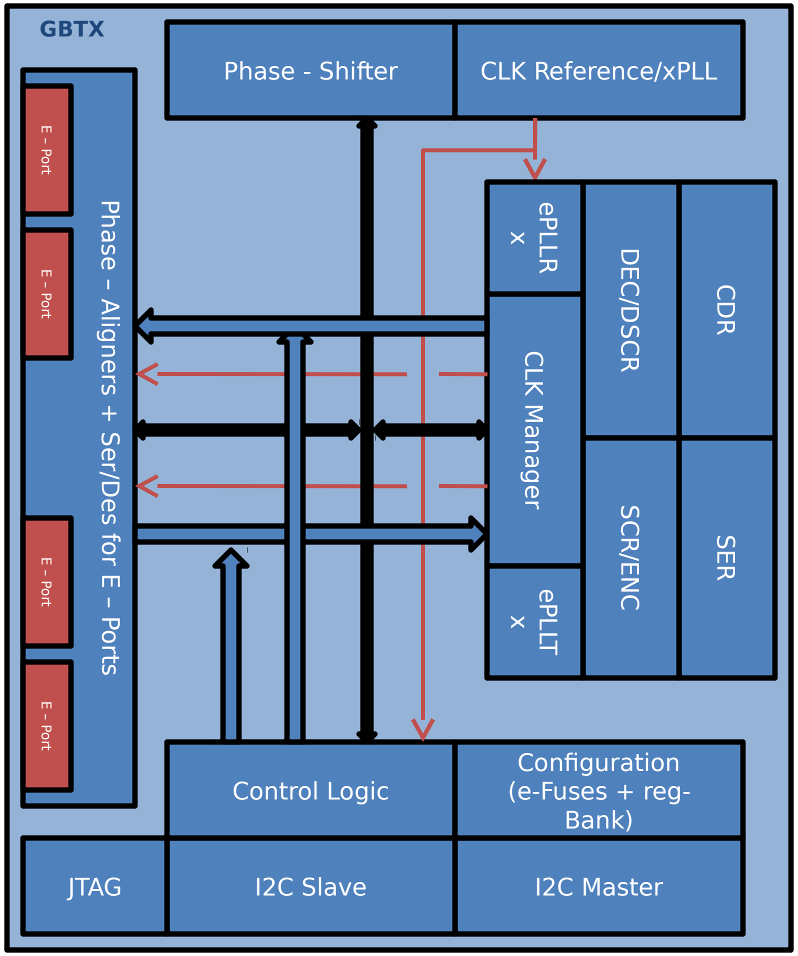
GBTX Functionality (2/4)

e-Links Special cases

- 8B/10B mode:
  - 44 input (max @ 80 Mb/s)
  - 36 output (max @ 80 Mb/s)
    - (Four outputs reused as inputs)
- Wide-Bus mode:
  - 56 input (max @ 80 Mb/s)
  - 24 output (max @ 80 Mb/s)
    - (16 “outputs” reused as inputs)

e-Links electrical characteristics

- Drivers:
  - SLVS signaling
- Receivers:
  - SLVS/LVDS signaling



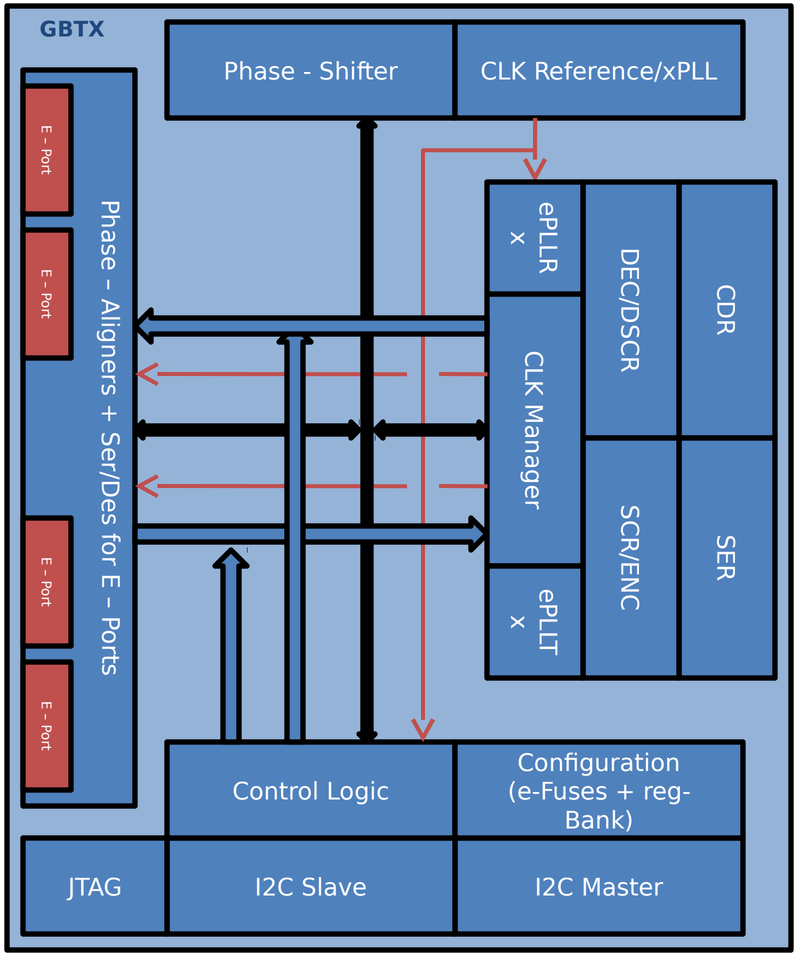
GBTX Functionality (3/4)

Phase-Shifter

- 8 independent clocks
- Programable in frequency:
  - 40 / 80 / 160 / 320 MHz
- Programable in phase:
  - 0 to 360◦
  - Phase resolution: 50 ps
    - (for all frequencies)
- Clock driver electrical levels:
  - SLVS

Reference clock:

- On package crystal
- Built-in crystal oscillator
- Built-in VCXO based PLL (xPLL)
- External reference can used as well



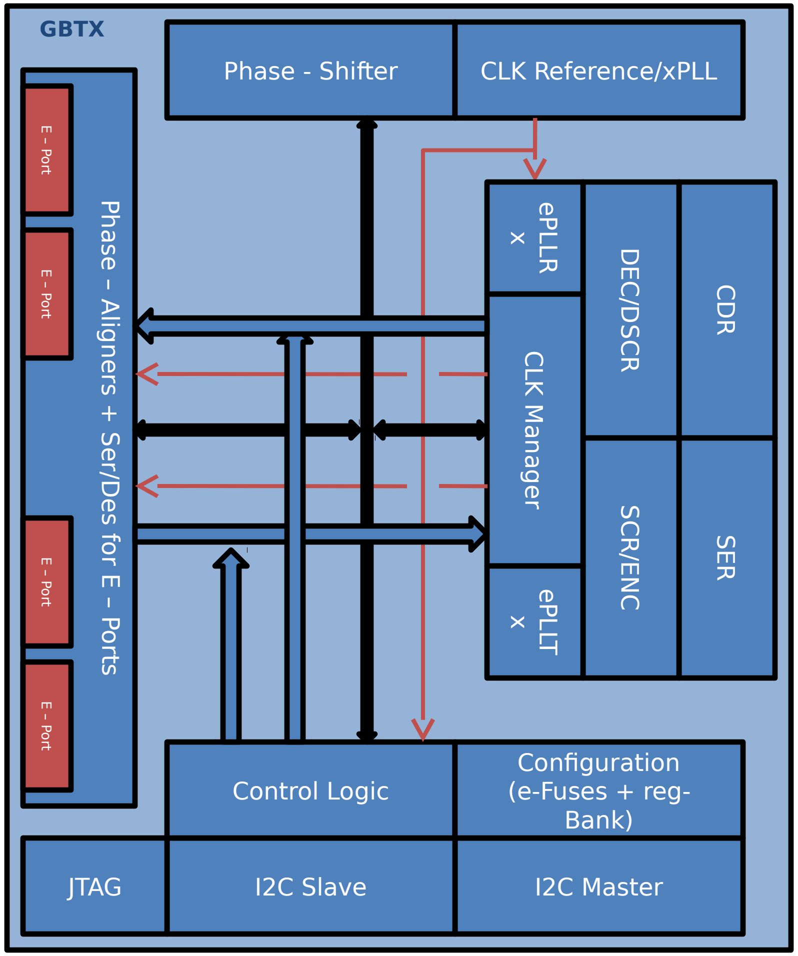
GBTX Functionality (4/4)

Chip Control

- e-Fuse register bank for burn in configuration
  - Standalone operation
  - Ready at power up
- Dynamic configuration and control
  - I2C Slave interface
  - IC control channel trough the optical link
- Watchdog circuit for chip operation supervision.

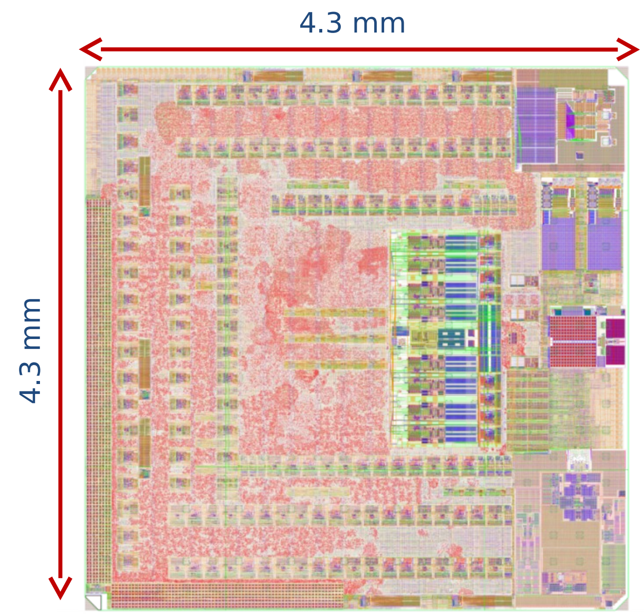
GBLD Control

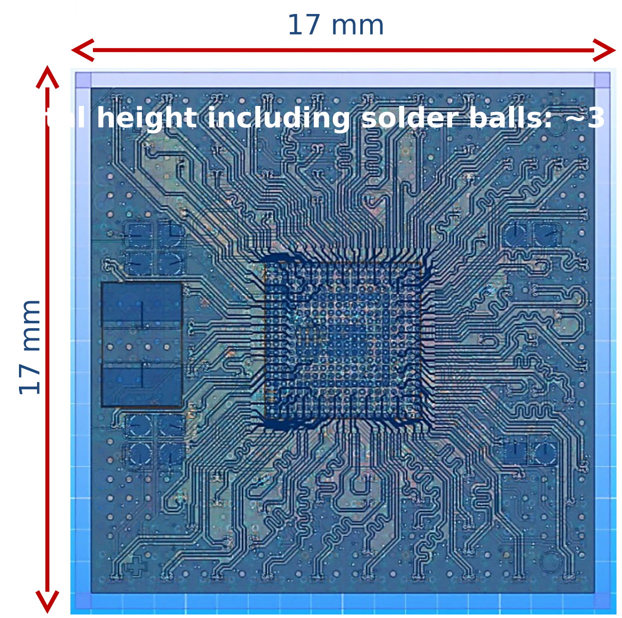
- GBLD dedicated I2C master interface
  - Copies configuration burned in the GBTX into the GBLD at start-up
  - Allows to program the GBLD either through the IC channel or through the I2C slave port



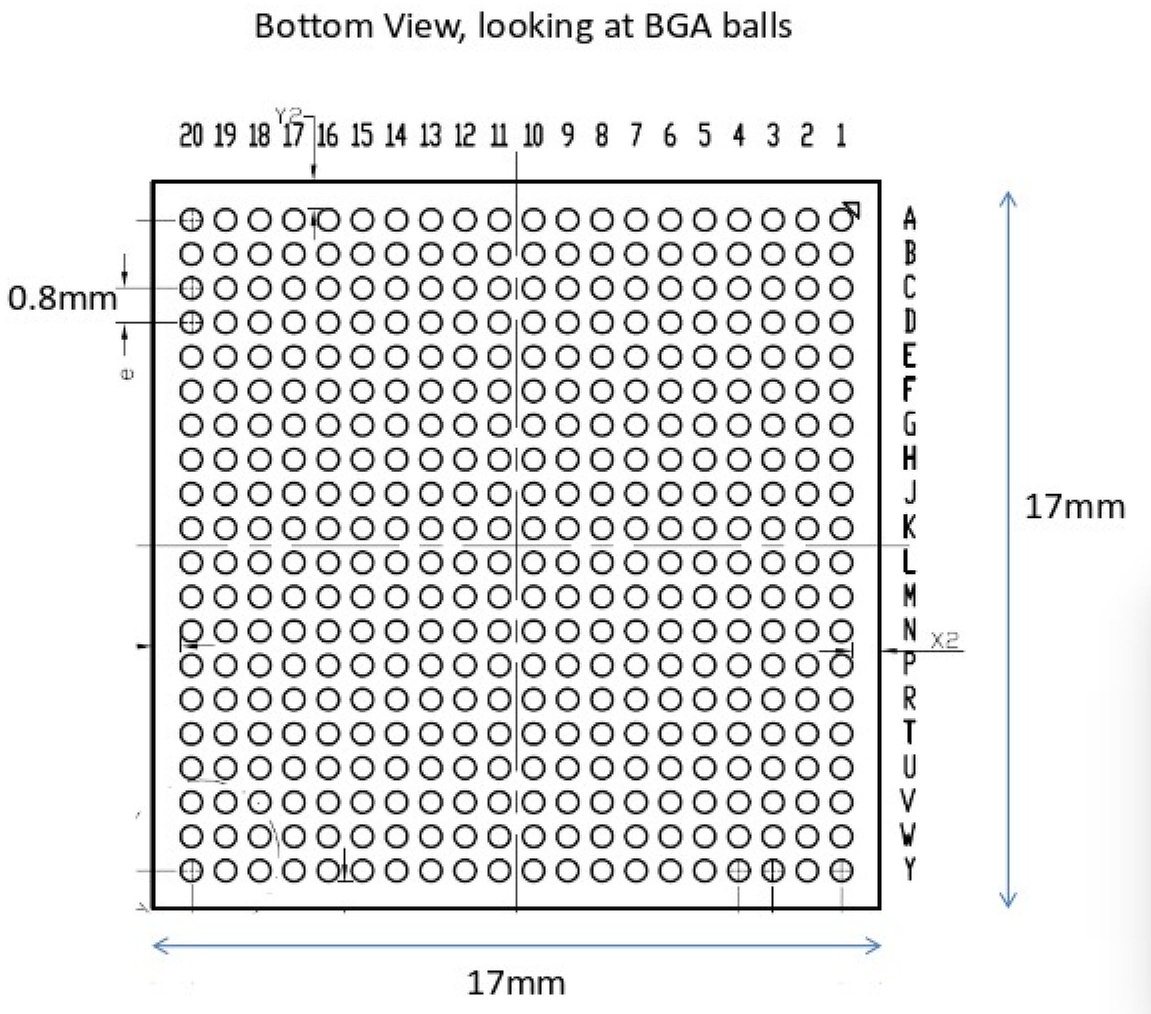
GBTX In Numbers

- ½ million gates
- Approximately:
  - 300 8-bit programable registers (all TMR)
  - 300 8-bit e-Fuse memory
- Clock tree (chip wide):
  - 9 clock trees (all TMR)
  - Frequencies: 40/80/160/320 MHz
- 7 PLLs:
  - RX: CDR PLL + Reference PLL (2.4 GHz)
  - Serializer PLL (4.8 GHz)
  - Phase-Shifter PLL (1.28 GHz)
  - xPLL (VCXO based PLL, 80 MHz)
  - (2x) ePLL (320 MHz)
- 17 master DLLs:
  - 9 for phase alignment of the e-links
  - 8 for clock de-skewing
- 56 replica delay lines:
  - For phase alignment of the e-links
- 7 power domains:
  - Serializer (1.5V)
  - DESerializer (1.5V)
  - Clock Manager (1.5V)
  - Phase shifter (1.5V)
  - Core digital (1.5V)
  - I/O (1.5V)
  - Fuses (3.3V)



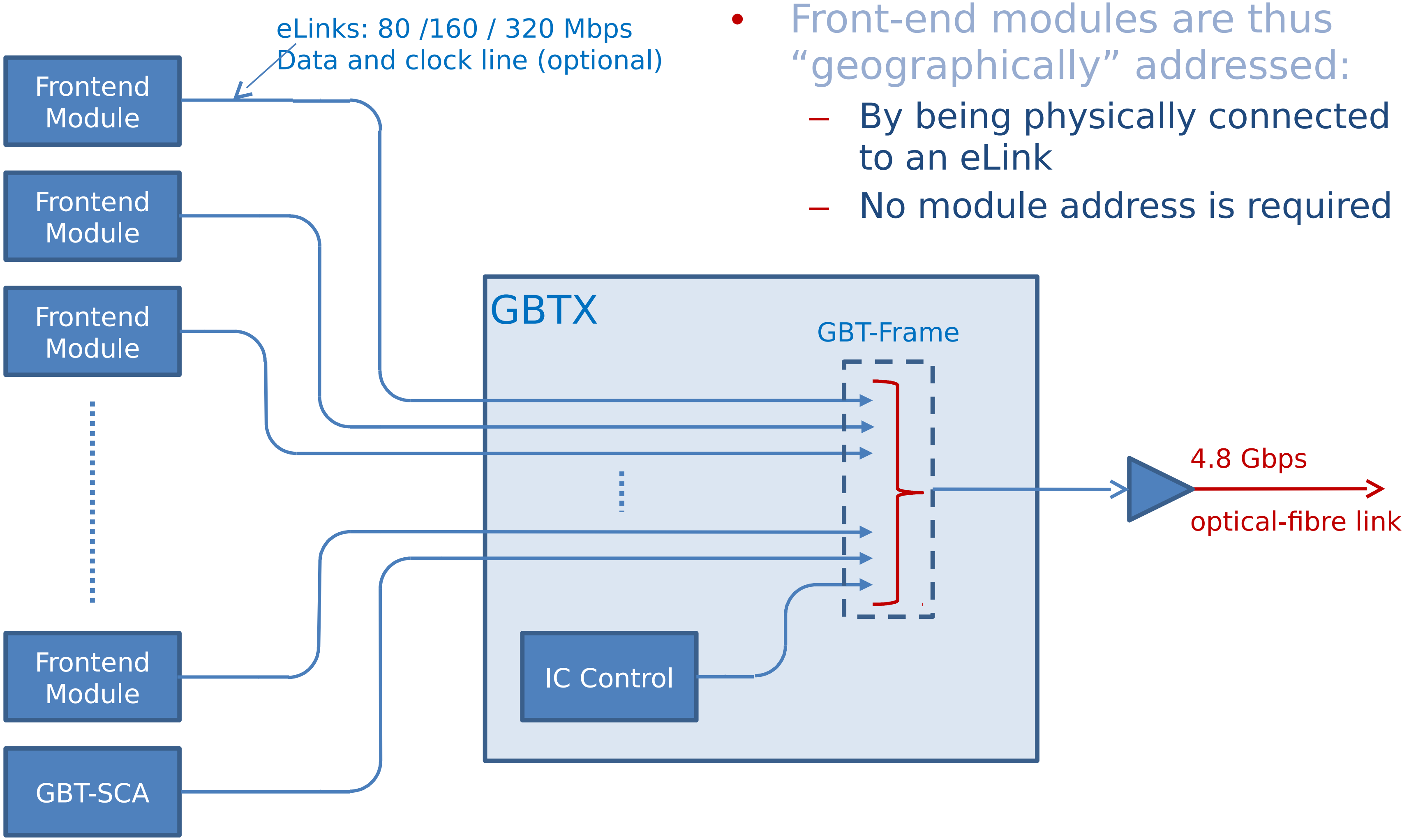


GBTX package



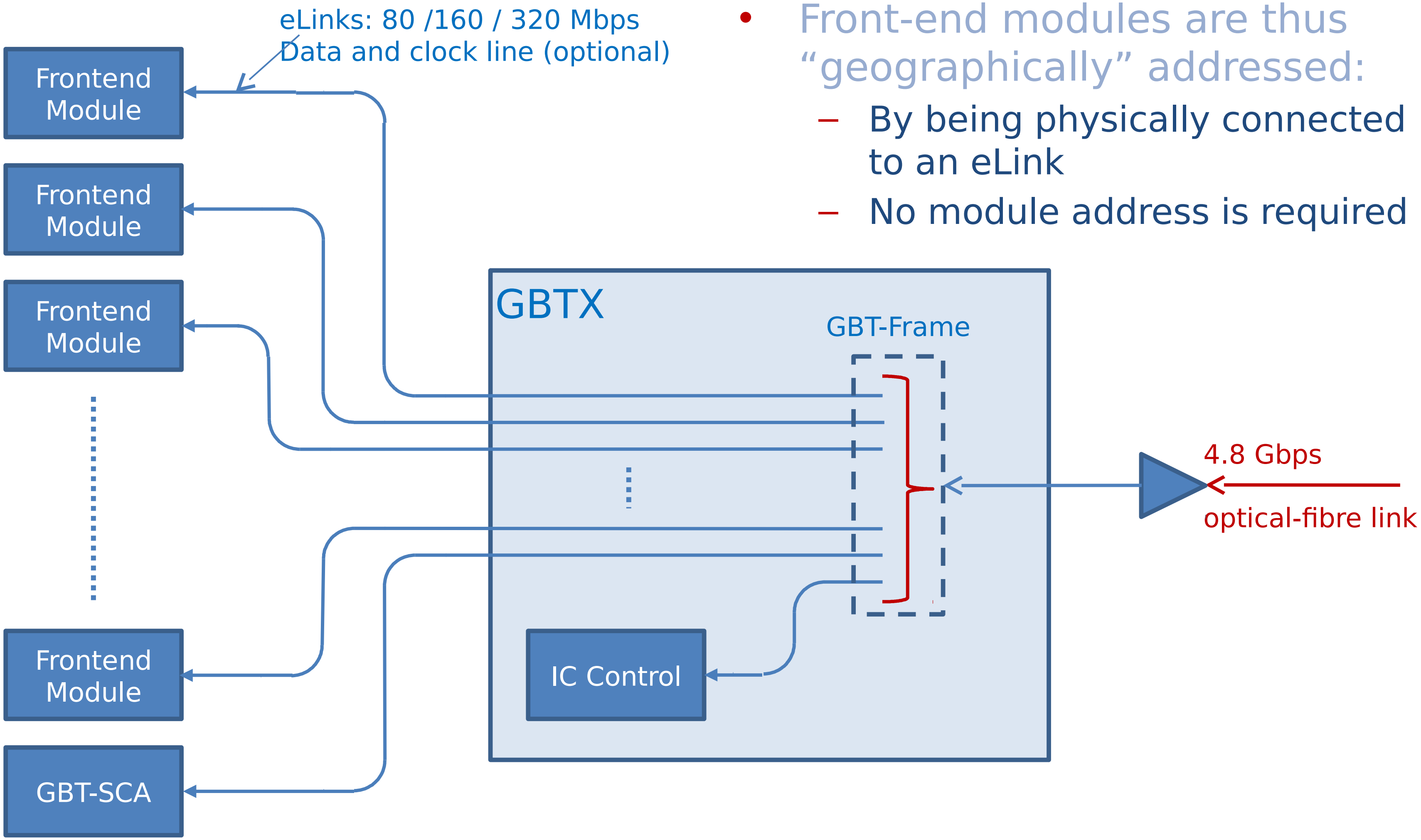
The GBTX up-link

- Each eLink is associated with a specific set of bits in the frame
- Front-end modules are thus “geographically” addressed:
  - By being physically connected to an eLink
  - No module address is required



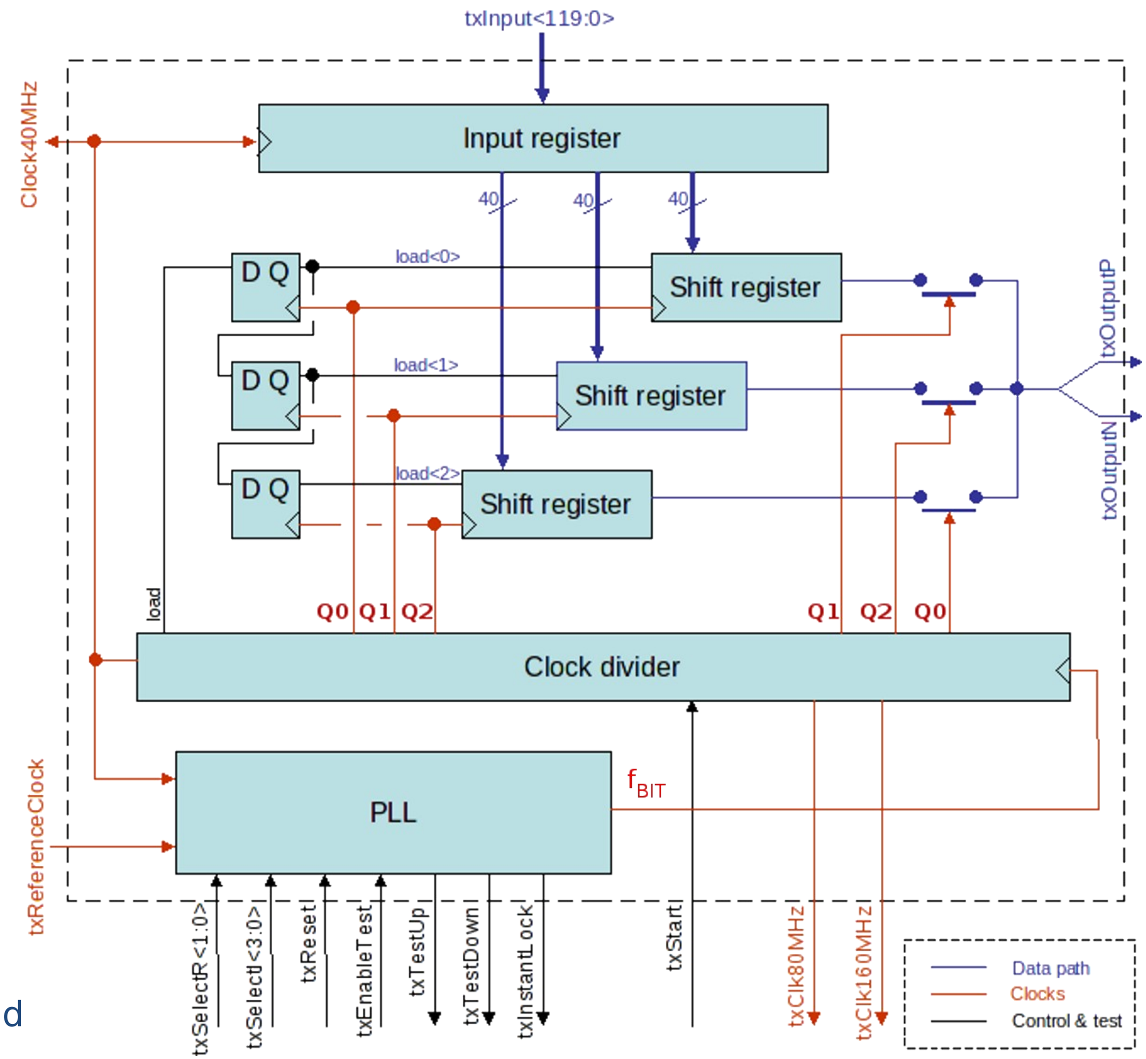
The GBTX down-link

- As for the up link, each eLink is associated with a specific set of bits in the frame
- Front-end modules are thus “geographically” addressed:
  - By being physically connected to an eLink
  - No module address is required

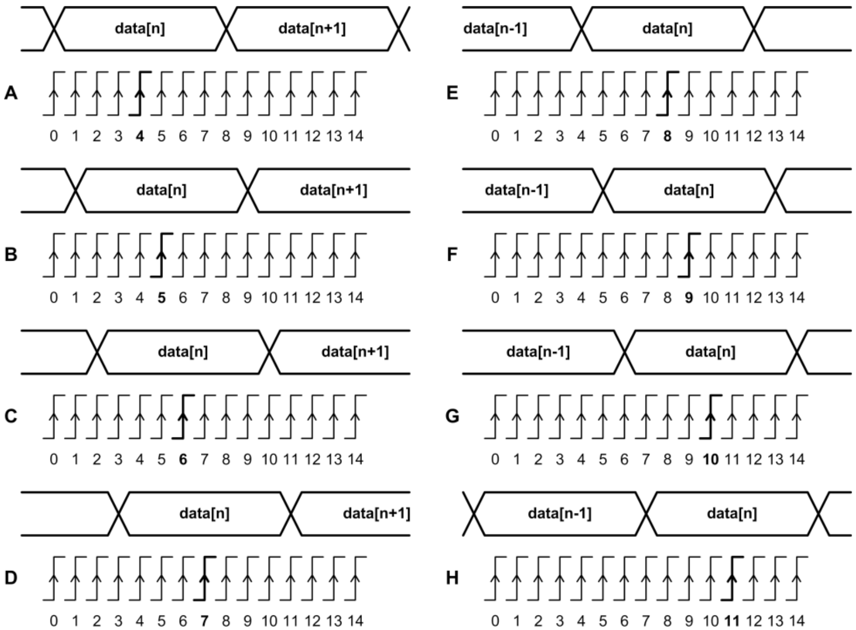


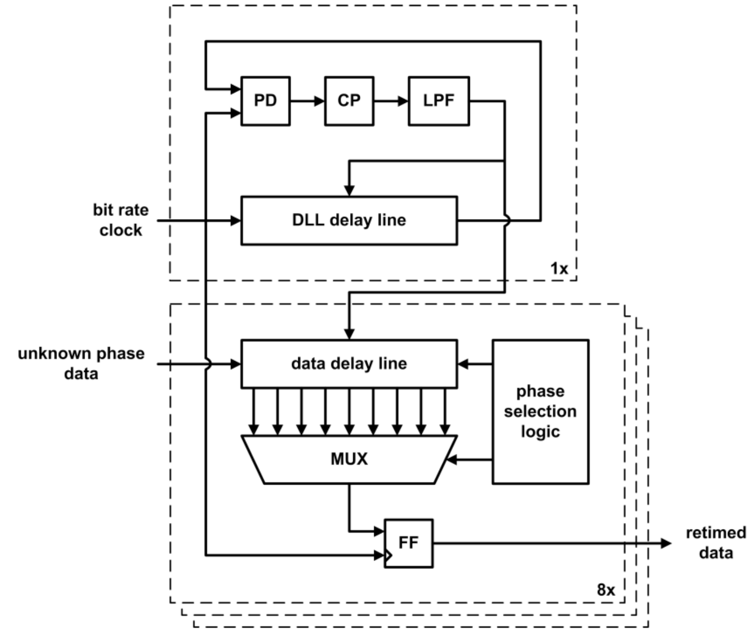
Serializer: Architecture

- Serializer:
  - 4.8 Gb/s
  - 120-bit shift register
    - 3 × 40-bit shift register (f=1.6 GHz)
    - 3-to-1 fast multiplexer (f=4.8 GHz)
- Data path:
  - No SEU protection
  - SEUs handled by the Reed-Solomon CODEC
- Clock divider:
  - Divide by 120
  - f = 4.8 GHz
  - Triple voted for SEU robustness
- PLL:
  - SEU hardened VCO
  - SEU hardened Clock Divider
    - Based on “custom” dynamic flip-flop
  - The PLL clock is used a the transmitter master clock (and not the reference clock)



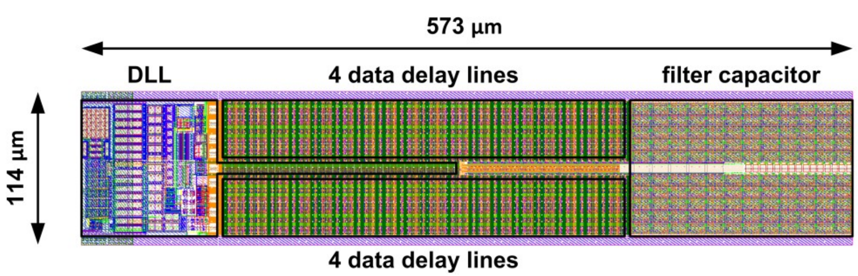
Phase Aligner





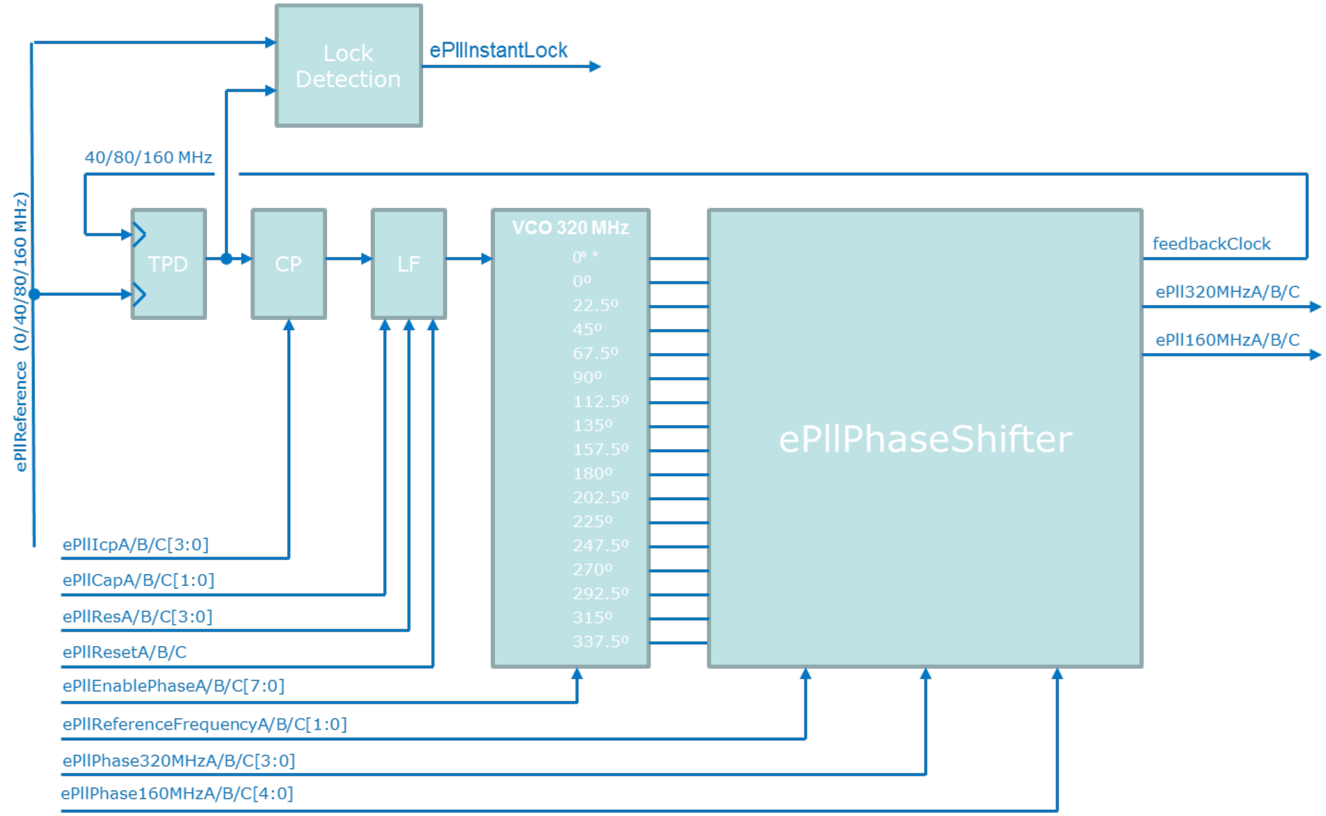
(The above picture is just for "easy representation". In reality the sampling clock phase is fixed and the data phase is adjusted.)

- The total delay line delay is equal to 7/4 T_{bit}
- The delay line is divided into 14 equal delay intervals $T_{bit}/8$
- In the automatic mode the circuit can tolerate jitter which is ±3/8 T_{bit}



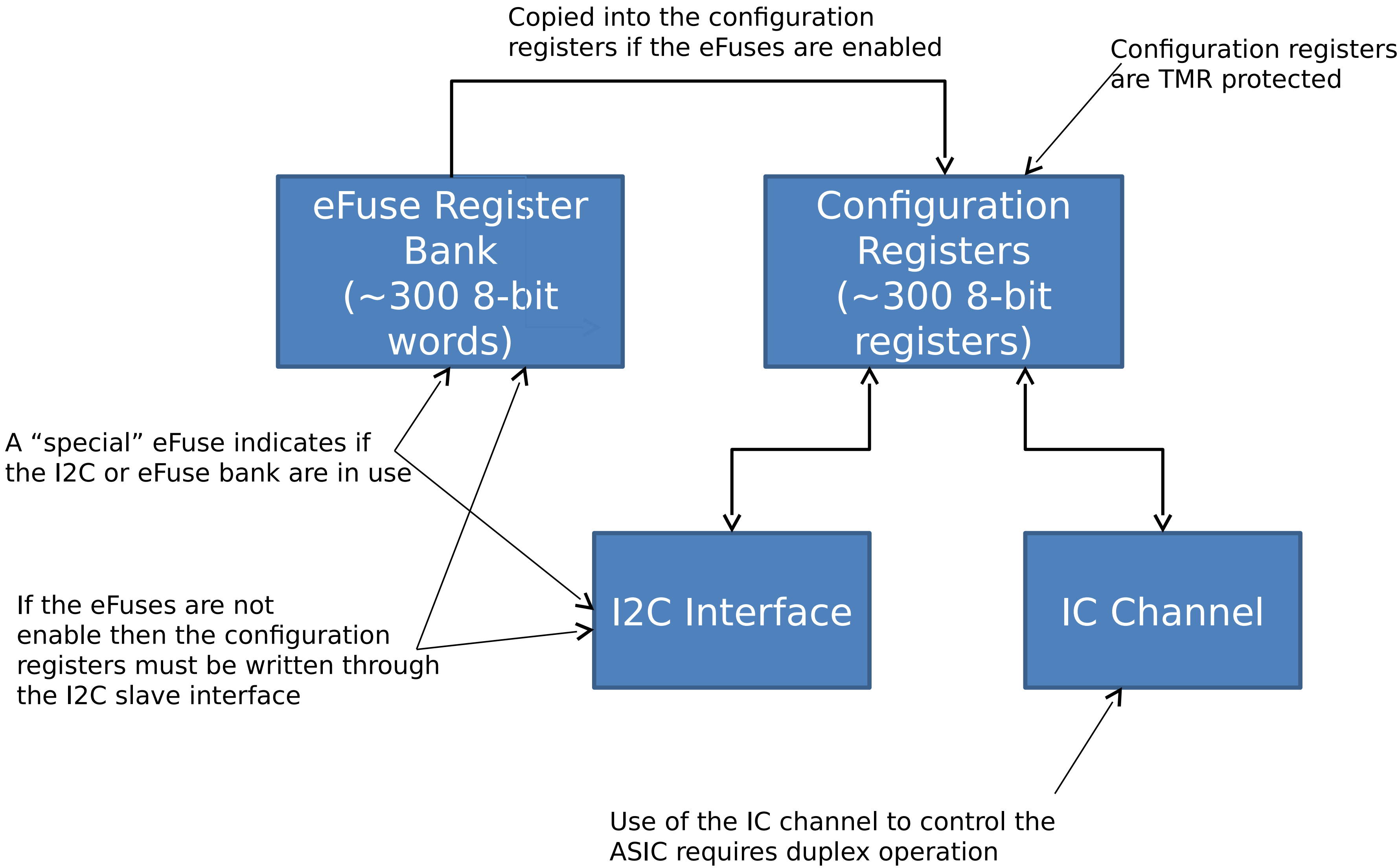
- One master DLL and eight replica delay lines
- Three modes of operation:
  - Static phase selection:
    - A system calibration must be done
  - Training with learned static phase:
    - 1st a training pattern is sent to the GBTX over the e-Link
    - 2nd after training the phase is fixed:
  - Automatic phase tracking:
    - No system calibration required
    - No need for DC balanced data
- Unused channels can be powered Off
- Power: 4 mW (for 8 channels)

ePLL

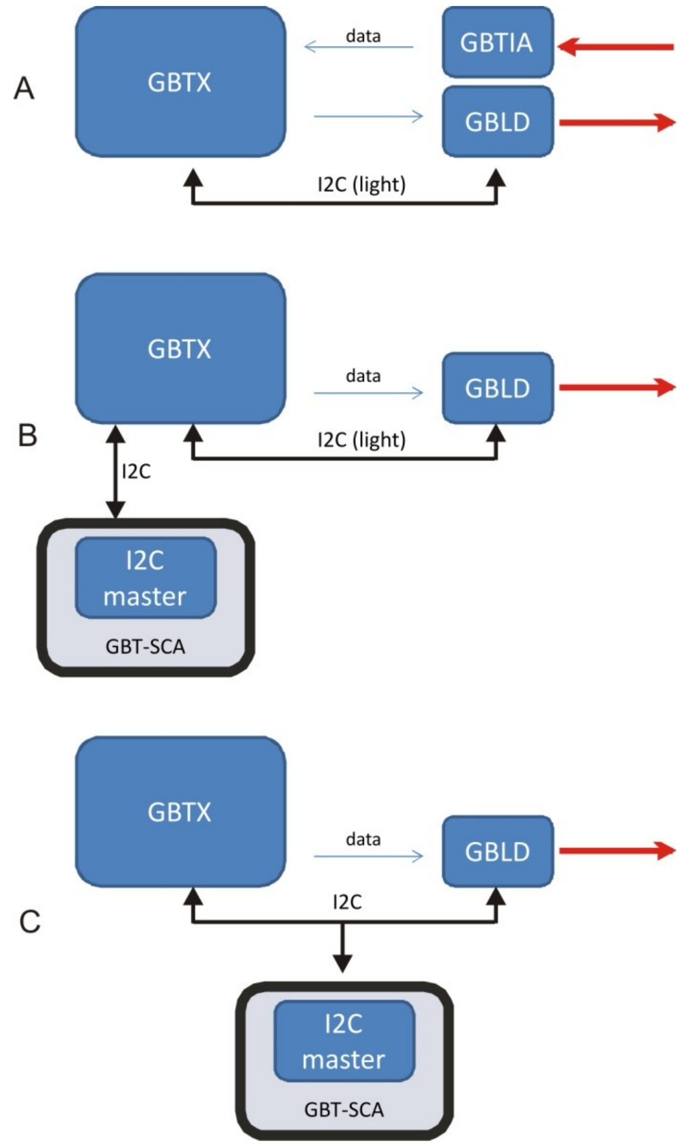


- Two ePLLs are used to generate the 160 and 320 MHz clocks needed to run the ePorts at 160 and 320 Mb/s respectively
- It allows phase shifting the internal clocks with 200 ps resolution
  - This is only for internal timing, can't be used for phase adjust of the eLink clocks
- The operation of the ePLLs is transparent to the users.
- The performance of the device is reflected on the ePort clocks at 160 and 320 MHz

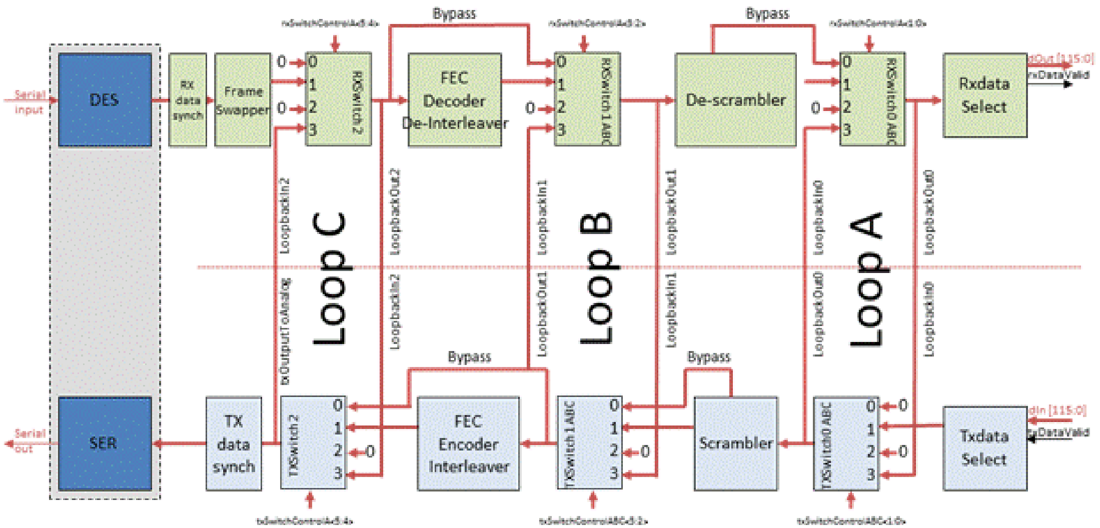
Controlling the GBTX



Interfacing with the GBLD



Built-in Test Features

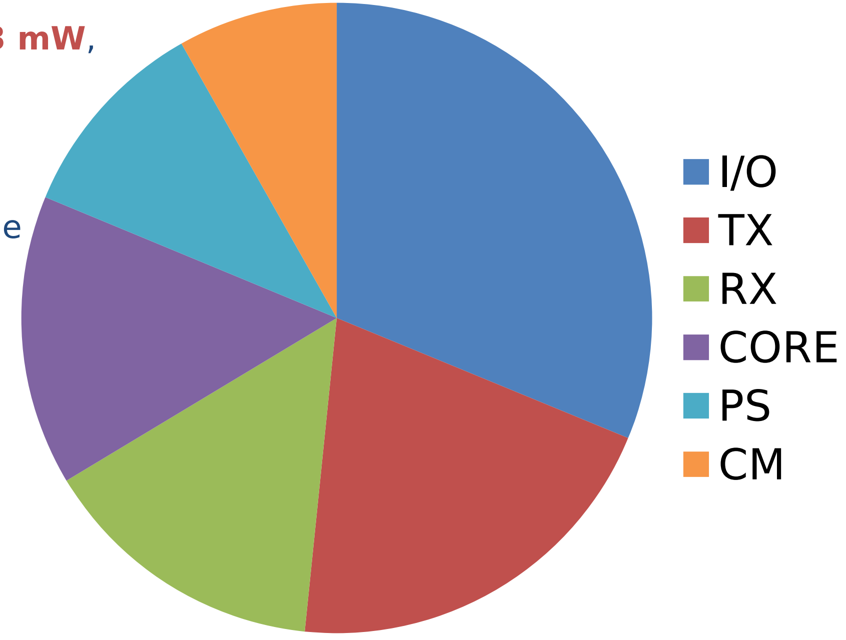


- A series of "loopbacks" allow to test the chip with different levels of depths:
  - Fast-serial to fast-serial
  - ePort to ePort
  - ePort – driver to ePort – receiver
- Tx high speed test patterns:
  - Header + AAA_BBBB_AAAA_BBBB_AAAA_BBBB_AAAA_BB
  - Header + counter[25:0] + counter[29:0] + counter[29:0] + counter[29:0]
  - Header + 4'h0 + prbs[6:0] x 16
- Rx bit error counter:
  - Works with the fixed pattern
- ePort patterns to validate the GBTX to Frontend timing

GBTX Power Consumption (1/2)

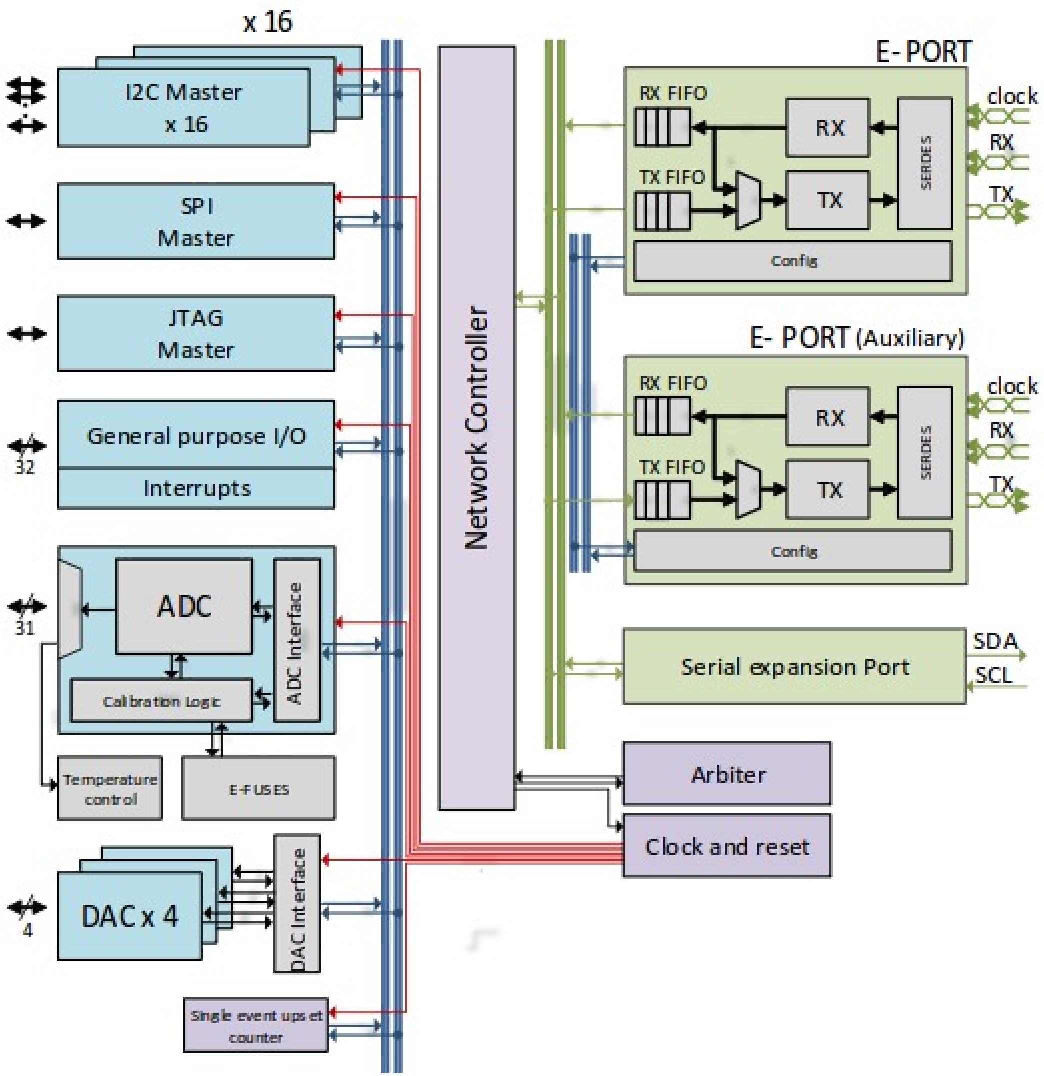
All power supplies voltages = 1.5V except EfusePower = 3.3V

- I/O (gndIO/vddIO):
  - P = 41 × 8.2 mW (Data SLVS-Tx) + 41 × 8.2 mW (CLK SLVS-Tx) + 41 × 0.65 mW (SLVS-Rx) = **698 mW**, I = 466 mA
- TX (gndTx/vddTx):
  - P = **456 mW**, I = 304 mA
- RX (gndRx/vddRx):
  - P = **330 mW**, I = 220 mA
- CORE (GND/VDD):
  - P = 305 mW (Standard cells) + 8 × 3.5 mW (Phase-Aligners) = **333 mW**, I = 222 mA
- PS (gndPS/vddPS):
  - P = 42 mW (PLL) + 8 × 16 mW (channel) + 8 × 8.2 mW (SLVS-Tx) = **236 mW**, I = 157 mA
- CM (gndCm/vddCm):
  - P = 2 × 41.5 mW (E-PLL) + 100 mW (XPLL) = **183 mW**, I = 122 mA
- E-Fuses (EfusePower):
  - P = **465 mW** , I = 141 mA
  - (Only during e-fuse programming. Not added to the total power figure below.)
- **Total:**
  - **P = 2.2 W**
  - (This is worst case power consumption: all functions ON, worst case simulations)



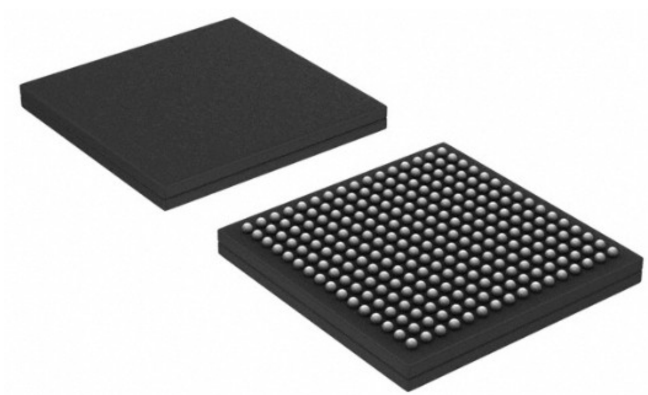
GBT-SCA

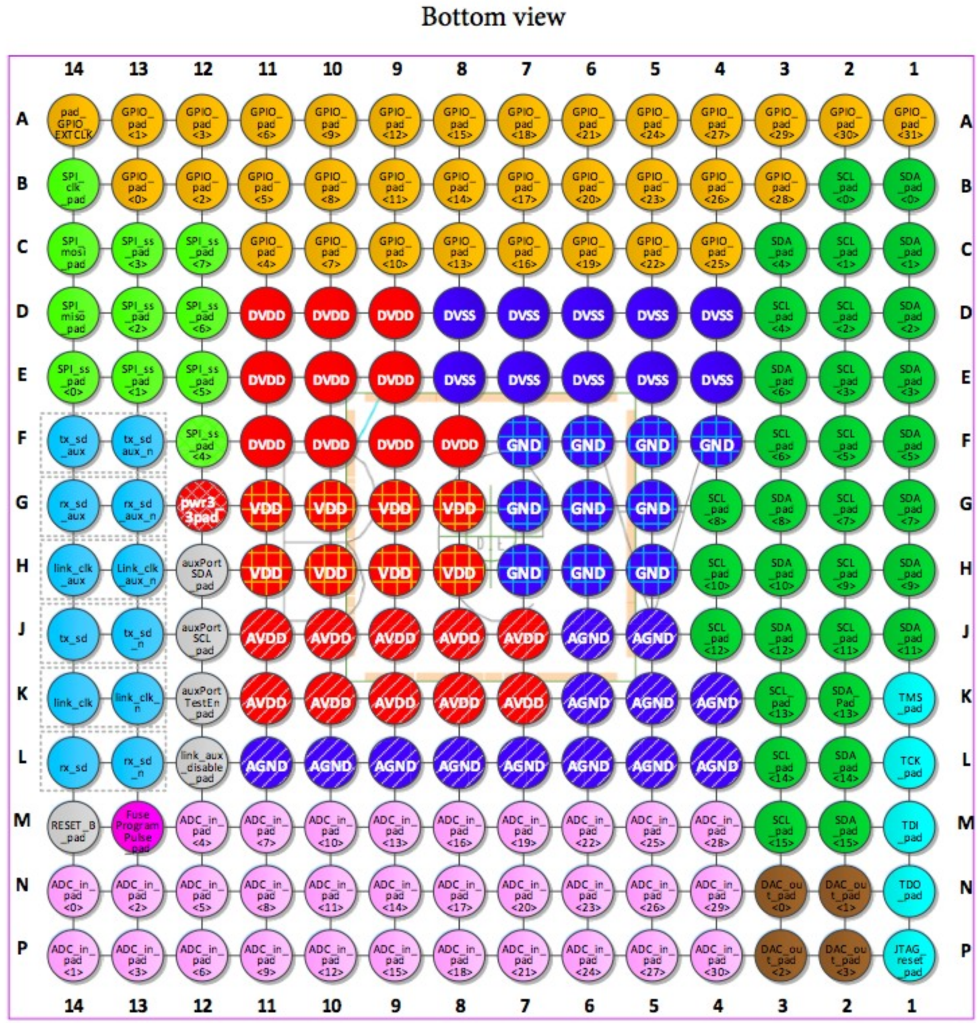
- ASIC dedicated to slow control functions
- System Upgrades for SLHC detectors.
- Replacement for the CCU & DCU ASICs (Communication Control Unit & Detector Control Unit in CMS).
- It will implement multiple protocol busses and functions:
  - I2C, JTAG, SPI, parallel-port, etc…
- It will implement environment monitoring and control functions:
  - Temperature sensing
  - Multi-channel ADC
  - Single channel DAC
- Flexible enough to match the needs of different FE systems.
- Technology: CMOS 130nm using radiation tolerant techniques.



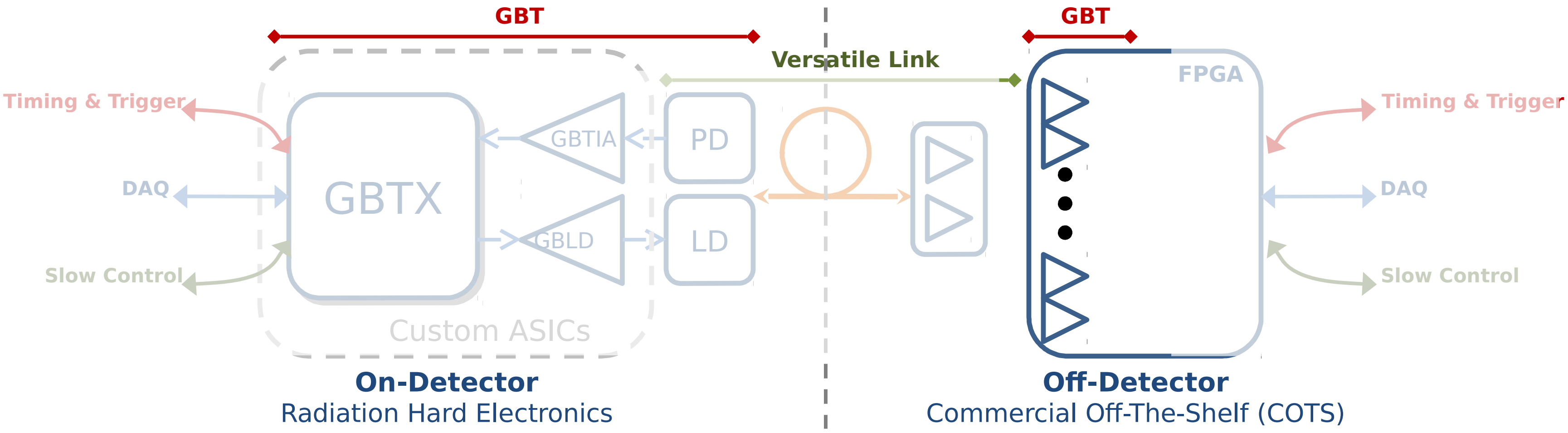
GBT-SCA final product package

- Package Type: LFBGA
  - Low Profile Fine Pitch BGA
    (Chip Scale Package)
  - Ball Pitch: 0.8 mm
  - Size: 12 x 12 mm
  - Height: 1.2-1.7 mm
  - Pin count: 196





GBT-FPGA



- Started in 2009 as a simple proof-of-concept,
  Code implemented on an Altera SIIGx and a Xilinx V5
  Interoperability validated, link characterized
  Presented at TWEPP2009
- Core made available, studies conducted on determinism, used to test the GBT prototype
-
- Many requests from various teams and for various usages
- Project launched in 2013, Manoel started to work on it extensively

GBT-FPGA 2015 status

- Available Package on svn: https://svn.cern.ch/reps/ph-ese/be/gbt_fpga
  - Core code (VHDL)
  - Example Designs
  - Documentation & tutorials
  - TCL Scripts
  - Targeting
    - Xilinx : Kintex 7 (FC7, KC705) , Virtex 7 (VC707), Virtex 6 (GLIB)
    - Altera: Cyclone V (SAT, Cyclone V GT Devkit), Stratix V (AMC40), Arria V GT (coming)
  - Additional Unsupported Cores (GBTx and SCA slow control)
- Website: https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx
- egroup : GBT-FPGA-users
- 120 users
  - Some of them contributing very actively

Engineering Run

- Tapeout:
  - June 2014
- Three metalization options
  - GBTX:
    - LM 6 – 2, C4
  - GBTIA:
    - LM 6 – 2, WB
  - GBLD & GBT – SCA:
    - DM 3 – 2 – 3, WB
- Wafers:
  - October & November 2014

Available Quantities and Status

- GBTIA:
  - Chips/wafer: 2144
  - 4 wafers (8576 chips)
  - Chips will be wafer probed at CPPM
- GBLD:
  - Chips/wafer: 1340
  - 3 wafers (4020 chips) wafers shared with GBT – SCA
  - 2650 parts packaged by NovaPack
  - A small sample already tested
- GBTX:
  - Chips/wafer: 536
  - 4 wafers (2136 chips)
  - 180 parts packaged by ASE
  - All packaged parts tested (yield 97.8%)
- GBT – SCA
  - Chips/wafer: 268
  - 3 wafers (804 chips) wafers shared with GBLD
  - 208 parts packaged by NovaPack
  - First samples to be tested soon

ASICs Production

- Production wafers:
  - Lead time 4 months
    - Earliest availability: June/July 2015
  - Still to be ordered
- Quantities:
  - GBTX: ~60k
  - GBLD: ~60k
  - GBTIA: ~15k
  - GBT – SCA: ~15k
- (GBTX) Crystal production:
  - Pre-production: March 2015 (contract + 6 weeks)
  - Production follows in batches of 15k
  - Complete October 2015 (contract + 34 weeks)
- GBTX packaging:
  - To start June/July
- GBLD packaging:
  - Start June/July 2015
- GBTIA:
  - Integrated in the VTRX

Cost for the User

- GBTX
  - 50 CHF
- GBT-SCA
  - 24 CHF
- VTRX (MM)
  - 200 CHF
- VTTX (MM)
  - 150 CHF

Users and Quantities

GBT Chipset & VL Components Needed Quantities (1 Dec. 2014)

(Options)

	TOSA		ROSA		Latch		VTRx		VTTx	GBTX	GBT-SCA	GBLD	GBTIA
User	**SM**	**MM**	**SM**	**MM**	**SM**	**MM**	**SM**	**MM**	**MM**				
LHCb		16000		2000		9000		2000	7000	14000	6000	16000	2000
CMS HCAL	200	5690	200	270	200	2980	200	270	2710	5700		5890	470
PixPhase1	3000											3000	
ATLAS SmallWh		3500		1200		2350		1200	1150	2300		3500	1200
ATLAS SmallWh option										*1200*			
ATLAS LArg		600		600		600		600		600		600	600
ATLAS LArg Option		*6000*				*3000*			*3000*	*6000*		*6000*	
ALICE		10000		3600		6800		3600	3200	10000	5000	10000	3600
BE-BI-BL	500		500		500		500					500	500
BE-BI-QP	500		500		500		500					500	500
BE-CO-FE													
CBM@FAIR		6700		2500		4600		2500	2100	6700	2500	6700	2500
PANDA@FAIR										250			
Total	***4200***	***42490***	***1200***	***10170***	***1200***	***29330***	***1200***	***10170***	***16160***	***39550***	***13500***	***52690***	***11370***
Option	***0***	***6000***	***0***	***0***	***0***	***3000***	***0***	***0***	***3000***	***7200***	***0***	***6000***	***0***
Total with option	***4200***	***48490***	***1200***	***10170***	***1200***	***32330***	***1200***	***10170***	***19160***	***46750***	***13500***	***58690***	***11370***

The Low-power GBT (LpGBT)

Low Power Dissipation and Small Footprint:

- Target: 500 mW
- (GBTX: 2W)
- Critical for pixel detectors
- Critical for tracker/triggering detectors

- Bandwidth:
  - Low-Power mode
    - 2.56 Gb/s for the optical down link
    - 5.12 Gb/s for the optical up link
  - High-Speed mode:
    - 2.56 Gb/s for the optical down link
    - 10.24 Gb/s for the optical up link

- e-Links:
  - Down-links:
    - 80, 160 and 320 Mb/s
  - Up-Links, Low-Power Mode:
    - 160, 320 and 640 Mb/s
  - Up-Links, High-Speed Mode:
    - 320, 640 and 1280 Mb/s

- Functionality:
  - “Replica” of the GBTX
  - Reduced subset of the GBT Slow Control Adapter (GBT – SCA) functionality will be included