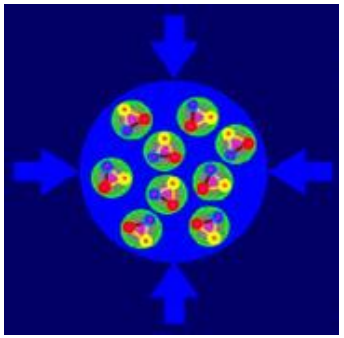
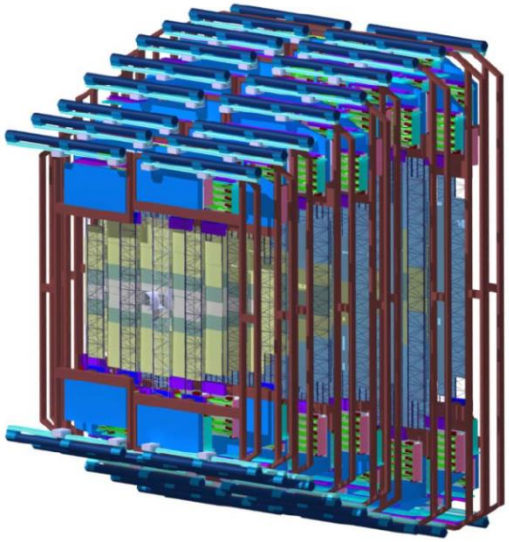


CBM

STS



Common CBM ROB Prototype

with GBTX and Versatile Link for STS-XYTER, GET4 and SPADIC Readout Chains

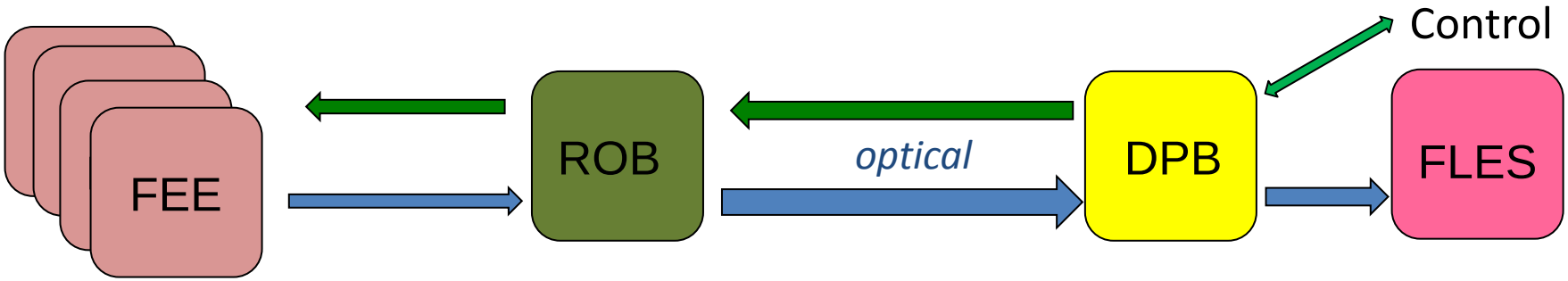
CBM Panda DAQ Session

09. April 2015

J. Lehnert

GSI

CBM Readout Chains



Frontend Electronics (FEE)
… with *detector specific* ASIC
(or FPGA… → J. Michel)
based functionality

Readout Board(s) (ROB)
similar functionality
- data aggregation from FEE links
- electrical to optical interface
- FEE control path
- clock distribution and synchronization

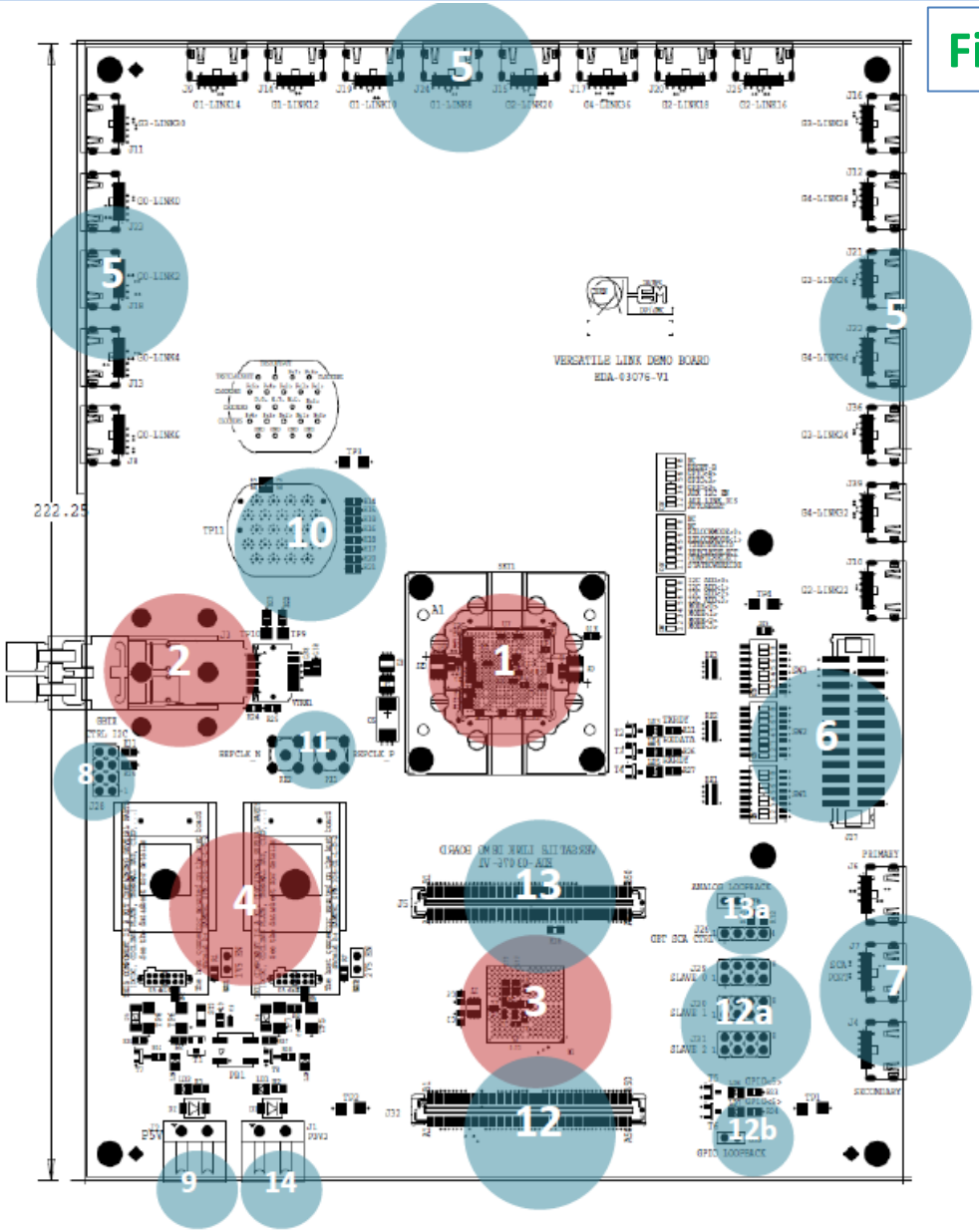
- located close to FEE

Data Processing Board (DPB)
→ W. Zabolotny
common CBM DAQ layer:
- FPGA based
  - data formatting
  - preprocessing
- timing and control interfaces
- interface to FLES (FLIB)
- in CBM building (experimental hall or surface)

⇩

CERN GBT based solution

GBT Step1: CERN Demonstrator Board VLDB



First tests with GBT devices:

1. Single GBTx (& Socket)
2. Single VTRx
3. SCA
4. DC-DC (FEASTMP) 1.5V and 2.5V
5. GBTx FE E-links
6. GBTx and SCA configuration pins
7. GBTx and SCA SC e-link
8. I2C control bus & fuse burning bus
9. General power plug
10. GBTx TTC Clk outputs
11. GBTx Ref Clock Input
12. SCA Digital connector
    a. SCA I2C/GPIO connectors
    b. SCA GPIO loopback
13. SCA Analog connector
    a. SCA DAC/ADC loopback
14. 3.3V power plug for fuse burning

CERN VLDB - Status

- first **3 prototype boards:**
  - tests finished
  - design update ongoing
- **(First) production batch**
  - probably will already include SCA
  - available for users in June?

- Auxiliary boards/tools:
  - SCA daughterboards (digital, analog functionality)
  - E-Link FMC board
  - USB-I2C dongle
    - I2C control of GBTx
    - Fuse programming

GBT Step2: Common CBM ROB Prototype

Next step for CBM after tests with VLDB:
Common CBM GBT prototype board (C-ROB)

- **Full** GBTx, SCA and Versatile Link **functionality** required for readout and control of all ASIC based CBM readout chains
  - STS: (STS)CBM-XYTER
  - MUCH: CBM-XYTER
  - TRD: SPADIC2
  - TOF: GET4
- **FMC connector** with all **frontend connectivity** (GBTx E-Links and required SCA functionality)

  → projects are free to connect to any FEE prototype or series interface, but will need to build individual interface FMCs

Detector Requirements

	STS	TOF	TRD
Readout	40 E-Links IN at 320 MHz 3 GBTX	14 E-Links IN at 320 MHz 1 GBTx	42 E-Links IN at 320 MHz (for prototype testing) 3 GBTx:
	Widebus mode for uplink		
Control/Clock	5 E-Link OUT (for up to 5 FEBs)	4 E-Link OUT (for 4 TOF_ROBs)	6 E-Link OUT
	5 user clocks (for up to 5 FEBs)	4 user clocks (for 4 TOF_ROBs)	6 user (or E-Link) clocks
SCA		JTAG	
		12 GPIO	
	I2C for GBTx control		I2C for GBTx control
	ADCs for slow control on ROB (voltages, temperature)		

Red: frontend interface

Further Requirements

"General Purpose": to be able to use the prototype boards for some generic slow control tests and applications

- SCA
  - few I2C
  - few ADCs
  - DACs
  - …
- Full SCA functionality on second FMC? → no

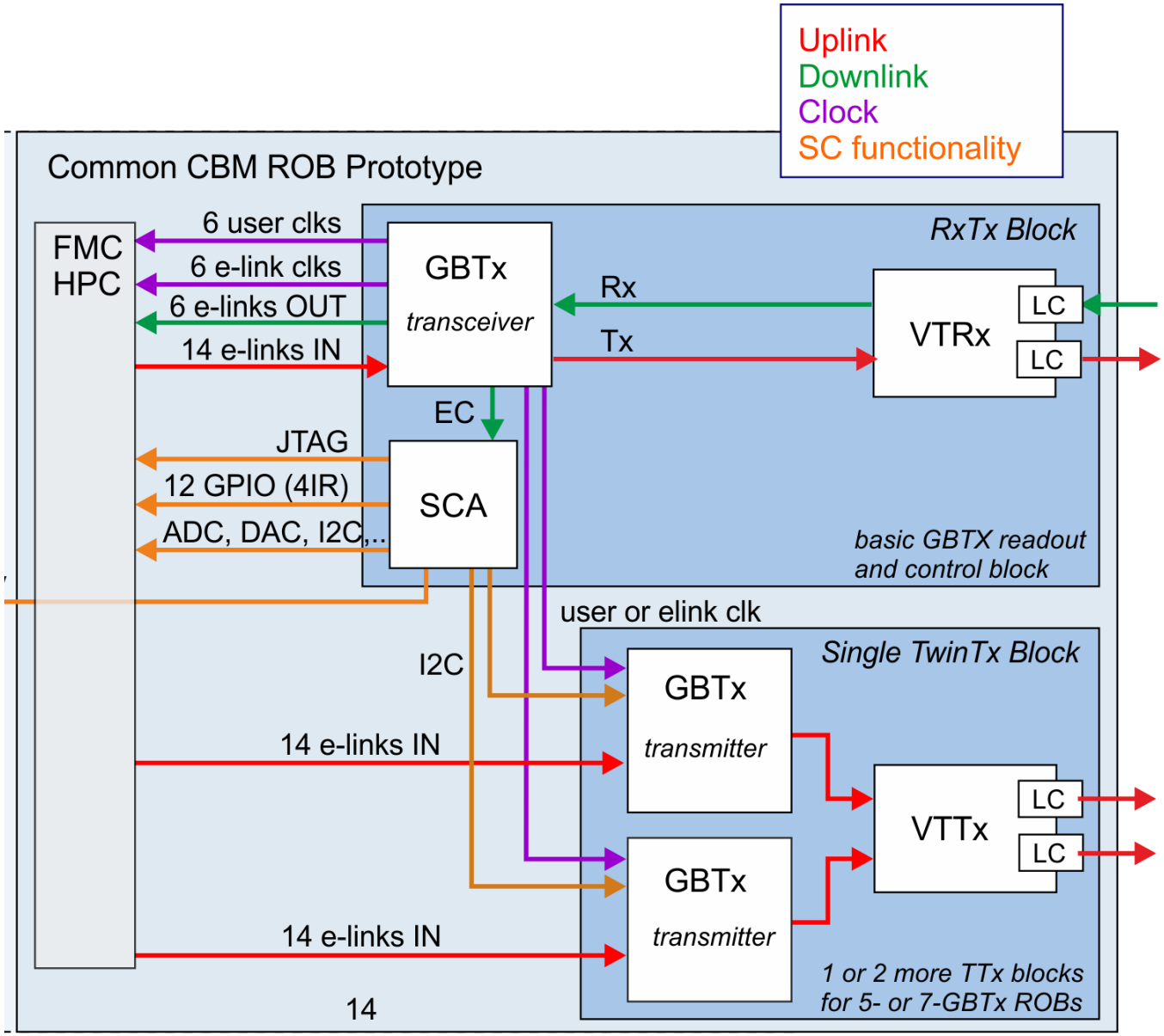
From VLDB to C-ROB

extensions to VLDB functionality
reduced functionality wrt VLDB

- 1 GBTX → **3** GBTX
- 1 VTRx → 1 VTRx + 1 **VTTx**
- Multipurpose SCA
  → SCA for GBTx control (onboard)
  - 1 GBTx ("master") connected to VTRx controlled via IC channel
  - 2 **GBTx** connected to VTTx are **controlled via I2C**
    (from master GBTx' EC port via SCA's I2C master interfaces)

  → subset of SCA slow control functionality
  - GPIO and JTAG for TOF
  - Selection of multipurpose functionality: ADCs, DAC, I2C,..
- 20 full e-ports on HDMI connectors
  → E-Port and Clocks on **FMC connector**
  - **14 + 14 + 14 E-ports (IN)**
    - Full readout bandwidth for 320 Mbps E-links
      both with widebus and GBT (10+10+10 ports) frames for the uplink
    - Subset of E-links at 160 Mbps or 80 Mbps (for testing)
  - few E-ports (OUT)
  - few E-clks and **user clocks** (phase adjustable)

Common ROB Block Diagram



Common ROB - FMC

Device	Functionality	**Units Connected to FMC**
GBTX Master	E-Link IN	**14**
	E-Link OUT	6
	E-Link Clk	6
	User Clk	6
Slave GBTX 1/2	E-Link IN	**14/14**
	E-Link OUT	0
	E-Link Clk	0
	User Clk	0
SCA	GPIO	12
	JTAG	1
	ADC	8
	DAQ	2
	I2C	4
	SPI	1
	Secondary E-Port	1
		164 Signals

Fits on single HPC FMC

Common ROB – Prototype Character

Keep some flexibility (and variability) in configuration and usage options

- for the different readout chains
- for additional testing

e.g.

- GBTX modes (transceiver type; frame type)
- E-Fusing option
- powering (FEAST MP onboard?)
- E-link clocks vs phase adjustable user clocks
- Misc signals: TxDataValid, GPIO external clock,…

Test and slow control connector with e.g.

- Reset
- Rx/TxRdy
- RxDataValid
- device test signals?
- …

The above items -and others- have to be finally agreed upon…

Current Status

Common ROB

- basic detector requirements collected
- general board concept
- details to be finalized (e.g. required GBTx configuration options,…)
- start of schematics with revised VLDB design from CERN
- layout after tests with VLDB
- Goal: readout chain (STS) with C-ROB end of 2015

GBTx/Versatile Link

- GBTx and VL components ordered
  - Pre-production devices available ~summer 2015
  - Full production run planned for second half of 2015

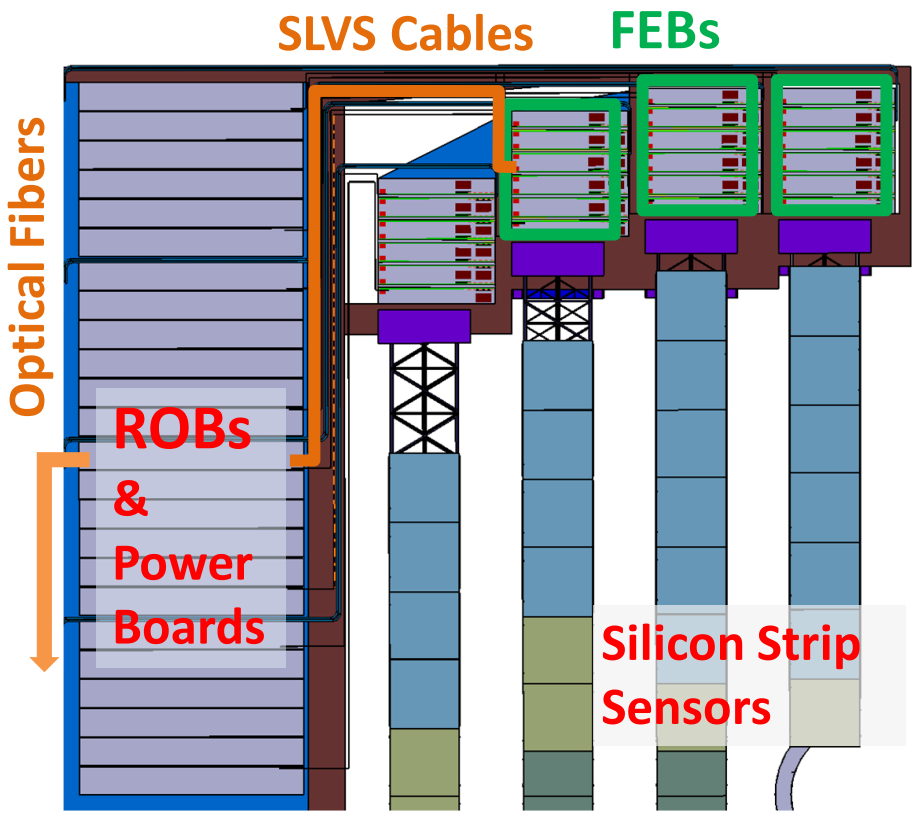
GBT Step(s) 3: Detector Specific ROBs - STS

For STS: fully featured **STS ROB-3** prototype

Challenges

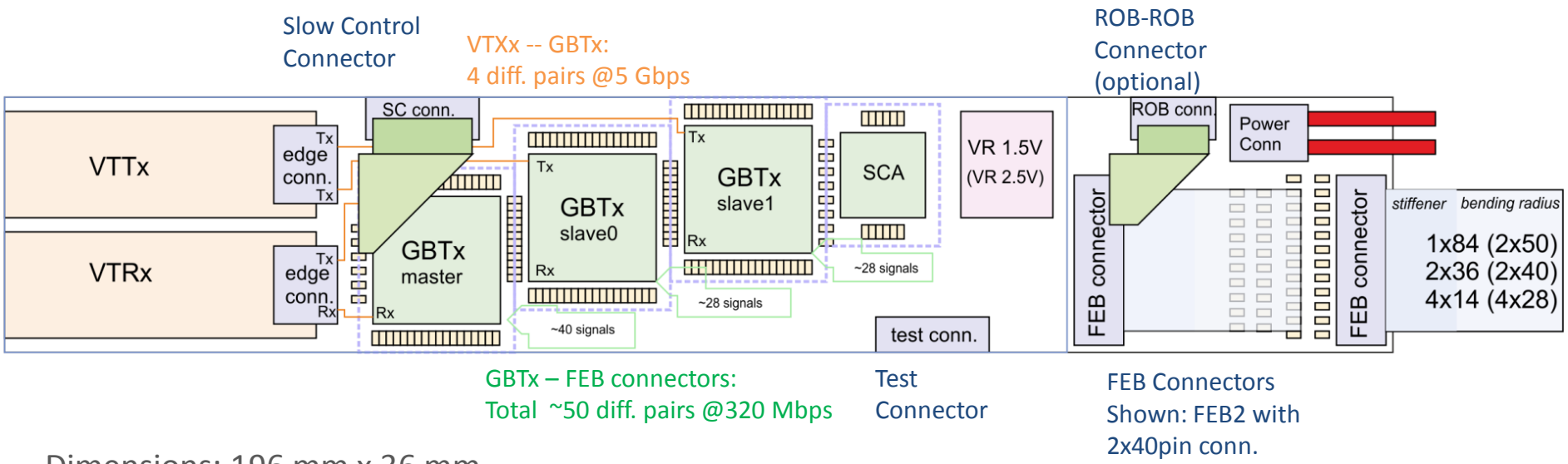
- **Radiation**
  - up to 100krad and $5x10^{13}$ n_{eq}/cm^2 in ROB locations over expected total operation time
- **Magnetic Field**
  - operation inside 1T dipole magnet
- **Space**
  - ROB size: approx. 83mm between side cooling plates of adjacent units
  - FEB connections: routing volumes, connector size
- **Cooling**
  - sensors operated at <= -5° Celsius
- **Powering Scheme**
  - FEBs operated at individual sensor potentials
    → AC coupling of FEB-ROB e-links

Quarter Station (every 2nd ladder)



STS ROB Prototype

Possible STS ROB-3:



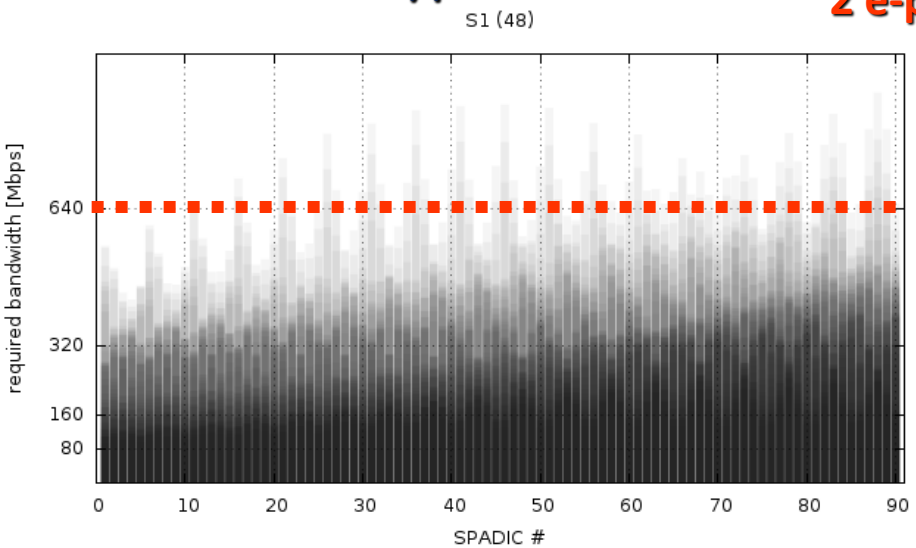
Dimensions: 196 mm x 36 mm

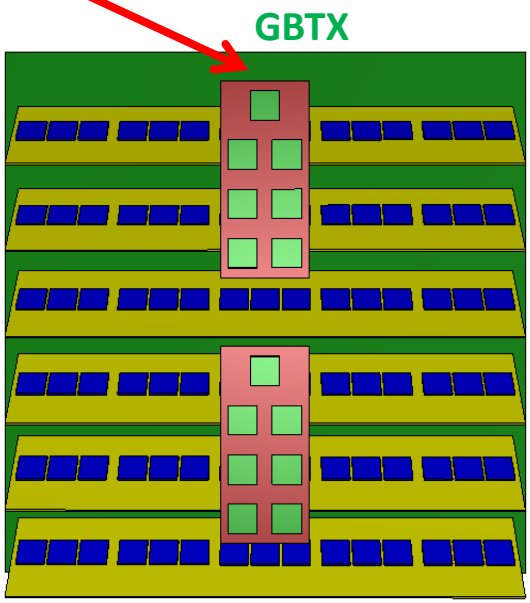
TRD ROBs

One or more **ROB-3, ROB-5 or ROB-7** on each detector module

Example:
TRD Module type 1 data rate

2 e-ports





Michael Krieger

90 Spadics a 2 e-ports = 180 e-ports
2x GBTx ROB 7 = 2x 7x 14 = 196 e-ports

usage 92%

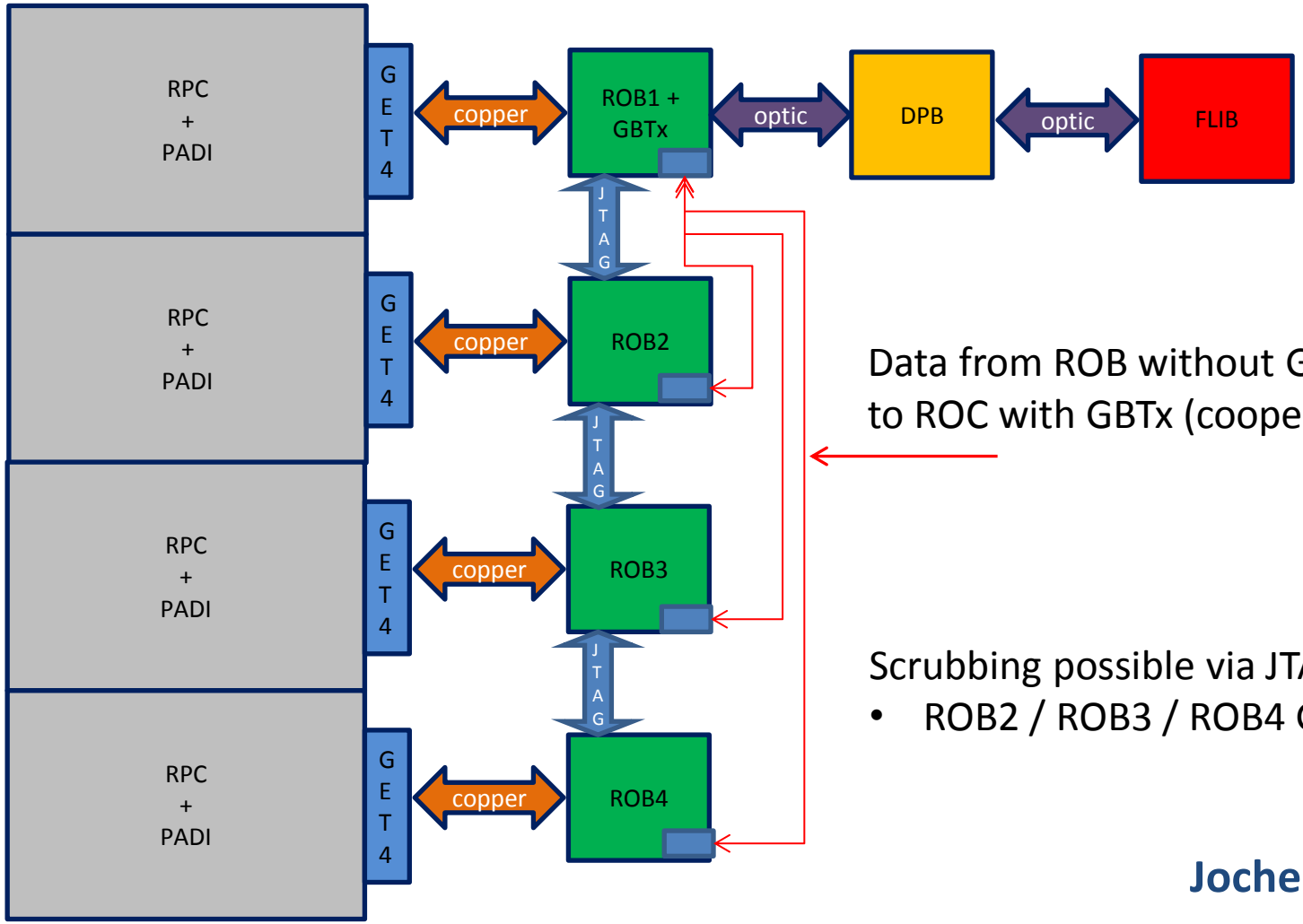
David Emschermann

TOF Readout with GBTx

Simple Block diagram for 1280 Channel, 1GBTx for 4 ROBs

- GBTx equipped on one ROB
- JTAG chain for scrubbing up to 4 ROB

→ Andrei Oancea



Data from ROB without GBTx to ROC with GBTx (cooper)

Scrubbing possible via JTAG

- ROB2 / ROB3 / ROB4 GBTx not equipped

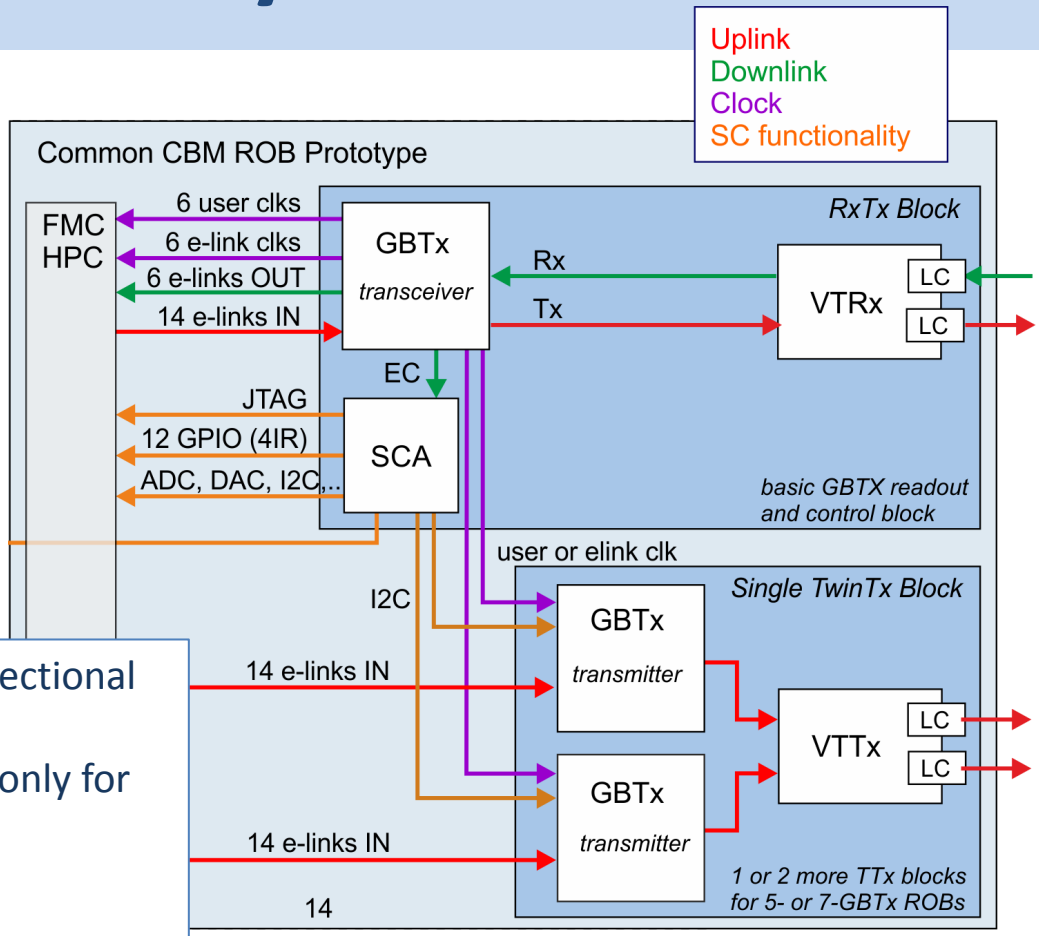
Jochen Fruehauf

Summary

CBM common ROB-3:

- Intermediate prototype ROB between VLDB and detector specific ROBs
- full functionality for all readout chains

- specification phase
- design to start soon
- boards available end of 2015



- 1 GBTx with 1 VTRx as transceiver for bidirectional communication
- 2 GBTx with 1 VTTx as transmitter (uplink only for data readout)
- Frontend connectivity
  - 42 E-Links IN with up to 320Mbit/s
  - Few(6) E-Links and Clks OUT
- Optical interface
  - 1 downlink (control); 3 uplinks (readout)
- Selected slow control functionality from SCA chip
  - I2C, JTAG, GPIO, ADC, DAC,
- FMC connector as FE interface

Backup

STS Readout Chain

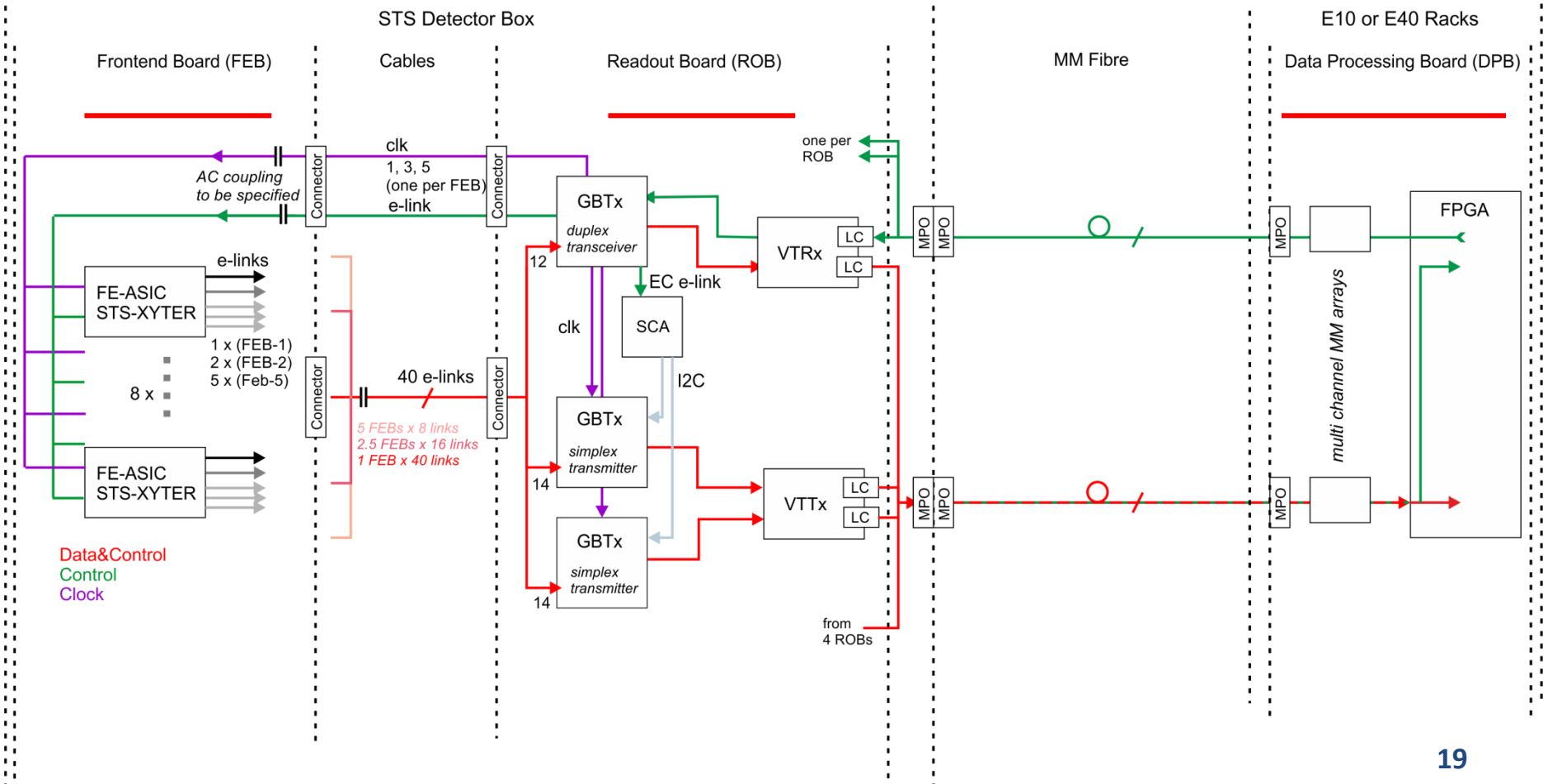
FEB
8 STS-XYTER

Electrical Interface
SLVS/LVDS
10-42 pairs/FEB

ROB
GBTx / VL

Optical Interface
4 MM fibers /ROB

DPB



STS Readout Board (ROB)

1 master GBTx connected to 1 VTRx transceiver
- Slow control, clock distribution
- Data readout

2 slave GBTx connected to 1 VTTx (twin transmitter)
- Data readout, control responses

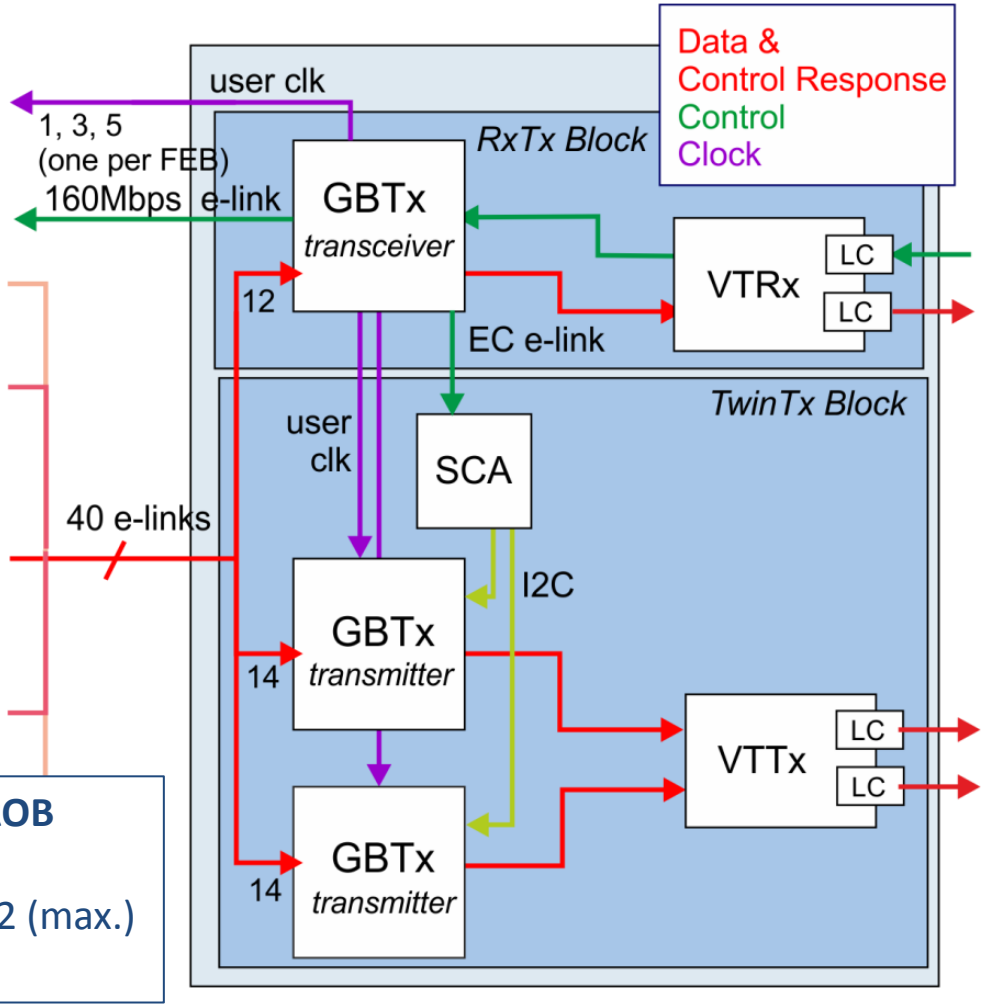
1 SCA as slow control interface from master to slaves

Frontend Side

Clock and Slow Control:
- single clock and slow control downlink to each FEB (160 Mbps)
- multidrop to 8 ASICs

Input from FEBs:
- GBTx **wide bus** mode
- 3x14 = **42 e-links @320Mbps**
- input bandwidth 13.44 Gbps

Minimized number of FEB-ROB connections:
on FEB side from 8+2 to 40+2 (max.) differential pairs



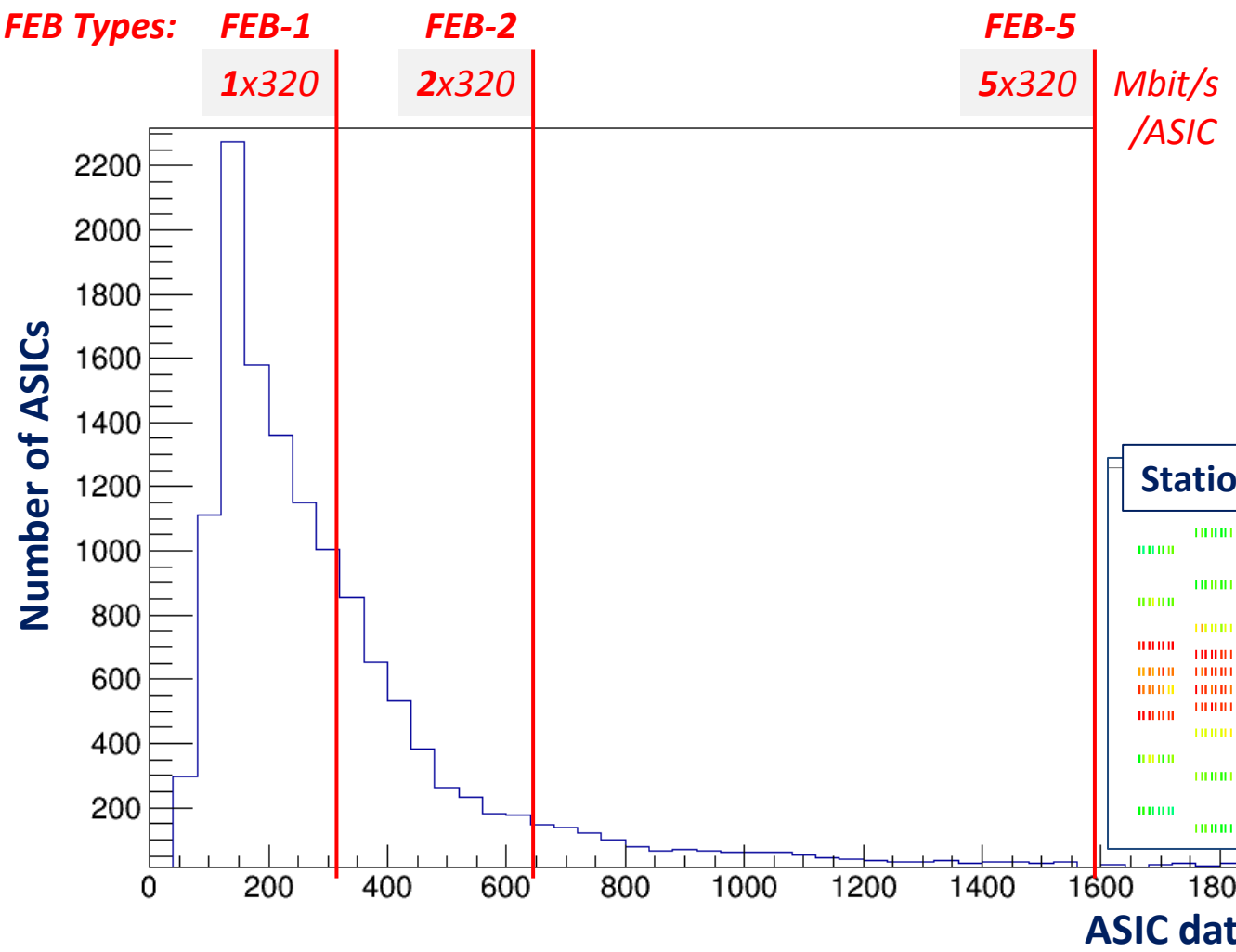
Backend Side

Output to DPBs:
- 1 VTRx, 1 VTTx
- **1 downlink**
- **3 uplinks**
- user bandwidth 3x4.48 = **13.44 Gbps**

SCA:
- I2C masters for slave GBTx control
- additional slow control features: temperature, voltage

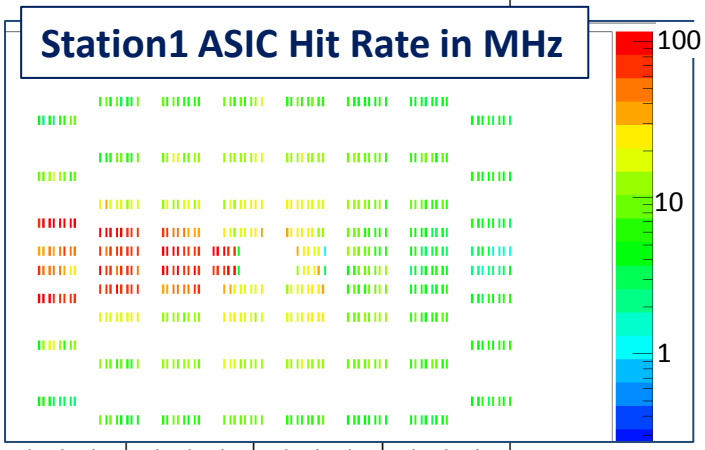
ASIC Data Volume and Readout Links

- use fastest E-Links (320 Mb/s)
- configurable number of E-Links in each ASIC: 1,2,5

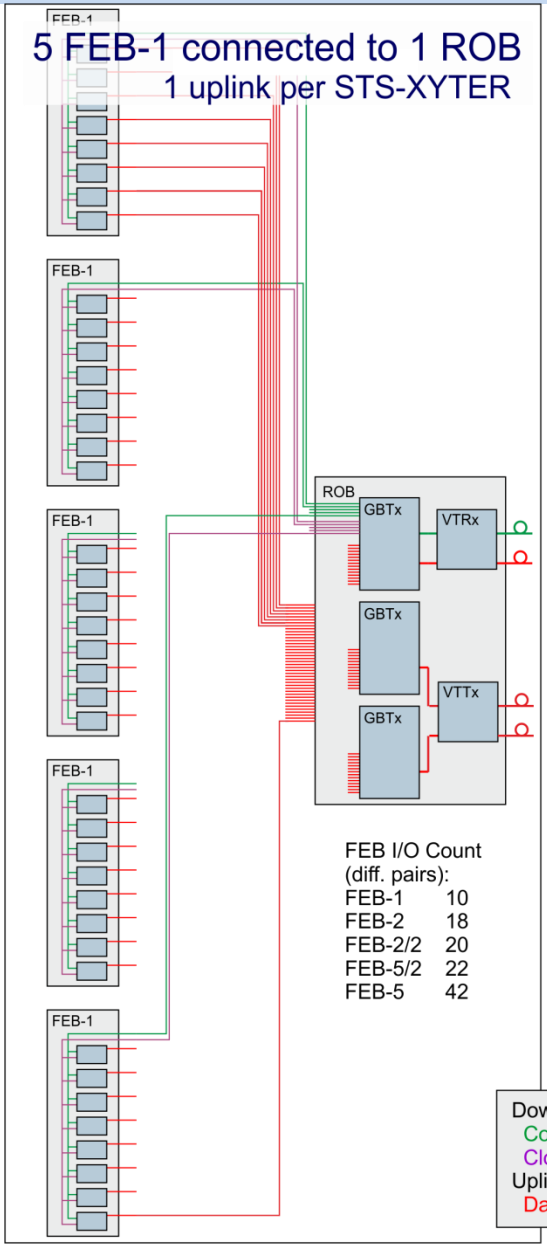


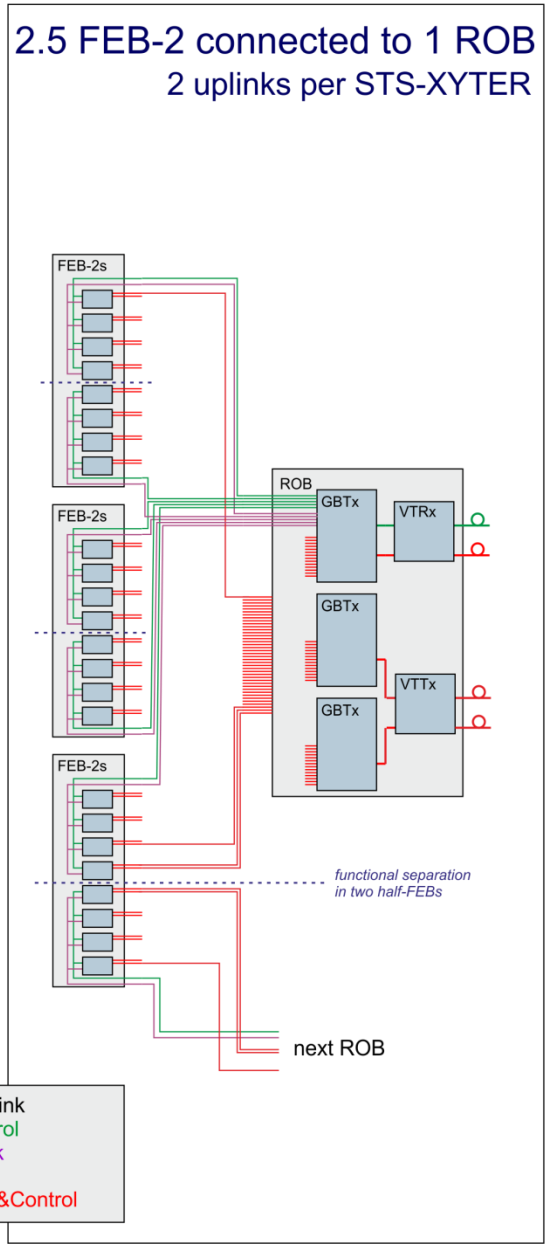
Worst Case RO Scenario:

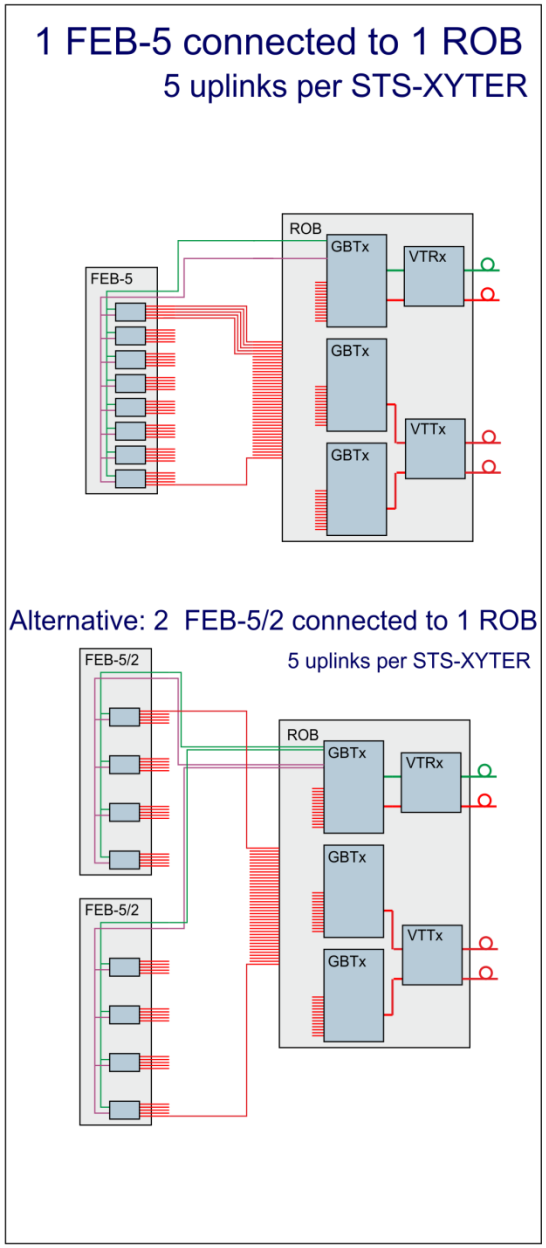
- **35 AGeV Au+Au**
- nominal beam (10^9) & interaction(10^7) rates
- **delta electrons** (mirrored left/right!)
- STS geometry 13d
- shielding from support structures
- 30bits/hit
- 6% protocol overhead



FEB Types and ROB Connectivity

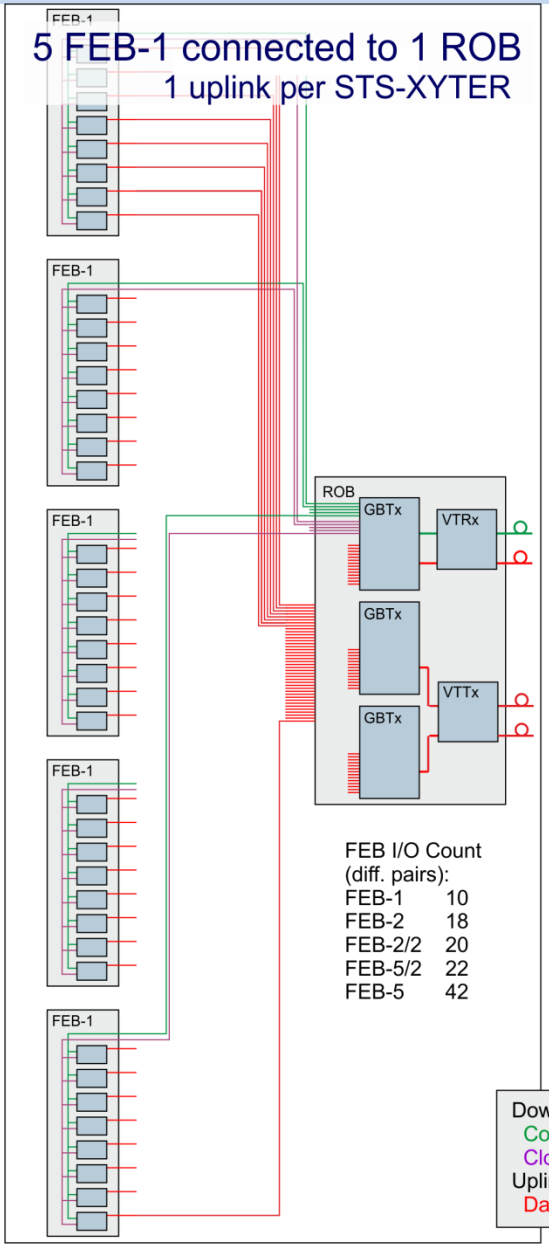


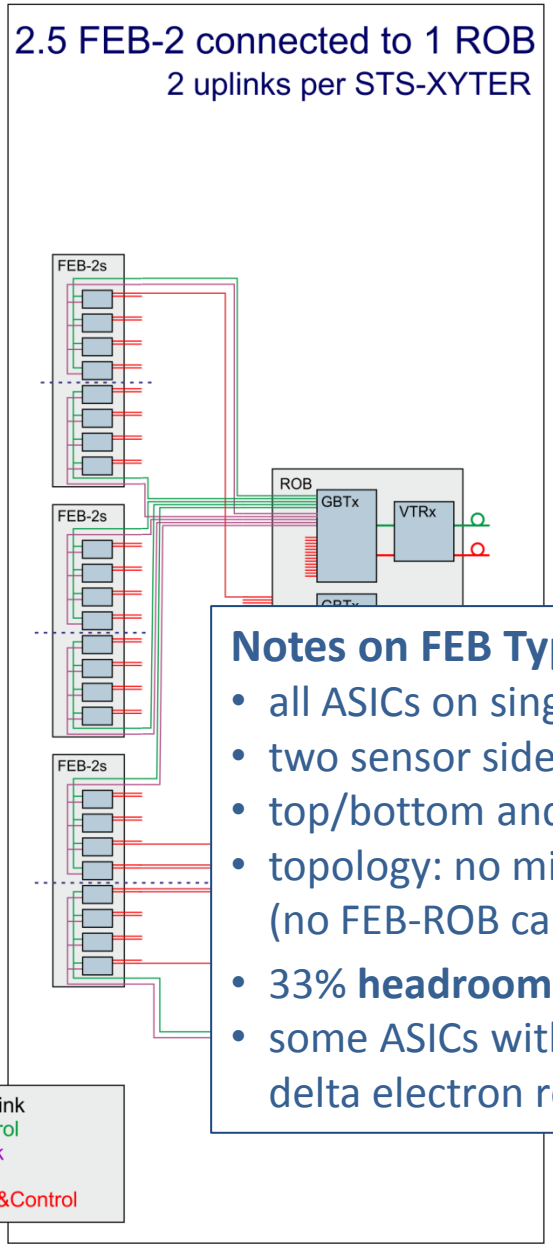


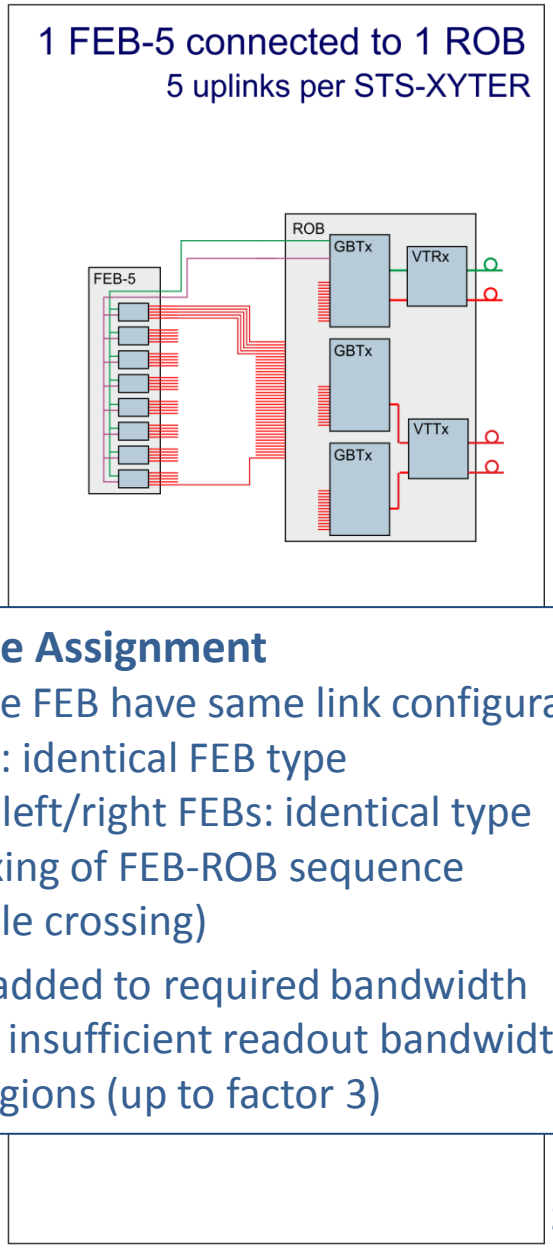


Downlink
Control
Clock
Uplink
Data&Control

FEB Types and ROB Connectivity







Notes on FEB Type Assignment

- all ASICs on single FEB have same link configuration
- two sensor sides: identical FEB type
- top/bottom and left/right FEBs: identical type
- topology: no mixing of FEB-ROB sequence (no FEB-ROB cable crossing)
- 33% **headroom** added to required bandwidth
- some ASICs with insufficient readout bandwidth: delta electron regions (up to factor 3)

STS Status

- **STS-XYTER** ASIC
  version2 being prepared for submission
  - implements E-Link interface (configurable up to 5 x 320 Mbit/s E-links)
  - implements newly developed dedicated readout and control protocol
- Readout and Control **Protocol**
  - synchronous protocol
  - optimized for secure control (downlink) and efficient readout (uplink)
  - verification ongoing
- CERN VLDB (Versatile Link Demonstrator Board)
  - single GBTx, VTRx, SCA: soon available for user tests
- Common **CBM ROB Prototype**
  - **Full GBTx/VL functionality** for all CBM ASIC readout chains (STS, TOF, TRD)
    - 1 master with VTRx and 2 slave GBTx (via SCA and I2C) with VTTx
  - **frontend connectivity** (GBTx E-Links, SCA) routed to **FMC connector**
  - specification phase
- CBM Detector Specific ROBs
  - GBT and Versatile Link components ordered: ~**1000 ROBs** for STS

CERN GBT and Versatile Link System

Goal

- Optical link for transfer of **data, slow control, clock, trigger** between

"**Outside**" (counting room, service building) *radiation free environment*	⟺	**Detector area** *significant radiation levels*

Two complementary projects of CERN(PH-ESE) & collaborators

- **G**iga**B**it **T**ransceiver : "develops and qualifies the required radiation hard ASICs"
  - **GBTx** ASIC: data transceiver
  - GBT-**SCA**: slow control ASIC
- **Versatile Link**: "selects and qualifies appropriate opto-electronic components for use in radiation environment"
  - **VTRx** (optical transceiver) and **VTTx** (optical twin transmitter): custom modules

Status

- prototypes tested; preparation for mass production
- single production run; next device generation in a few years (for LS3 upgrades)
- projected schedule: *samples in mid 2015, larger quantities in 2016*
  developed mainly for LHC LS2 upgrades 2018/19 – consistent with CBM timeline

Features of GBT/VL Based Readout

- symmetrical, bi-directional data transmission
  - **3.2 Gbit/s** user bandwidth; in uplink **4.48 Gbits/s** possible (without forward error correction)
- frontend side: 10 to 40 **E-links:** SLVS based with 320, 160 or 80 Mbit/s
  - data from e-link ports are multiplexed/demultiplexed in the GBT data stream
  - transparent to user protocol, no buffering or load balancing
- **deterministic latency** in both directions
- **radiation hard**
  - mass production will be qualified for 1 MRad total dose, 5×10^{14} n_{eq}/cm^2
- GBTx power
  - configuration dependent: <1.5W typical; 2.2W max.

***VTRx** (front) with SFP+ for comparison*

Photo: CERN

The GBT System