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A viable on-chip FPGA configuration memory scrubbing approach for CBM-ToF

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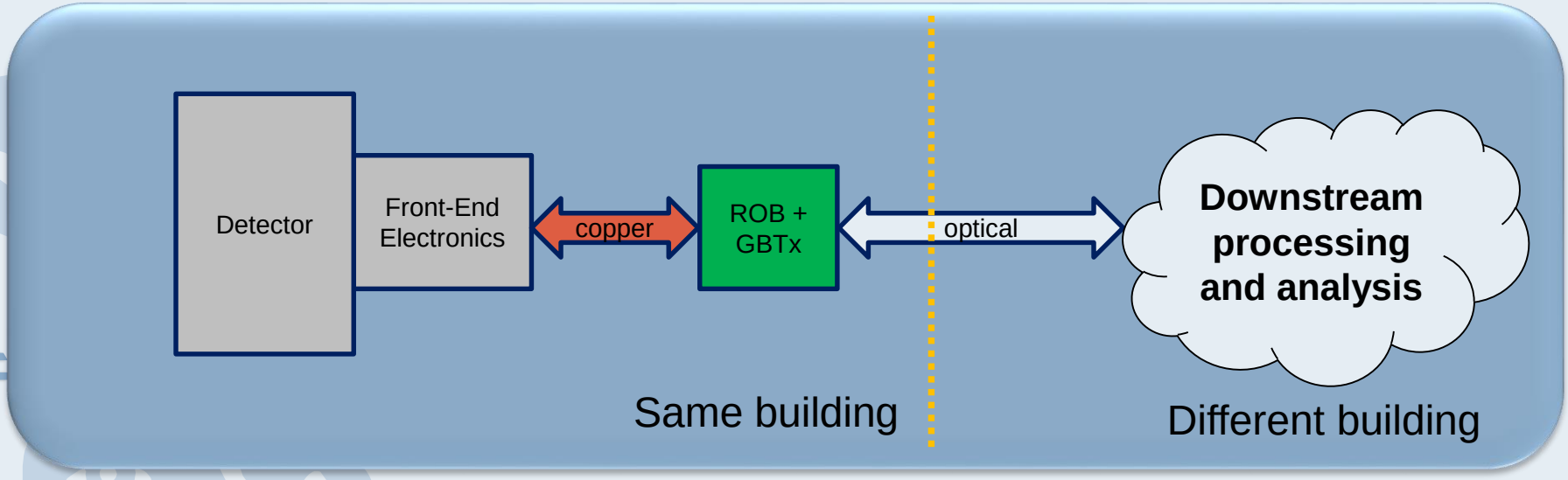
Outline

- **Motivation**
- **Resilience Concept**
  - 7 Series Scrubbing
  - Configuration Management Entity
- **The GBT-SCA**
  - Overview
  - JTAG interface
- **Current Status**
  - Implementation
  - Beamtests
  - Proof of concept
- **Summary**
- **Next Steps**

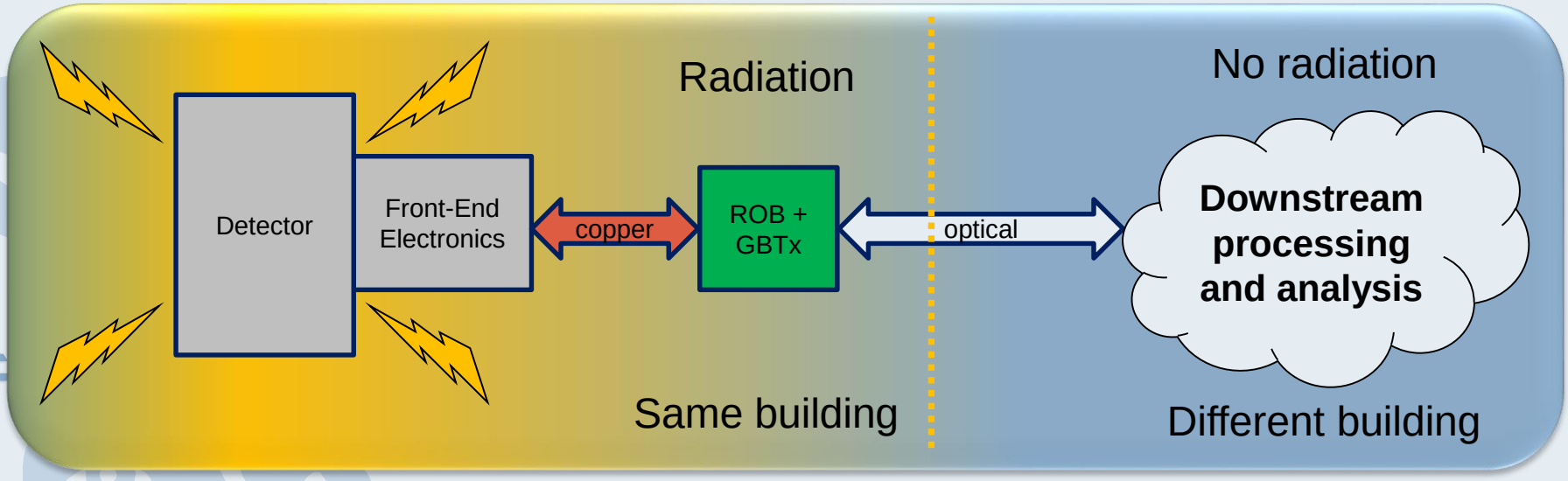
Motivation

Motivation



- **GBTx as downstream connection**
- **Local intelligence in ROB is essential:**
  - Zero suppression : Transmitting Gbps of noise is expensive and unnecessary
  - Pre-filtering, simple data compression, status, logs, etc.
- **FPGA is needed**
  - Flexibility: Firmware is adaptable to changing demands
  - General purpose: Easy connection to GBTx and custom front-end (that may change)

Motivation (Continued)



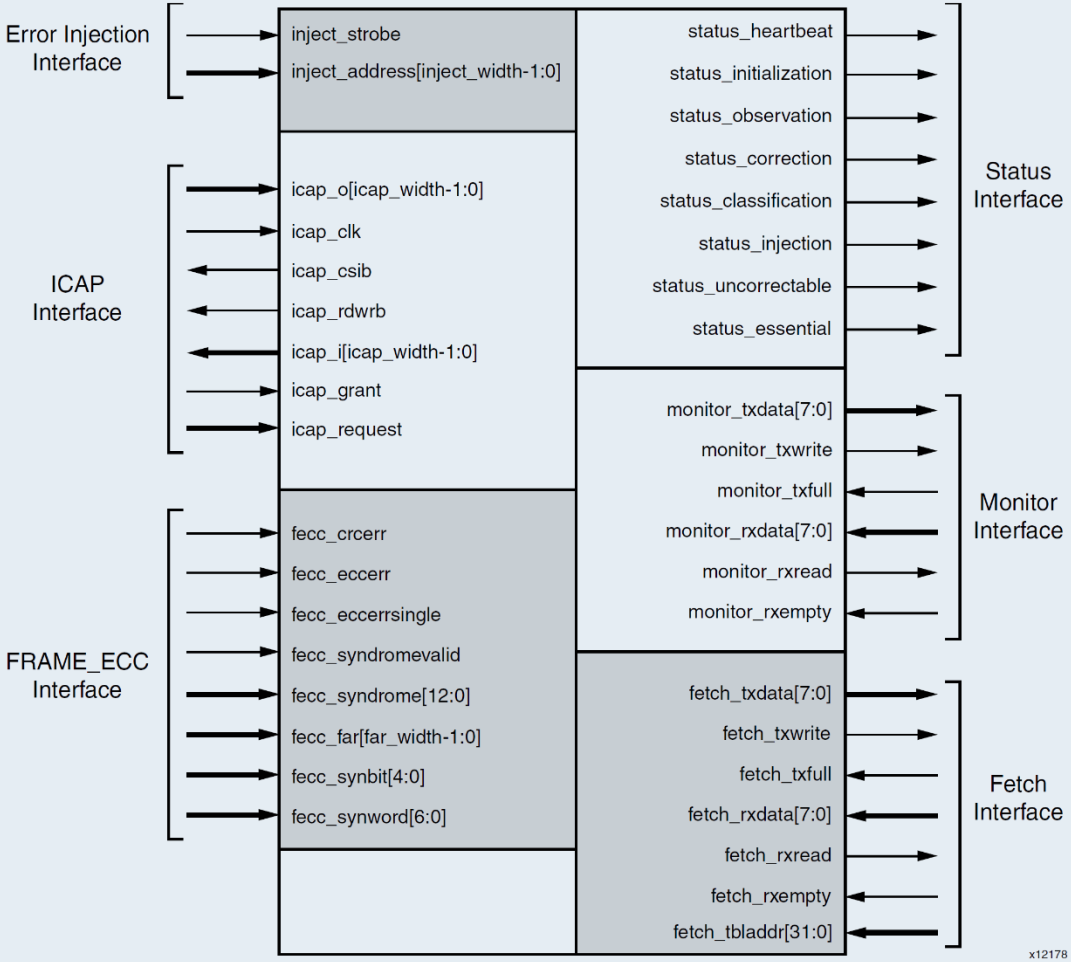
- **Read-Out Board (ROB) in radiation environment**
- **GBTx is rad-hard by design**
- **ROB FPGA is not**
  - Fault-tolerant and autonomous **Flash free** concept needed
  - Xilinx offers Soft Error Mitigation IP-Core (SECDED)
  - GBTx offers SCA (Slow Control Adapter ASIC)
    - JTAG interface
    - Interrupt-capable GPIOs for fast reactions to upsets

Resilience Concept

7 Series Scrubbing

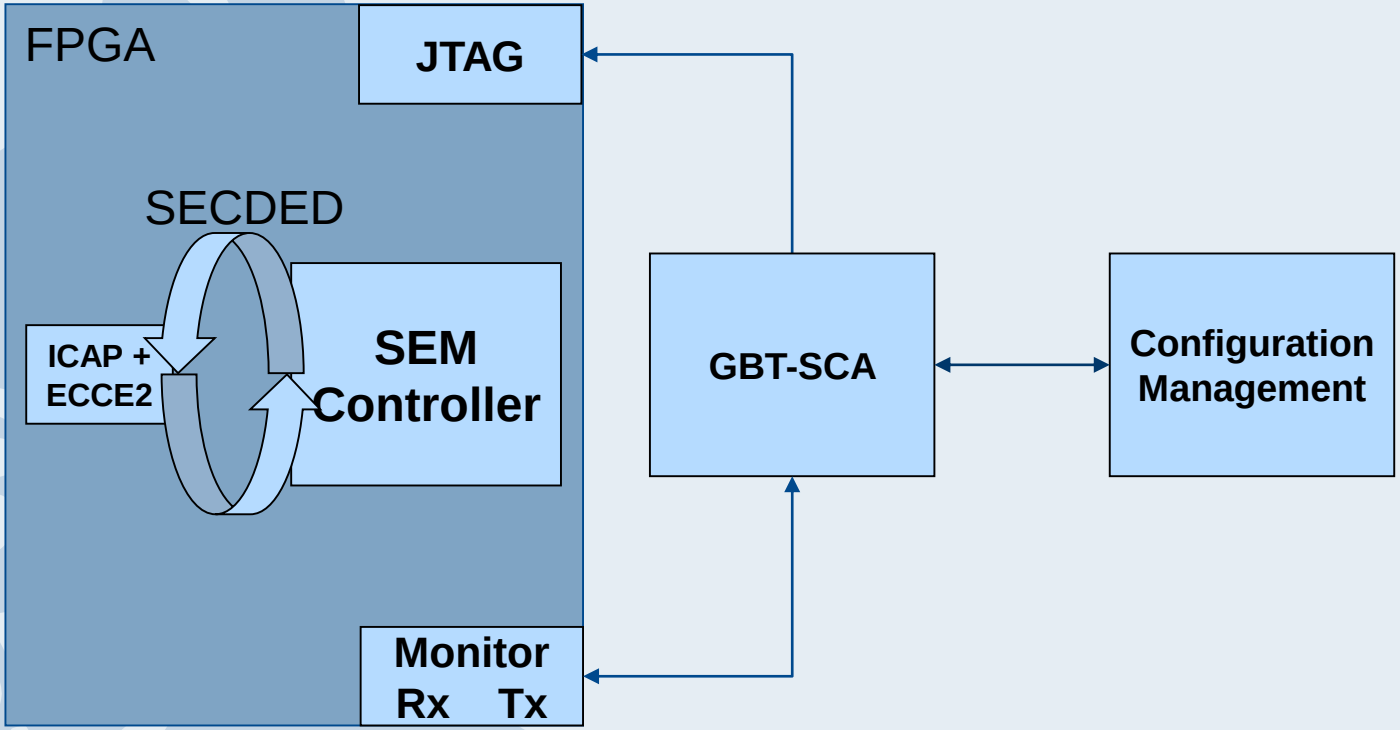
Soft Error Mitigation Controller

- Automatically corrects one-bit-errors (SECDED)
- FRAME_ECCE2 for readback CRC
- ICAP for configuration
- Monitor Interface for control commands
  - Status
  - Start / Stop
  - Error Injection
  - Watchdog
- Available for Artix 7 since Vivado 2014.1 (used in beamtest)



Scrubbing Strategy

- **Continuous readback through ICAP**
  - Fix and report single-bit upsets (SBUs)
  - No overhead for slow control



Scrubbing Strategy

- **Continuous readback through ICAP**
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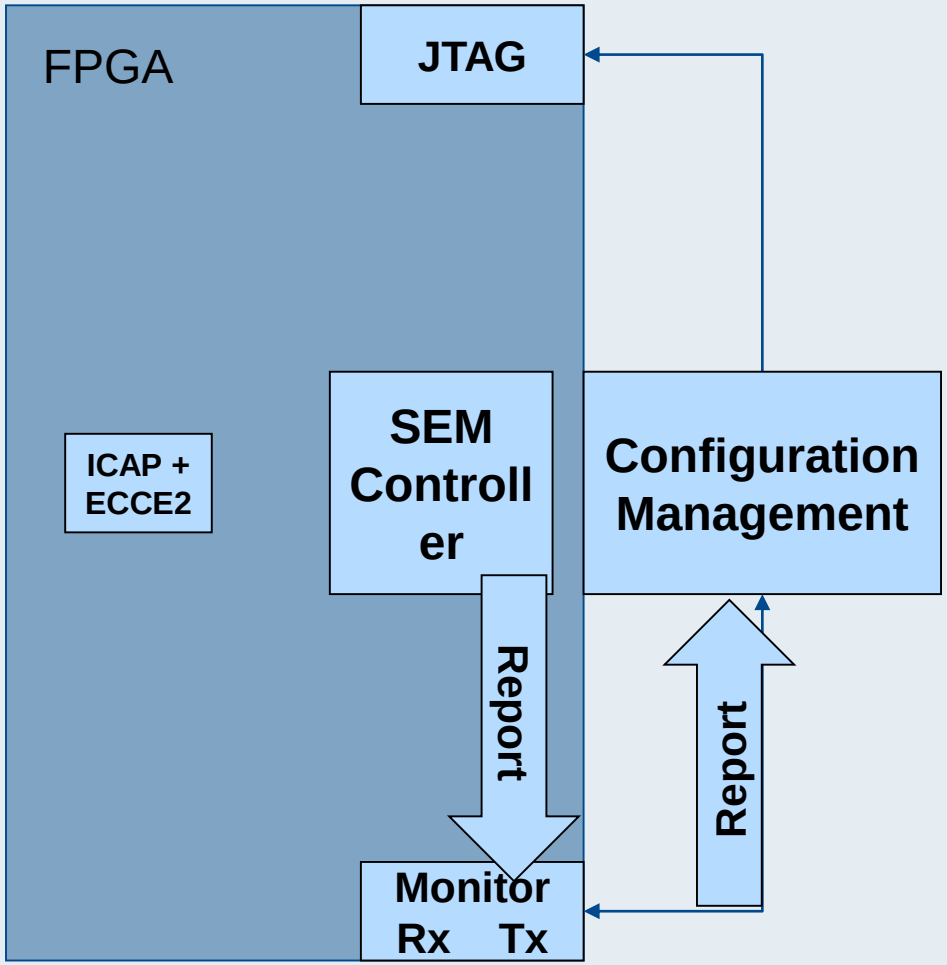
- **On multible-bit upset (MBU)**
  - report and stop



Scrubbing Strategy

- **Continuous readback through ICAP**
  - Fix and report single-bit upsets (SBUs)
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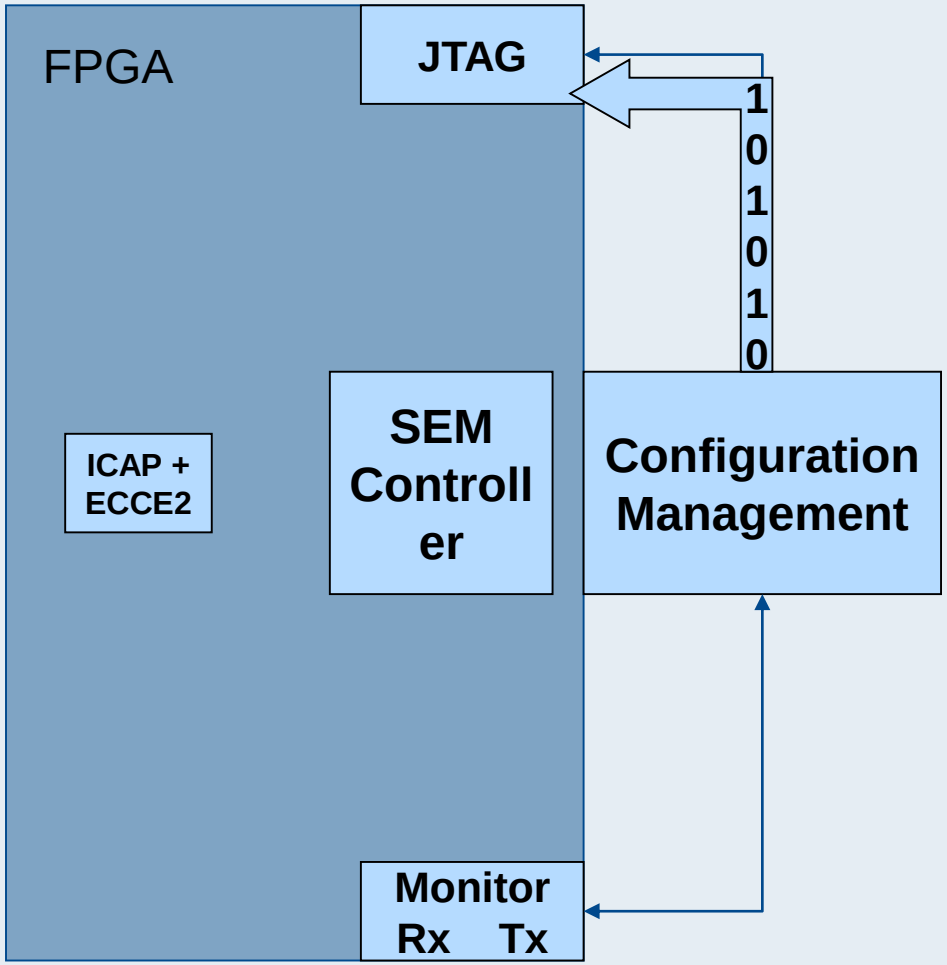
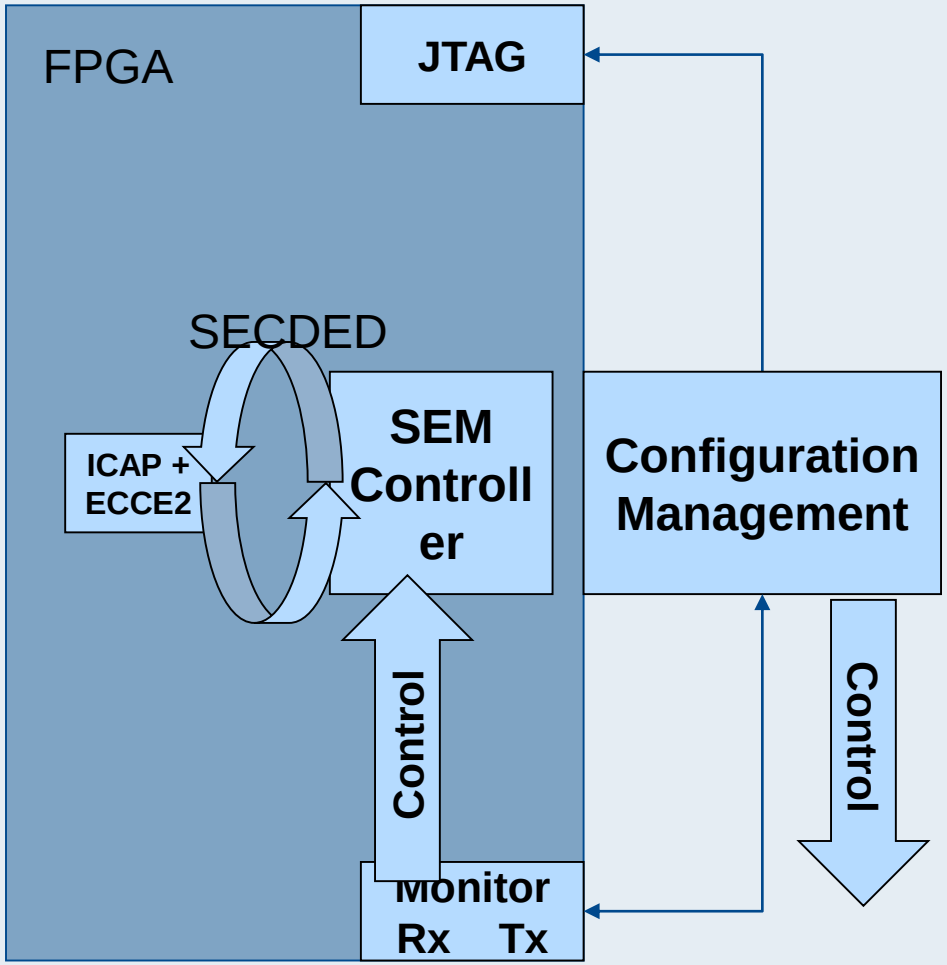
- **On multible-bit upset (MBU)**
  - report and stop
  - Fix error
    - ECC error: Reconfigure frame
    - CRC error: Reconfigure device



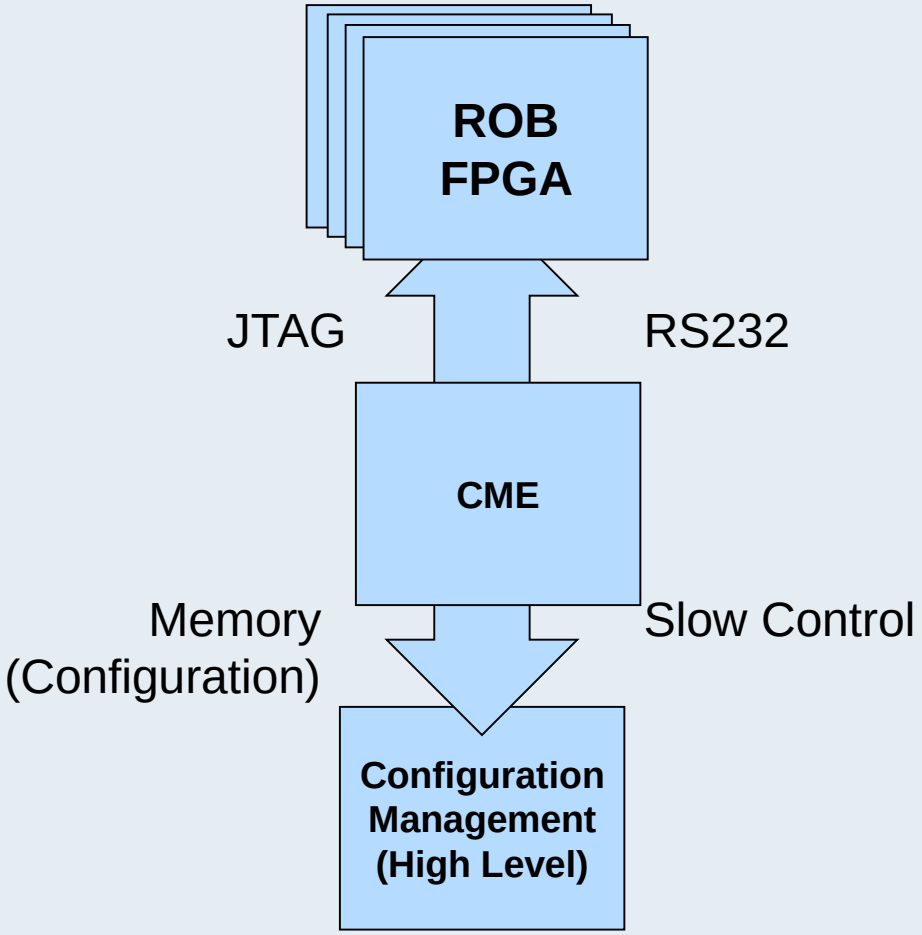
Scrubbing Strategy

- **Continuous readback through ICAP**
  - Fix and report single-bit upsets (SBUs)
  - No overhead for slow control
- **On multible-bit upset (MBU)**
  - report and stop
  - Fix error
    - ECC error: Reconfigure frame
    - CRC error: Reconfigure device
  - Fix and restart continuous readback



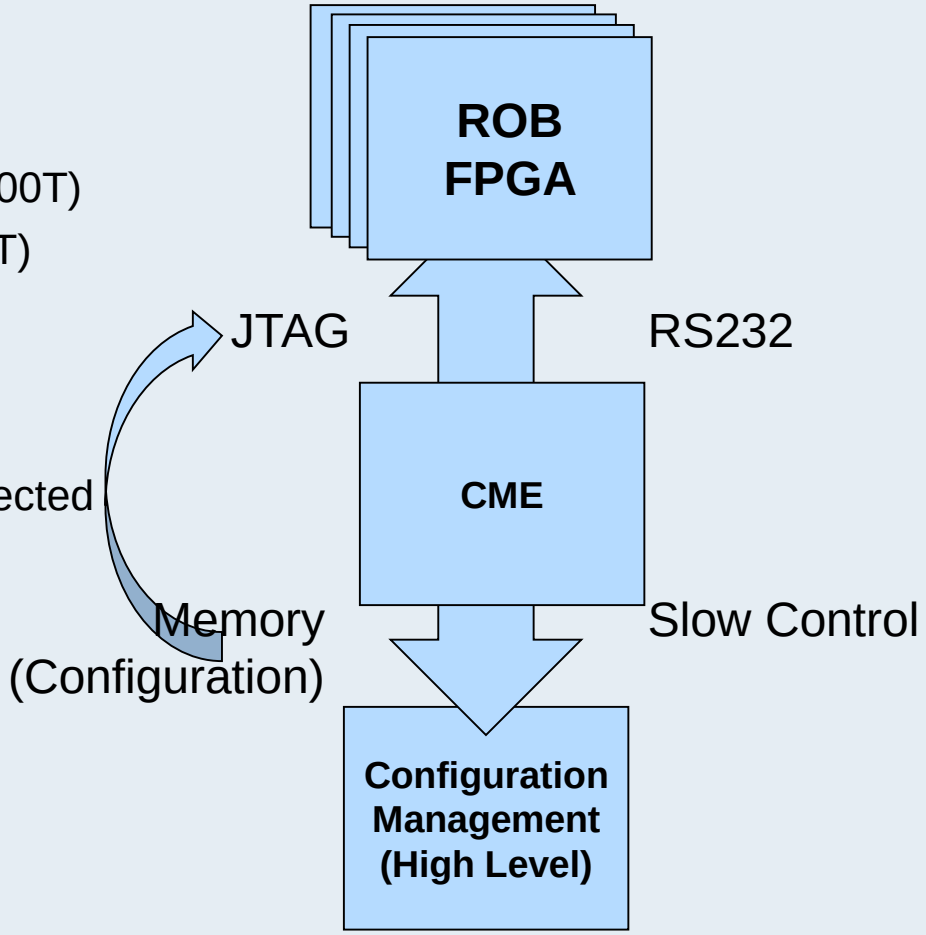
Cofiguration Management Entity (CME)

- **Heart of the Scrubbing Approach:**
- **SEM IP Core Control**
- **(Partial) Reconfiguration**
- **Configuration data fetching**
- **Statistics**
- **Fault injection (for test setups)**



Cofiguration Management Entity

- **Requirements:**
- **Reconfiguration:**
  - Frame Scrubbing:
    - 1 Frame = 101 Words = 404 B (7A200T)
    - Total of 18310 CLB Frames (7A200T)
  - Full Reconfiguration
    - ~9,2 MB (7A200T)
  - Access to this data needed
  - Programmed through JTAG port (connected to GBT-SCA)



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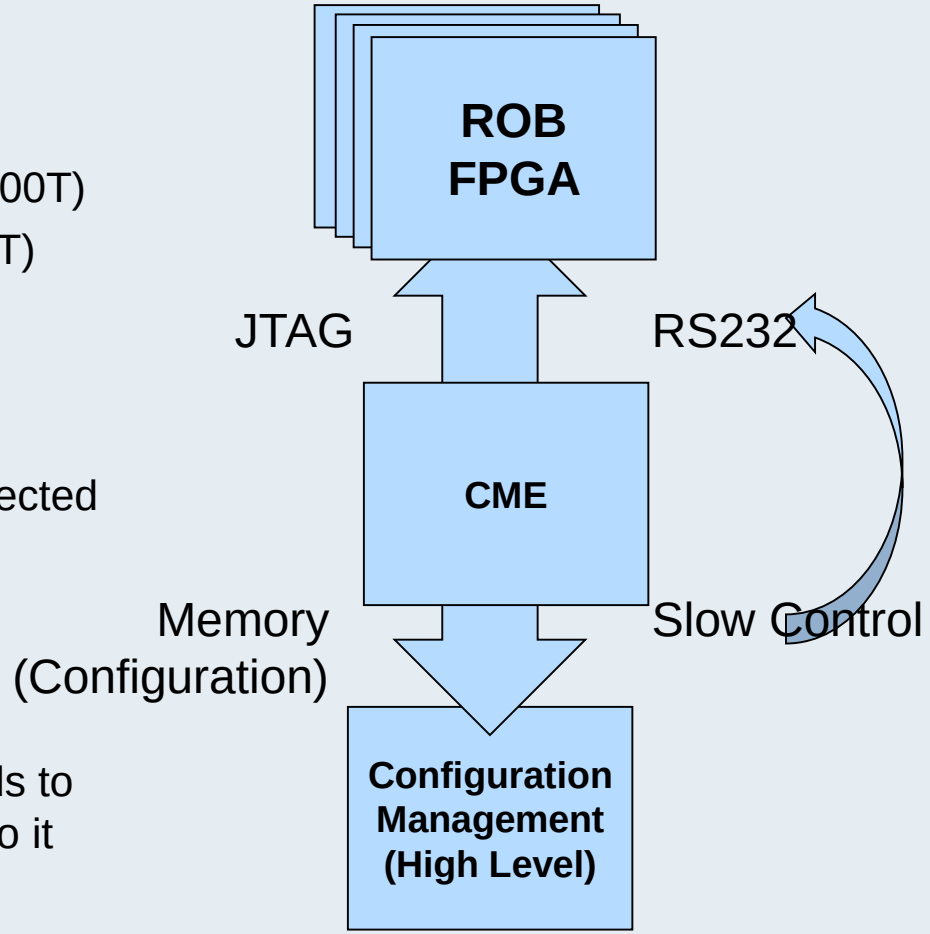
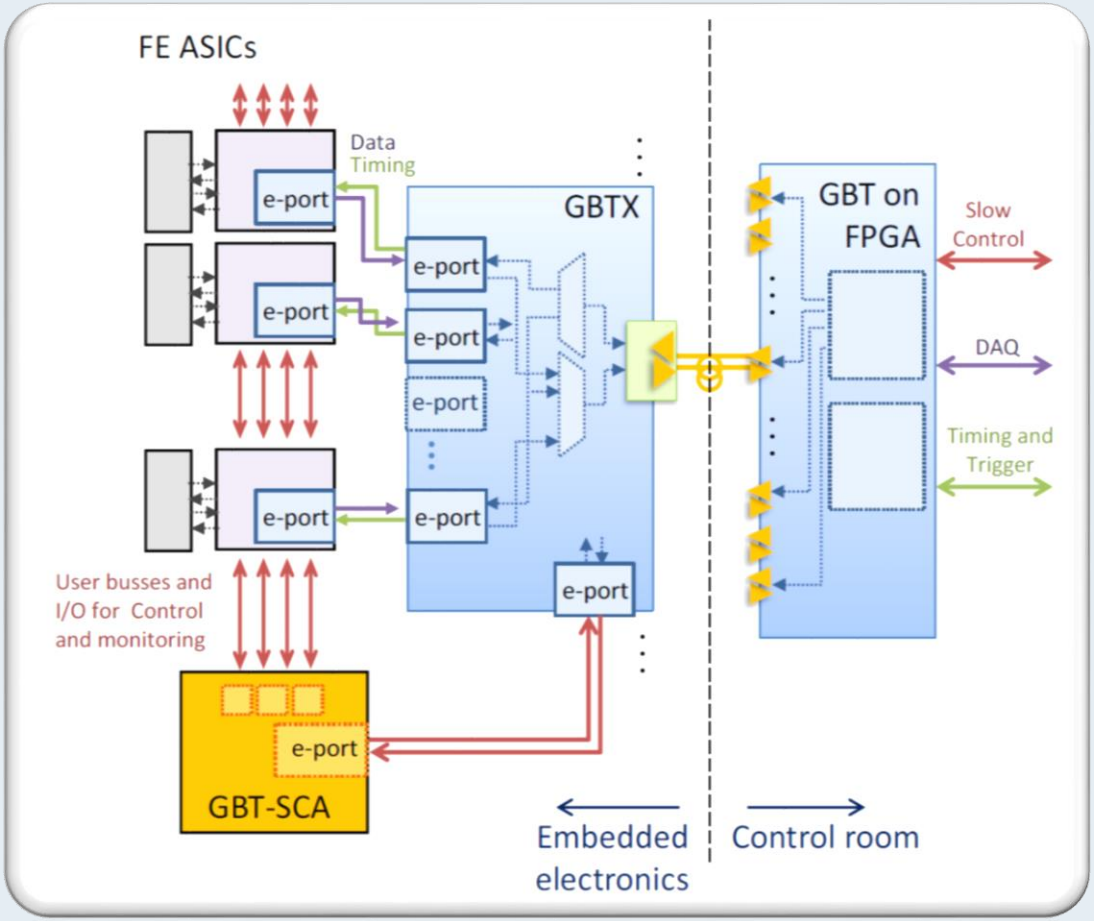
    - Total of 18310 CLB Frames (7A200T)
  - Full Reconfiguration
    - ~9,2 MB (7A200T)
  - Access to this data needed
  - Programmed through JTAG port (connected to GBTX)
- **Monitoring/Control**
  - RS232 Rx/Tx Signals for every SEM Controller
  - Configuration Management Entity needs to interpret the incoming data, and react to it



The GBT-SCA

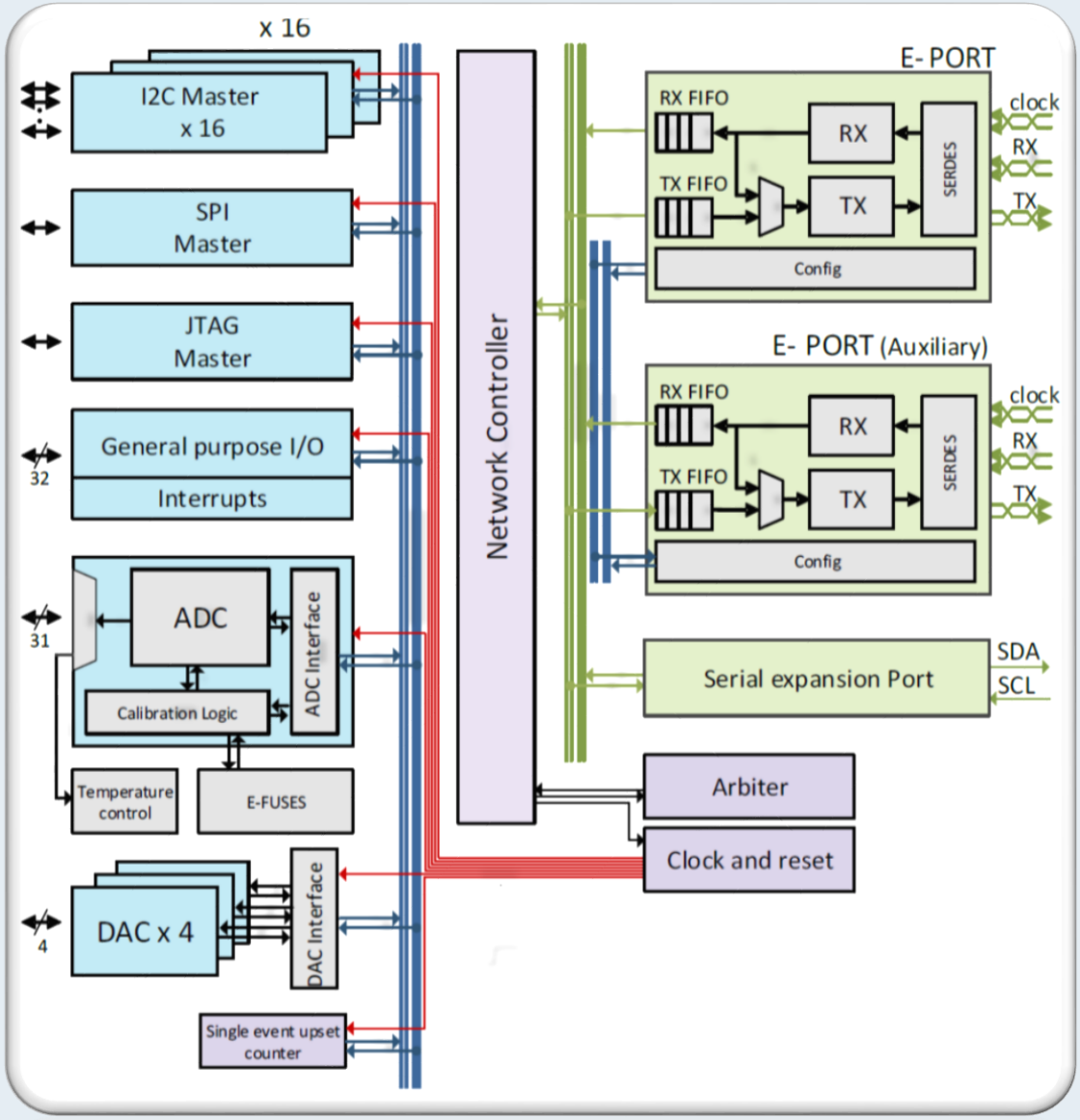
The GBT-SCA

- **ASIC dedicated to slow control**
- **Offered features include:**
  - JTAG master player
  - I²C
  - GPIOs
  - SPI
  - DAC
  - ADC



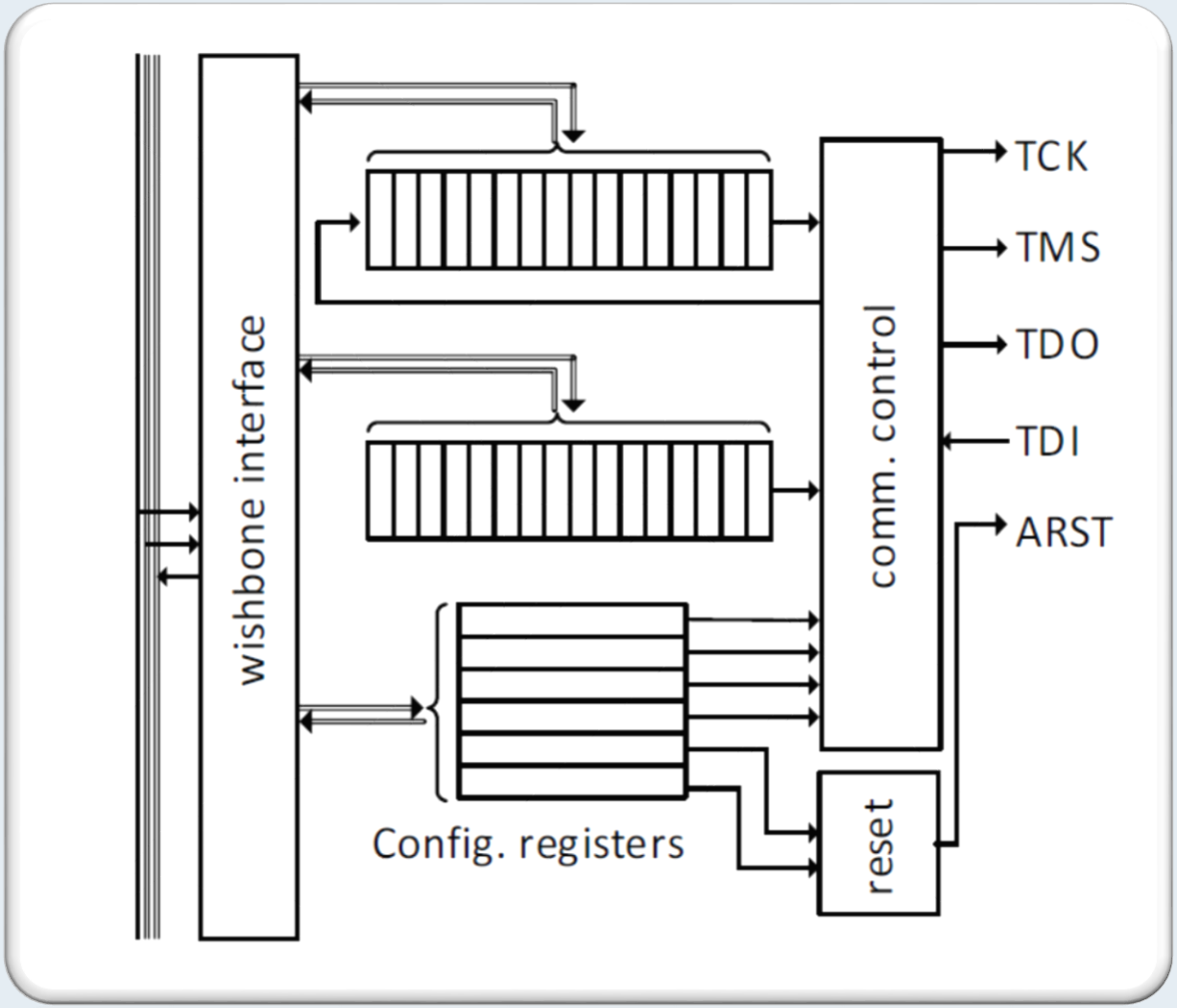
The GBT-SCA (Continued)

- **Transparent communication with modules**
- **Every module is accessible to the user as a channel**
  - Channel address determines module
  - Every channel has a set of commands
  - Commands are acknowledged



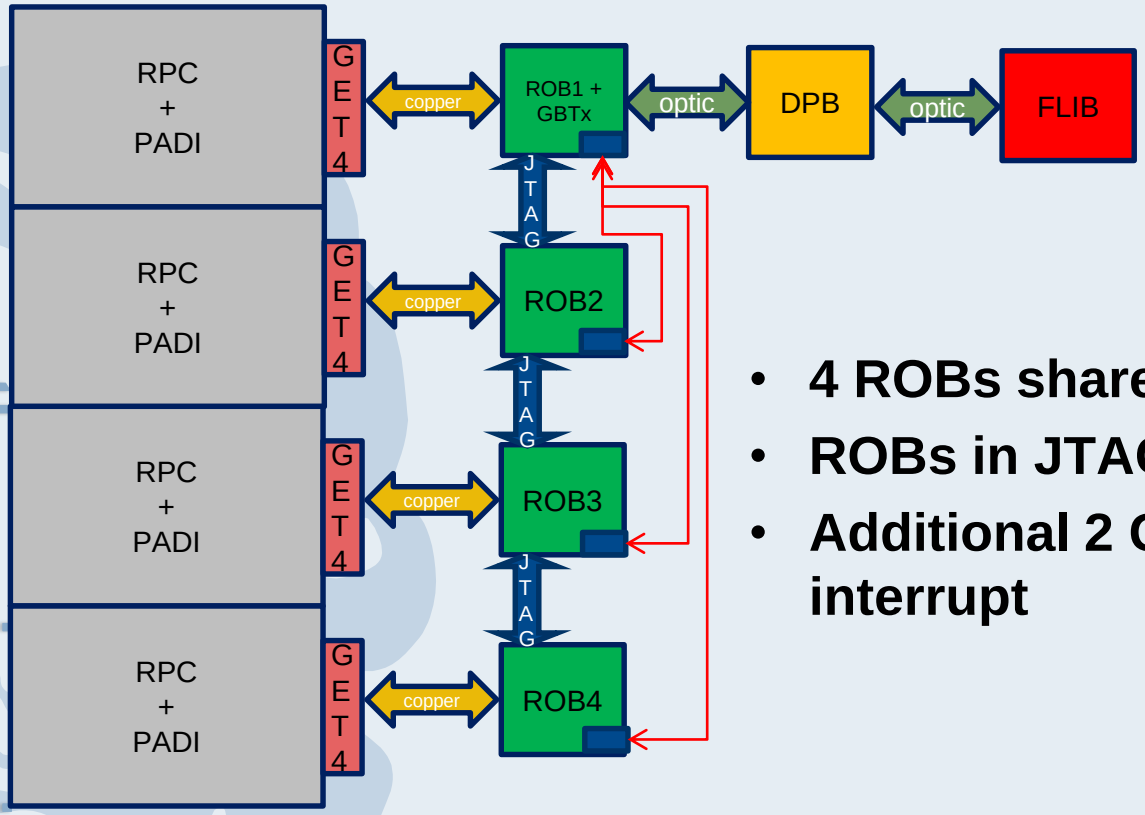
JTAG Interface

- **128 bit shift registers**
  - TDO/TDI
  - TMS
- **Configuration registers**
  - Clock speed
  - Sampling edge inversion
  - Transmission length
  - Start transmission
- **CCLK 156kHz – 20 MHz**
- **Software library**
- **Xilinx FPGA has already been programmed with it**



Current Status

Read-Out Chain

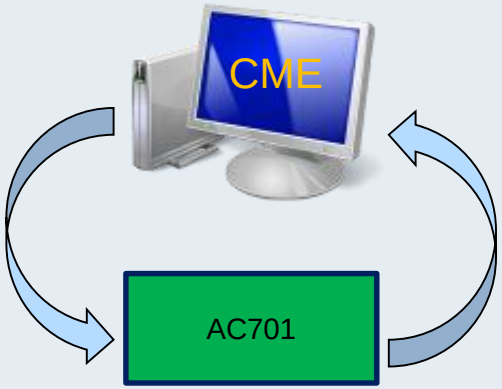


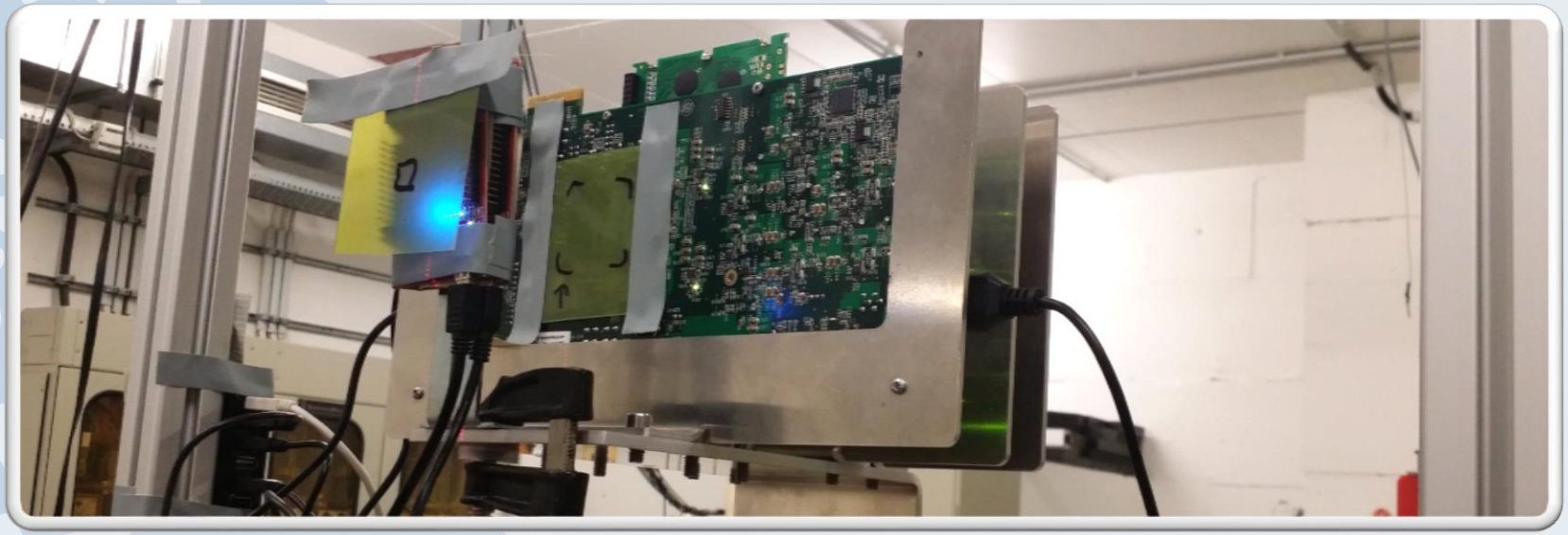
(c) Jochen Frühauf

- **4 ROBs share 1 GBT-SCA**
- **ROBs in JTAG daisy chain**
- **Additional 2 GPIOs per ROB + interrupt**

Implementation

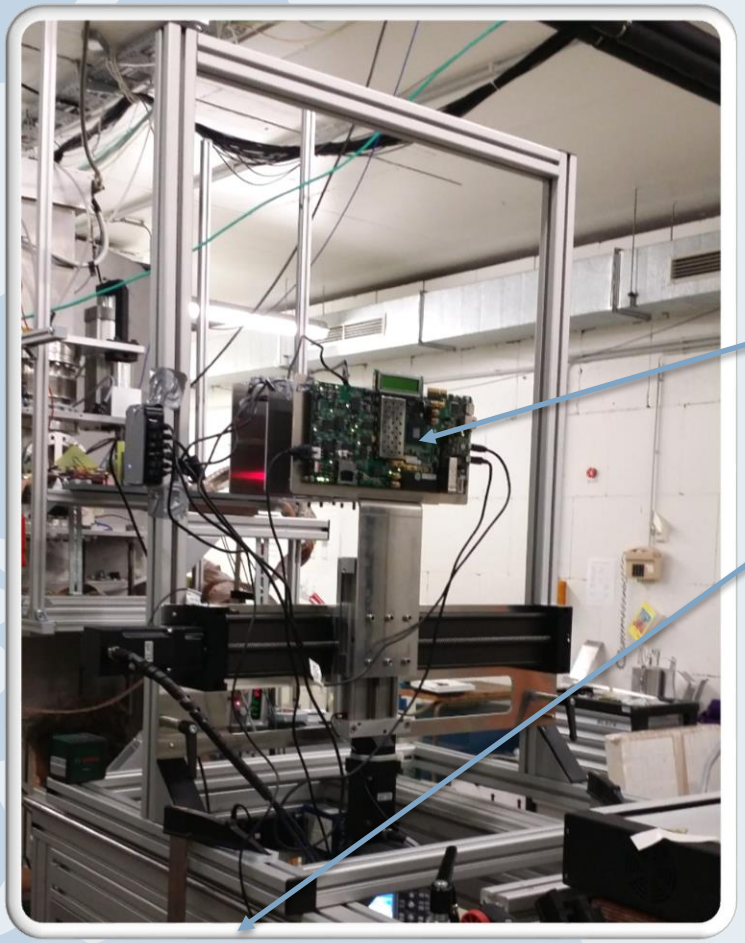
- CME running on PC
- SEM running on AC701
- RS232 and JTAG connection
- Two beamtests conducted with this setup





Beamtests

- **Beamtest @ FZ Jülich December 2014 & February 2015**
- **High and low rate runs**



AC701 development board running SEM Controller

PC running CME, XZ-Stage Control and monitoring tools

Beamtests (Continued)

- **Event Rates**

- **High rate [events per minute] ~** 2.5x10^7p/s

One-Bit ECC	Two Bit ECC	CRC	Frame Address Hit	SEM Halt	affected frame not CLB	Ghost Frame
32,22	4,06	0,39	0,00	0,05	0,00	0,92

- **Low rate [events per minute] ~** 4.2x10^6 p/s

One-Bit ECC	Two Bit ECC	CRC	Frame Address Hit	SEM Halt	affected frame not CLB	Ghost Frame
0,126	0,012	0,001	0,000	0,000	0,000	0,002

- **~10 min : Single-bit upset**
- **~71 min : Multiple-bit upset**
- **~14 h : Full reprogram**
- **This accumulates for many ROCs**

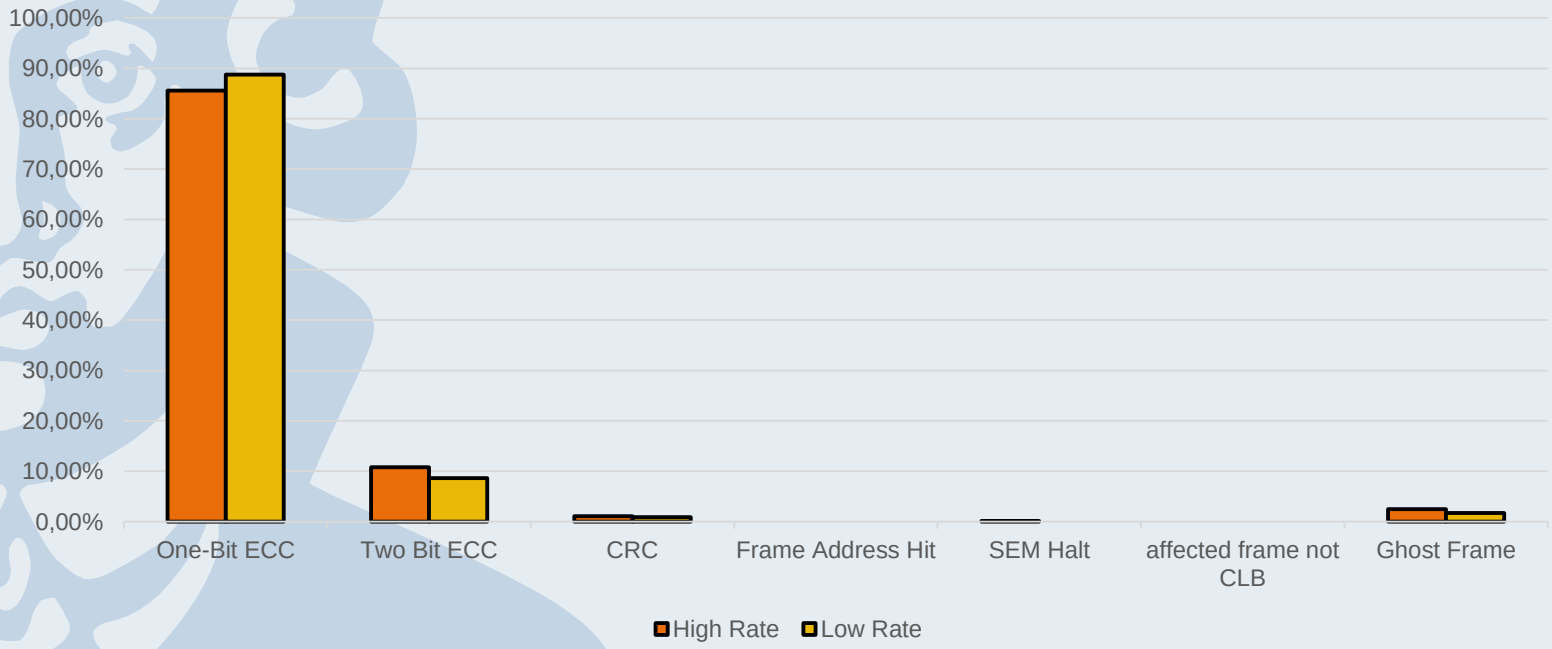
Beamtests (Continued)

- **High rate event distribution ~** 2.5x10^7p/s

One-Bit ECC	Two Bit ECC	CRC	Frame Register Hit	SEM Halt	affected frame not CLB	Ghost Frame
85,59%	10,80%	1,04%	0,00%	0,12%	0,00%	2,45%

- **Low rate event distribution ~** 4.2x10^6 p/s

One-Bit ECC	Two Bit ECC	CRC	Frame Register Hit	SEM Halt	affected frame not CLB	Ghost Frame
88,79%	8,62%	0,86%	0,00%	0,00%	0,00%	1,72%

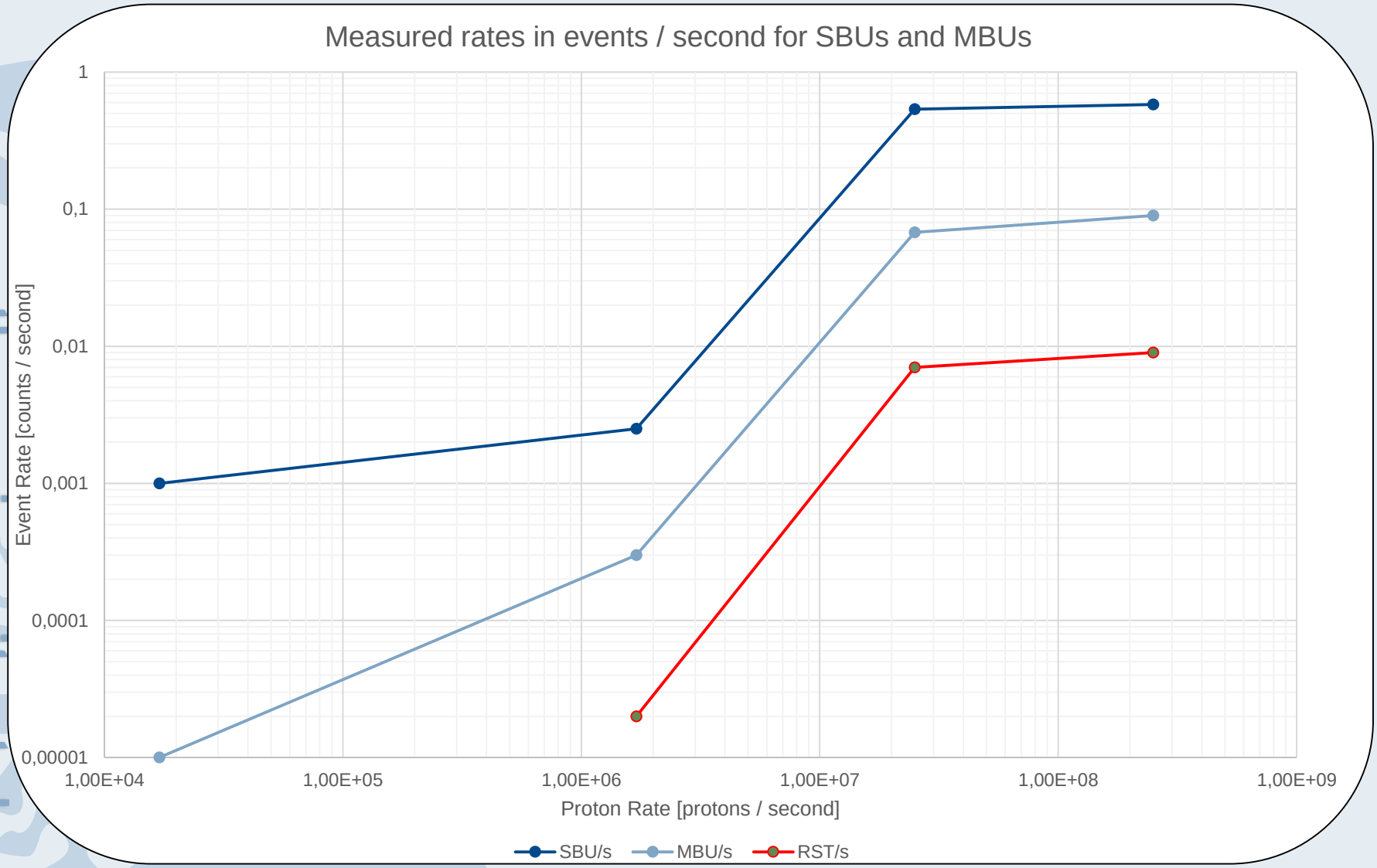


Beamtests (Continued)

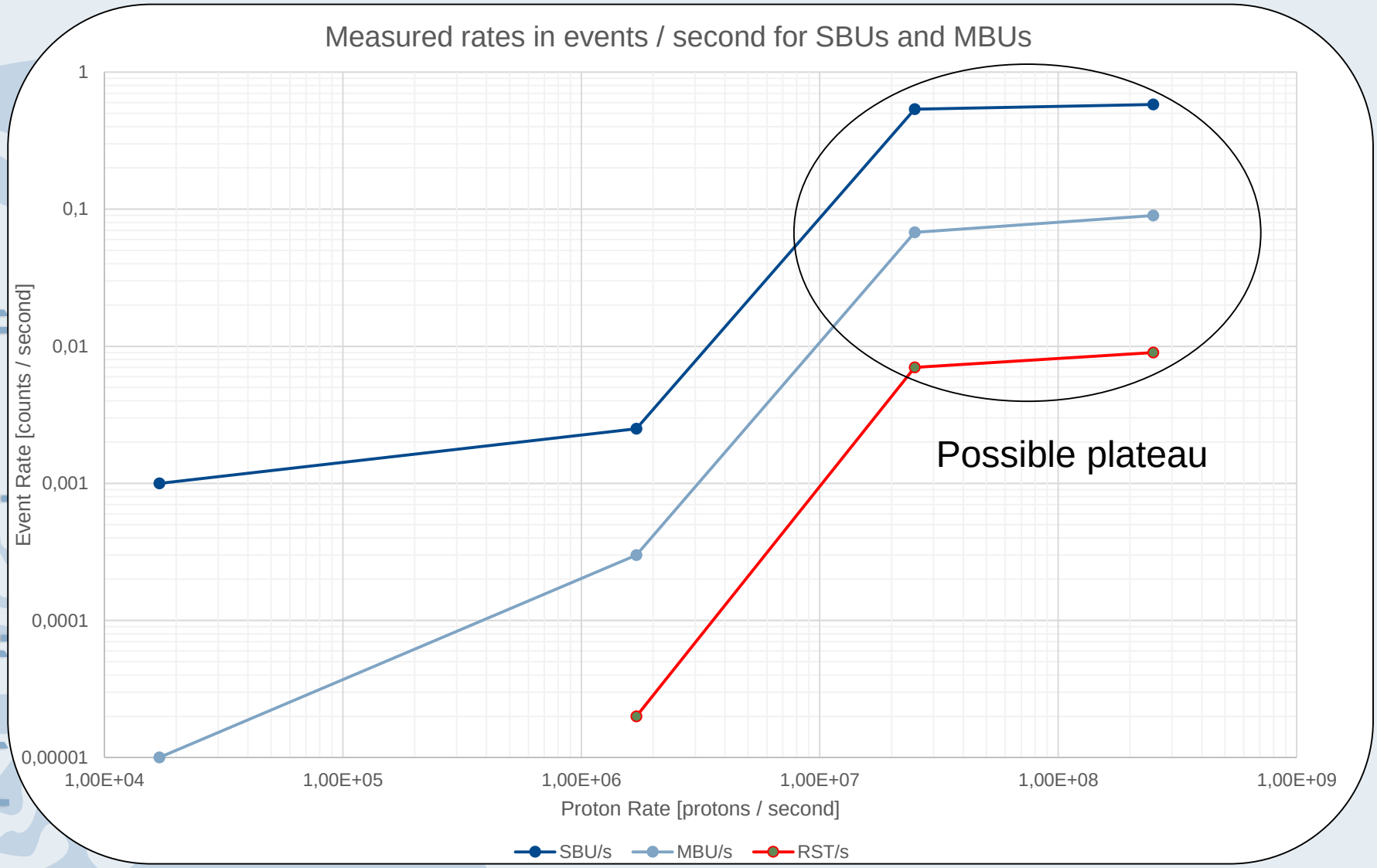
- **Less single-bit errors (SBUs) for higher rate than for lower**
  - Upper limit for SEM controller functionality?
    - More upsets than can be fixed
    - Rate should go into saturation

- **Irradiation at different Fluxes to gather more statistics**

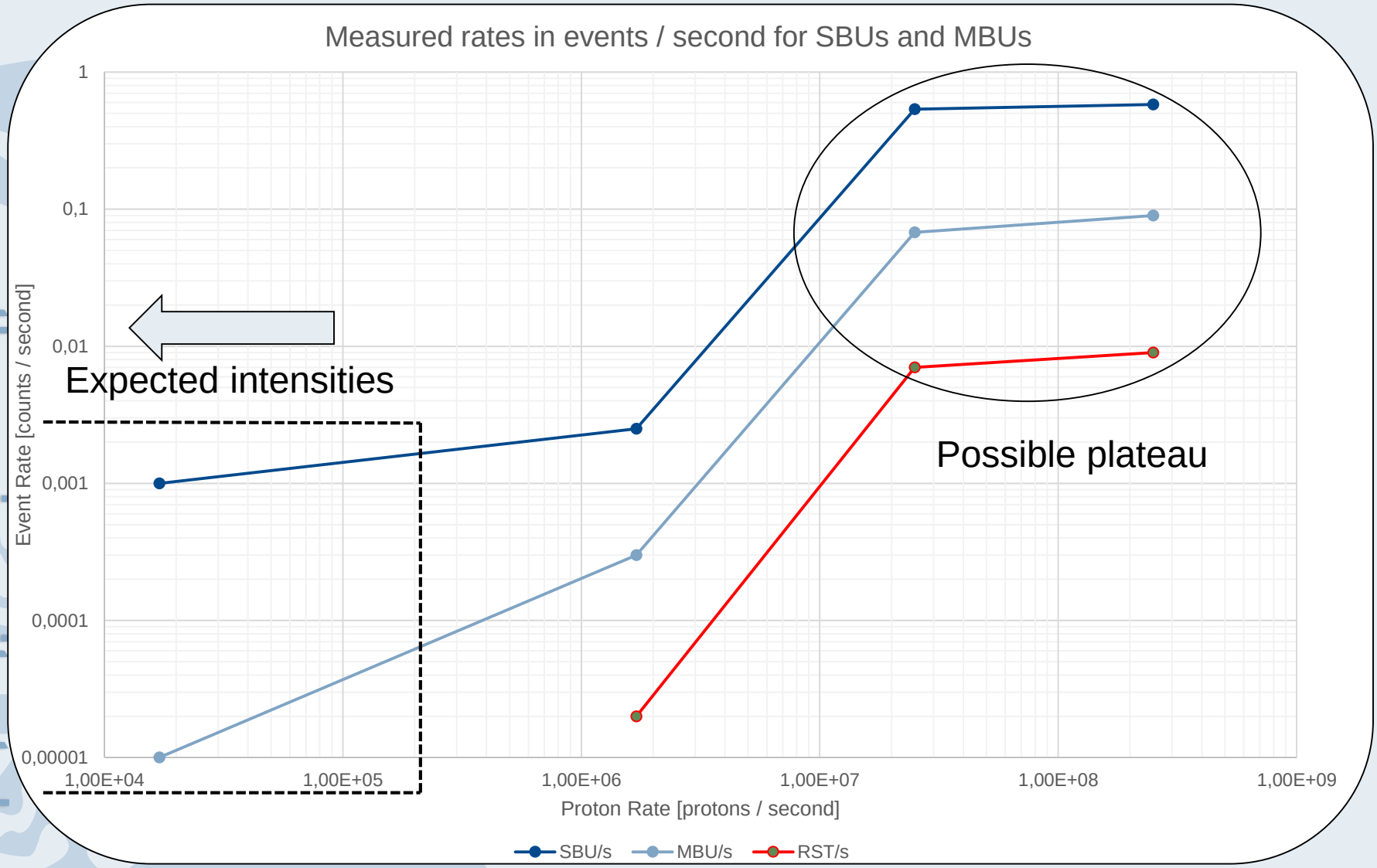
Beamtests (Continued)



Beamtests (Continued)



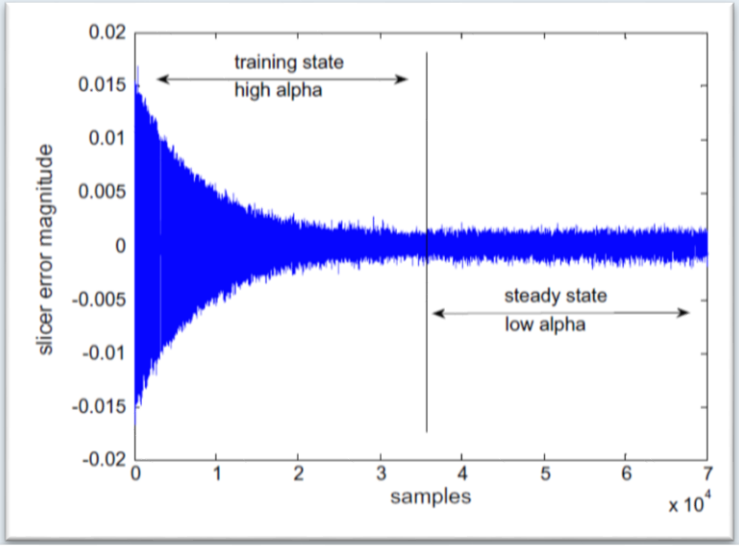
Beamtests (Continued)

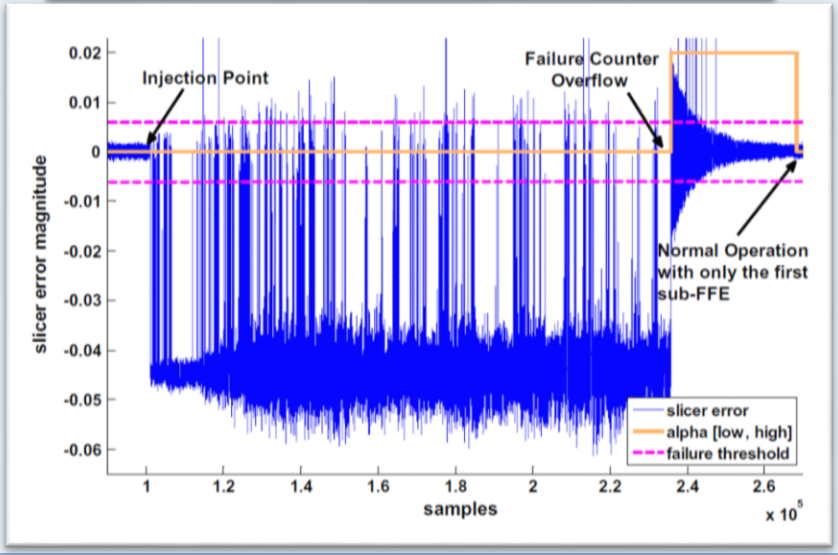


Proof of Concept

Mitigation of permanent faults in adaptive equalizers

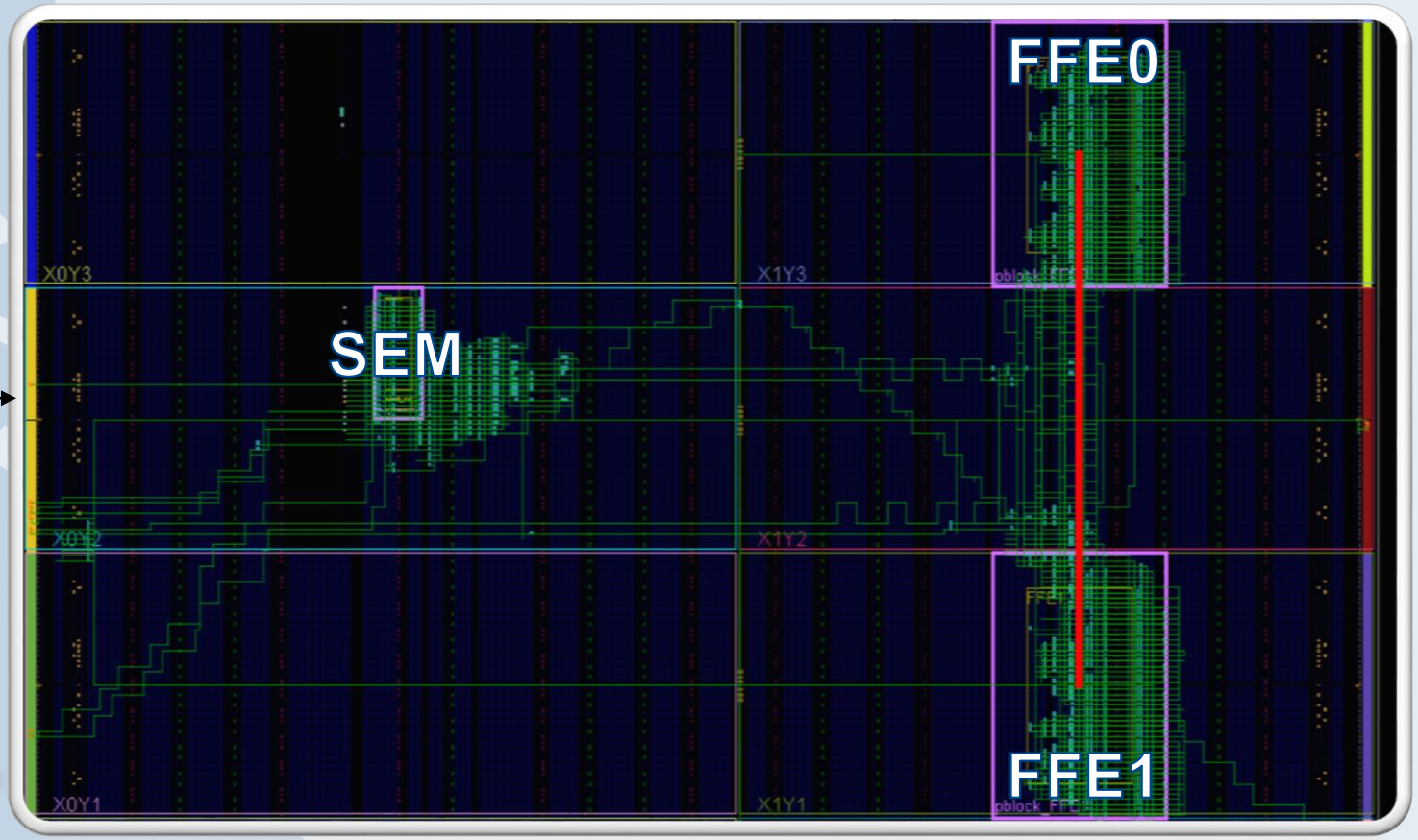
- **Equalizer removes noise from received data**
- **Slicer error used for adaption and Upset detection**
- **Upon upset detection in one instance, the output switches to the still intact one**
- **So far only simulations**





Proof of Concept

- **Design implemented on AC701 with SEM Concept**
- **Irradiated with 1,7E06 protons/second @ 2950 MeV/c momentum**



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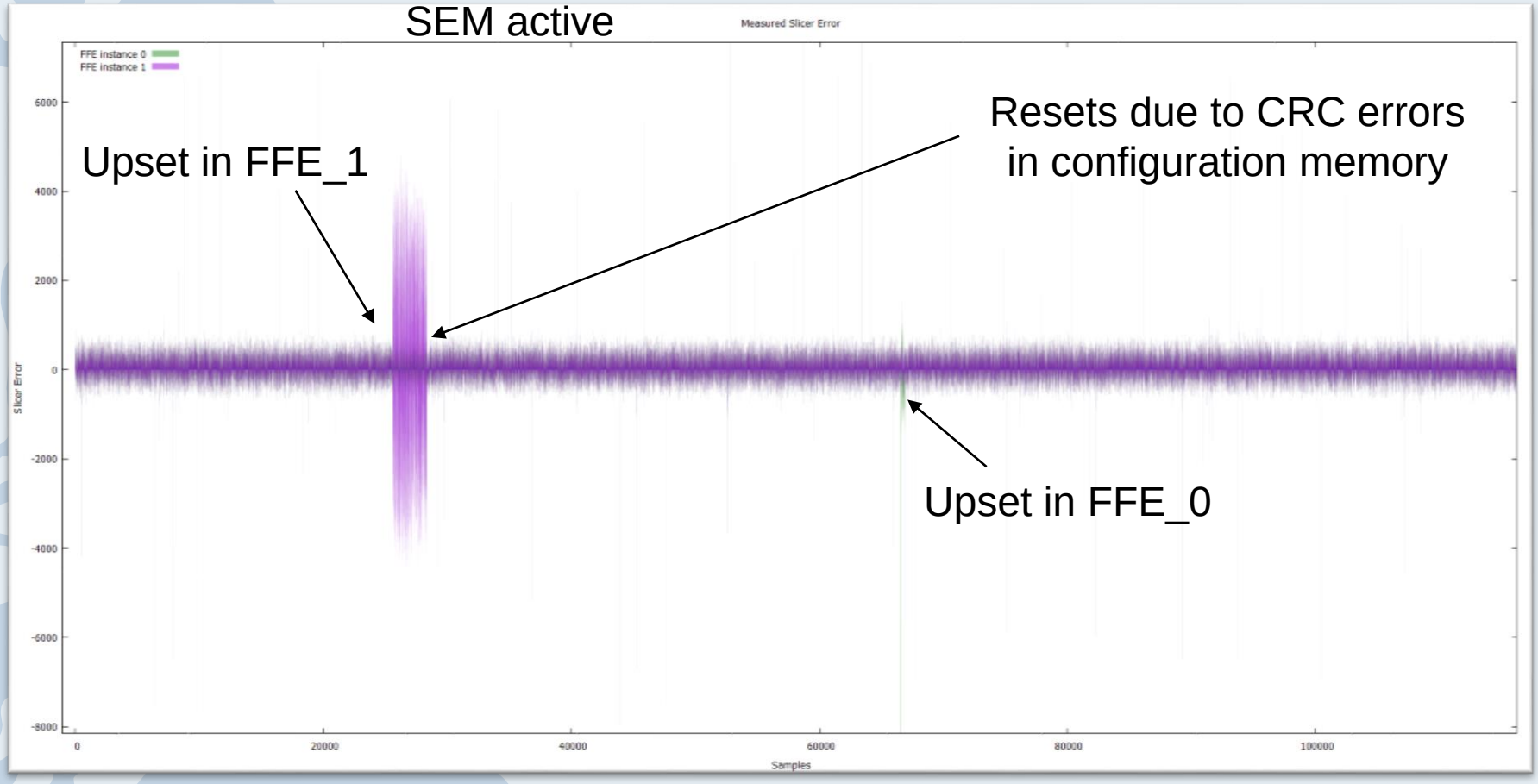

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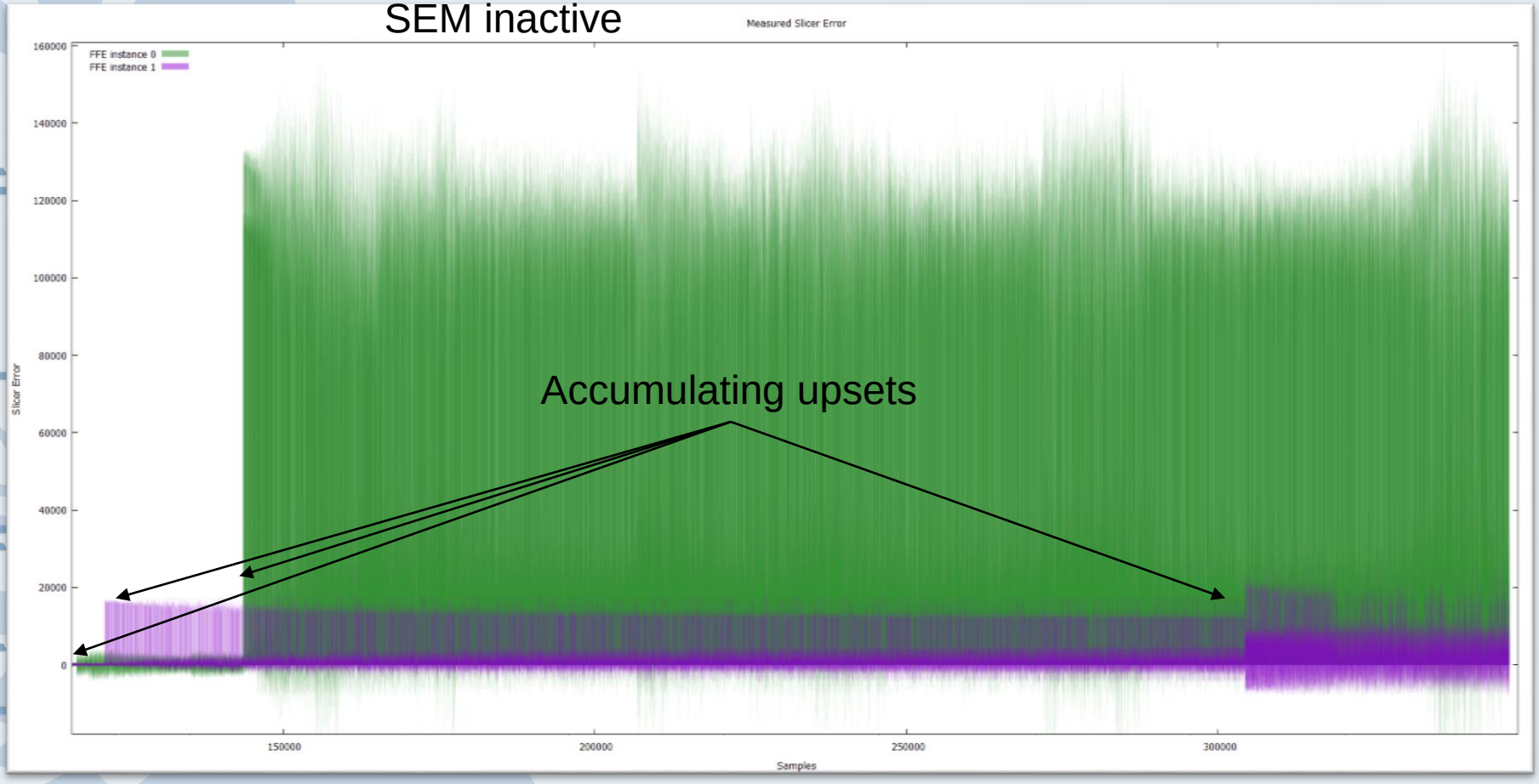

Summary

Summary

- **FPGA needs soft error mitigation techniques to operate in proximity of the detector**

- **Soft error mitigation concept is validated**
  - Repeated successful tests with proton beams of various intensities
  - Expected intensities for ToF < problematic intensities of the approach
  - Proof of concept with adaptive equalizer design

- **Event rates are in agreement with the approach of four FPGAs sharing one GBT-SCA**

Next Steps

Next Steps

- **Four ROBs will share a GBT-SCA**
  - Lab setup with multiple FPGAs in daisy chain for JTAG tests
- **Beamtest with four FPGAs in one chain**
- **Implement first data compression techniques**
- **Port System to GBT-SCA**

Thank you!

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Sources

- GBT: To SCA or not to SCA, Jano Gebelein, CBM FEE/DAQ Workshop 18.02.2014, Darmstadt, Germany
- GBT-SCA: The Slow Control Adapter ASIC for the GBT System (Draft Rev 6.2)
- LogiCORE IP Soft Error Mitigation Controller v4.0, Product Guide for Vivado Design Suite, PG036 19.06.2013
- Mitigation of permanent faults in adaptive equalizers, Pedro Reviriego, S. Liu, and Juan Antonio Maestro. Microelectronics Reliability 51(3):703-710 (2011)

Thank you!

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Backup

Data Rates

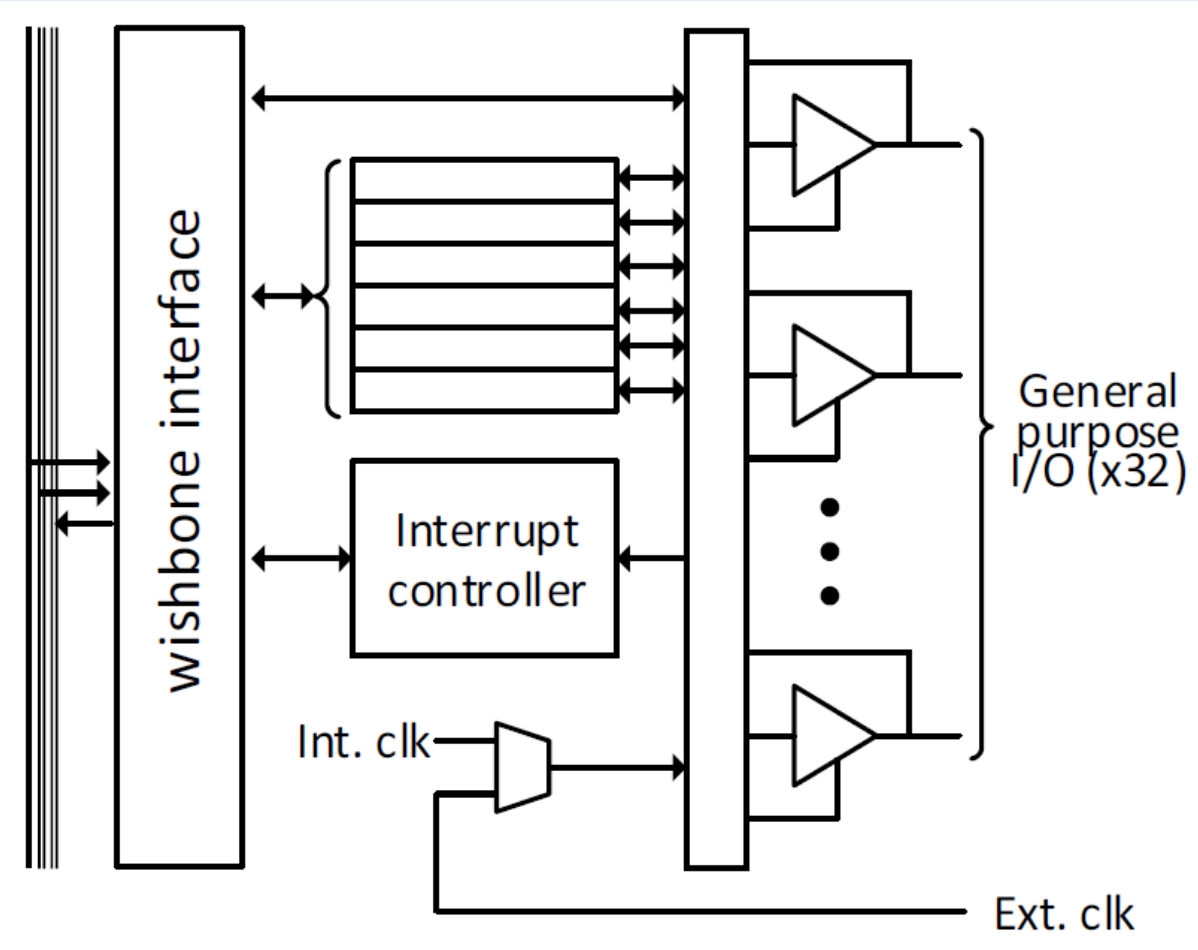
- **Upper limit:**
  - 4 FPGAs in permanent full reconfiguration (worst case)
    - JTAG:

Device	Bitstream Length	JTAG CCLK	# Devices	Duration	Bitrate
7A200T	77845216	6 MHz (std)	4	~52 s	~6 Mbps
7K480T	149880032	6 MHz (std)	4	~100 s	~6 Mbps
7A200T	77845216	20 MHz (JTAG master max)	4	~16 s	~20 Mbps
7K480T	149880032	20 MHz (JTAG master max)	4	~30 s	~20 Mbps

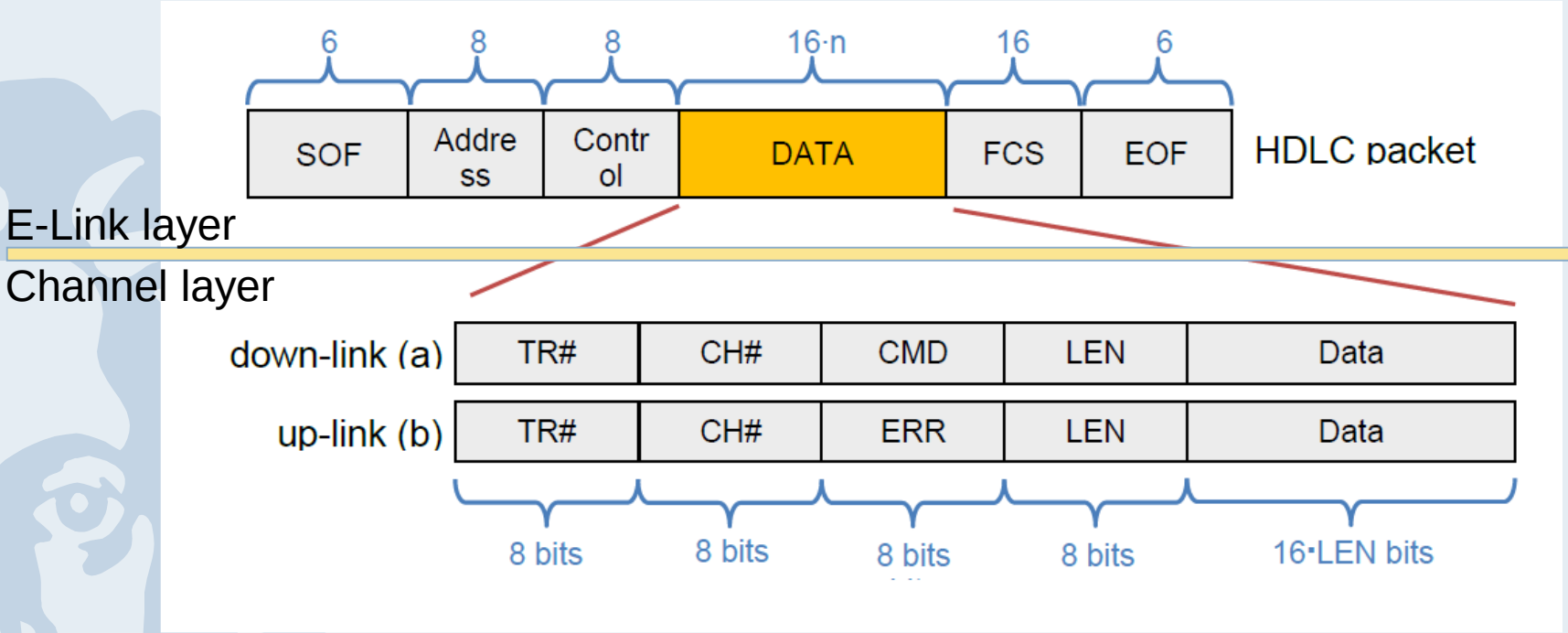
  - Bandwidth allocated by the GBT System for slow control: 80 Mbps
- **Reality: 10 % of all SEE-related events require intervention**
  - 8% Frame correction : partial bitfile of 3232 bits + overhead (~100 bits)
  - 2% Full reconfiguration
- **Tests in a moderate environment needed for event rate (done Dec. 2014 at COSY)**
  - Preliminary: ~10 events per hour

Interfaces

- **GPIO: Overview**
  - 32 independent GPIO signals
    - 40 MHz int. clk
  - Inputs can be configured to cause interrupt requests
  - 32 bit register of GPIO values
  - 32 bit register to enable/disable interrupt capability of a GPIO



Example: How to enable GPIO channel



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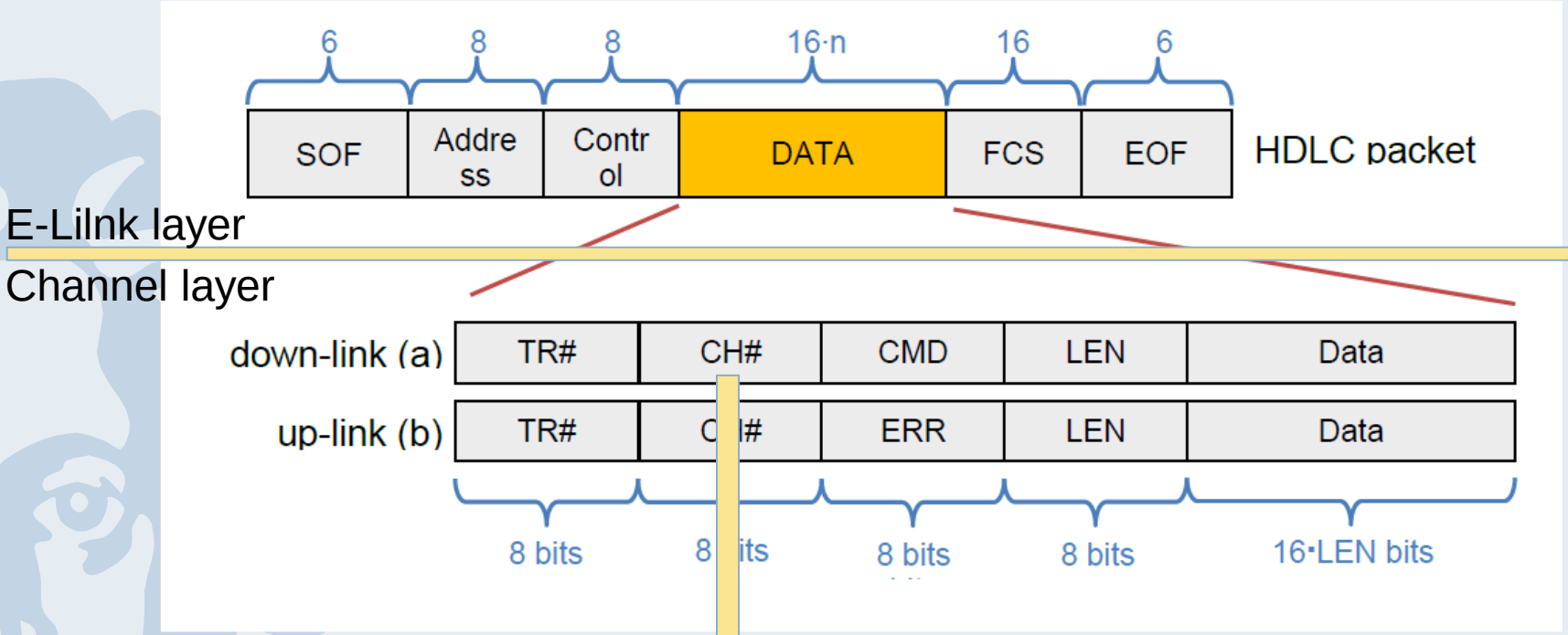
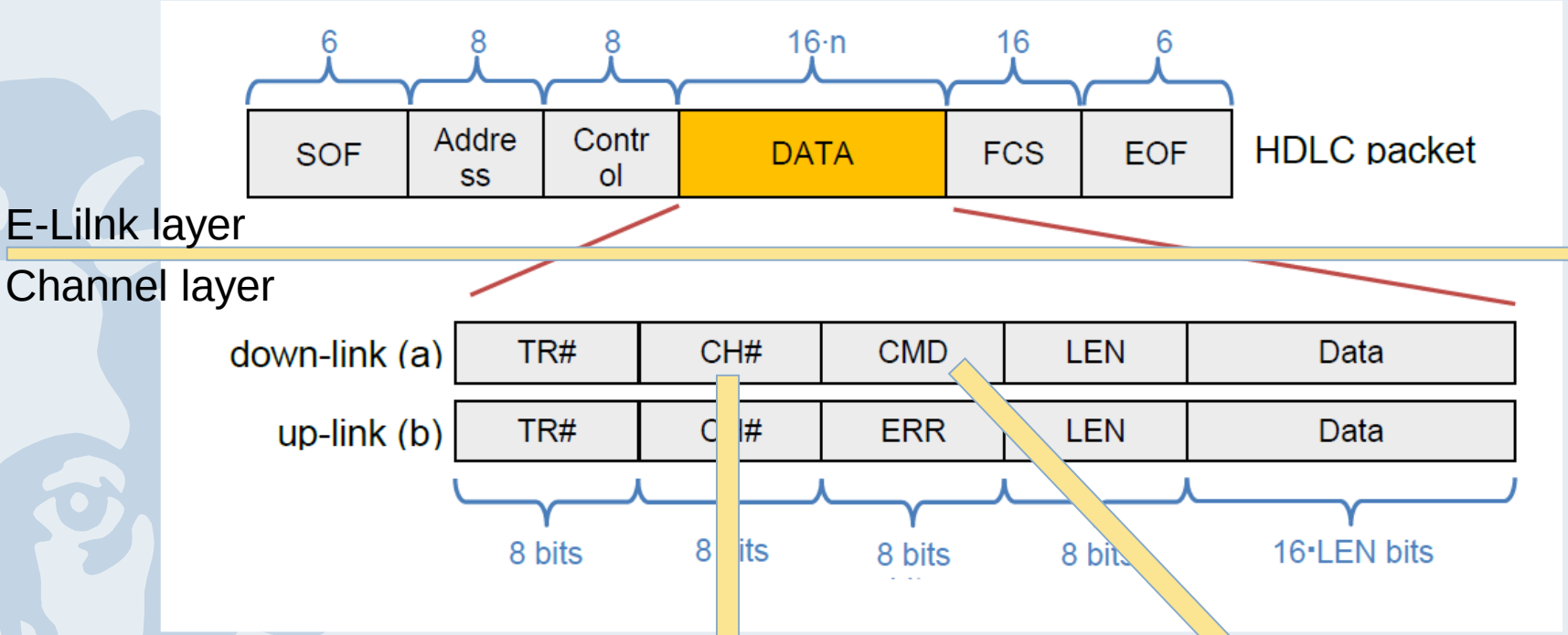


interface	Channel
GBT-SCA Configuration	0x00
GPIO	0x02
JTAG	0x13
I²C port 0	0x03

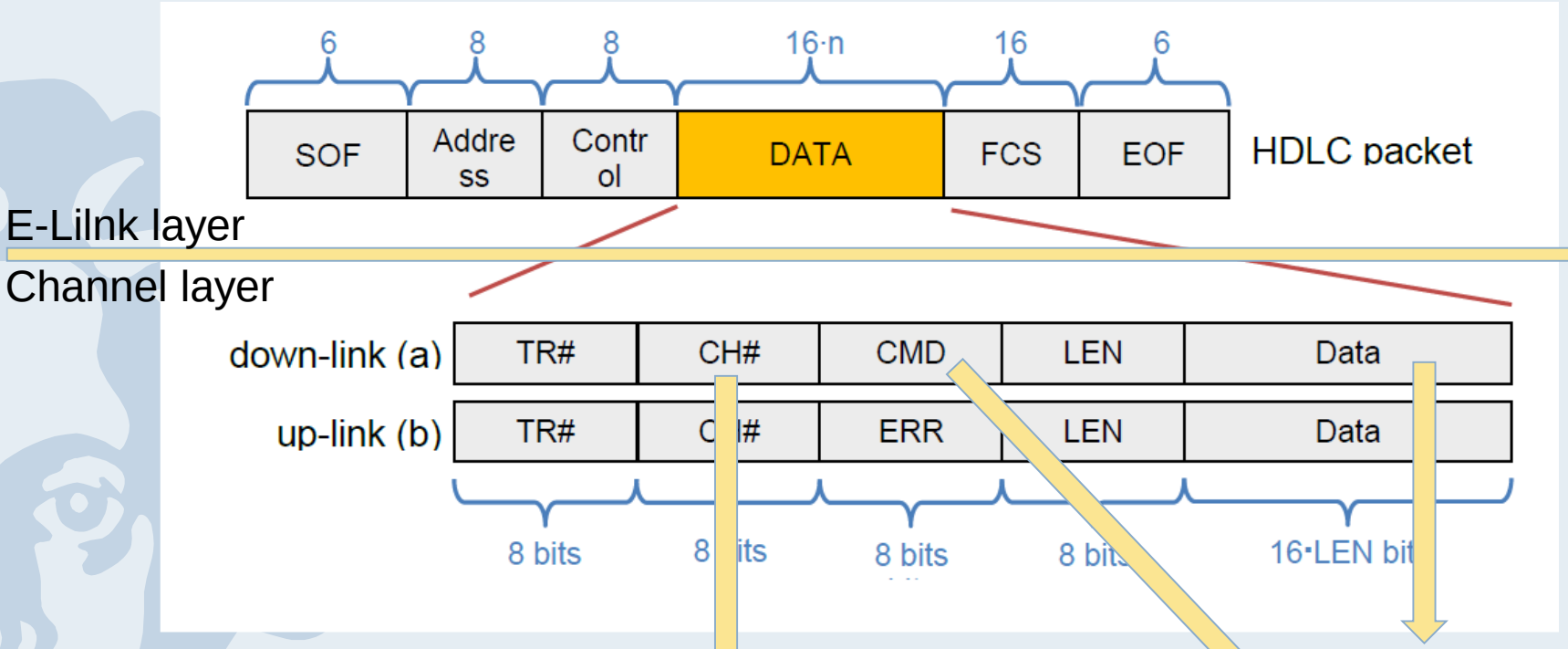
Example: How to enable GPIO channel



interface	Channel
GBT-SCA Configuration	0x00
GPIO	0x02
JTAG	0x13
I²C port 0	0x03

Action	Command
...	...
Read bits 0 to 7 from CH_EN registe	0x02
Write bits 0 to 7 of CH_EN register	0x03
...	...

Example: How to enable GPIO channel



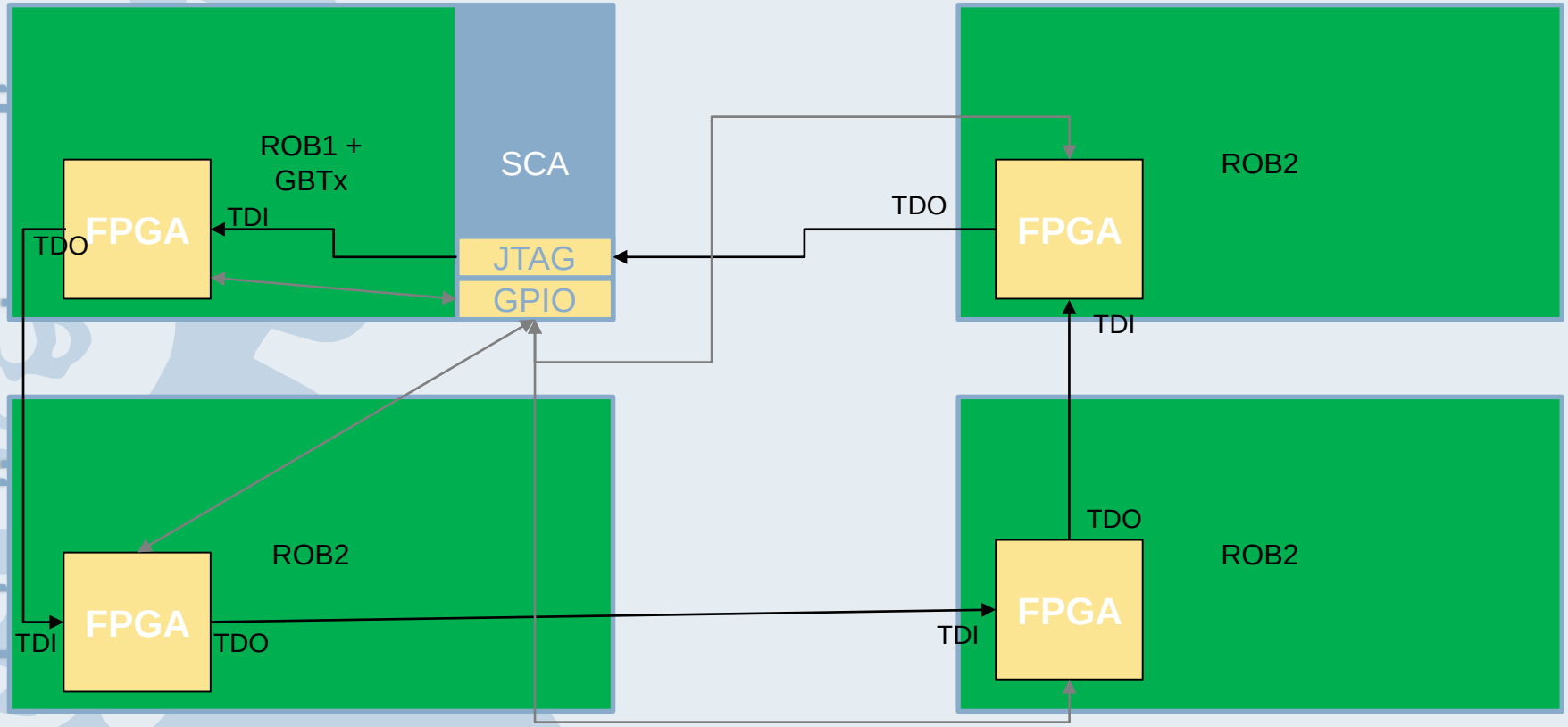
0x0004 (set register to 0x04)

interface	Channel
GBT-SCA Configuration	0x00
GPIO	0x02
JTAG	0x13
I²C port 0	0x03

Action	Command
...	...
Read bits 0 to 7 from CH_EN registe	0x02
Write bits 0 to 7 of CH_EN register	0x03
...	...

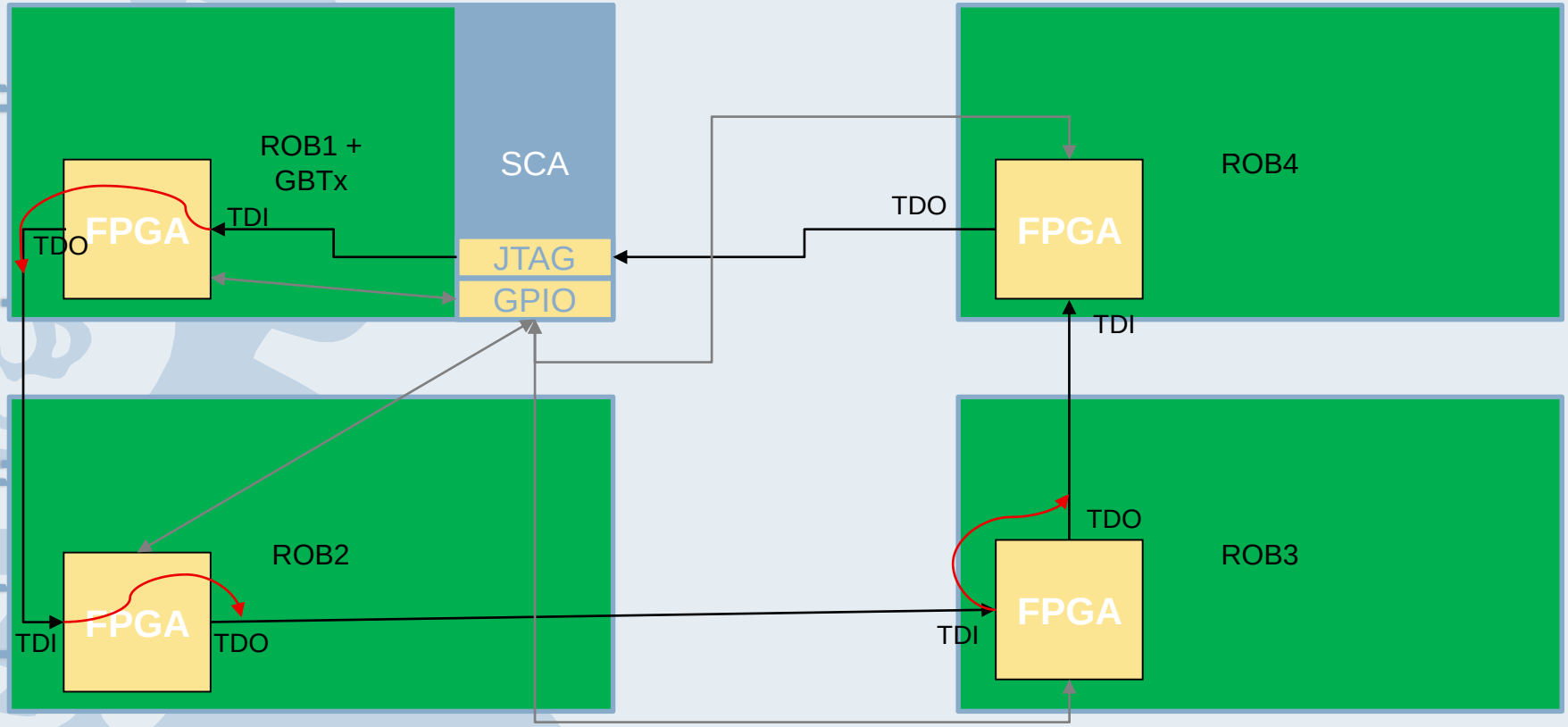
Current Approach

- **Strategy: Full configuration**
  - concatenate all bitfiles and push as one datastream:
    - FW1 + FW2 + FW3 + FW4 ⟶ SCA JTAG channel



Current Approach

- **Strategy: Partial reconfiguration**
  - Set unaffected devices to pass-through mode via JTAG
  - Push the partial bitfile for the affected device (ROB4)



Interfaces

- **JTAG : Selection of commands**

Configuration registers:

Command Name	CH	CMD	Description
JTAG_GO	0x13	0xA2	Starts JTAG transmission
JTAG_wrt_CTRL JTAG_rea_CTRL	0x13 0x13	0x80 0x81	Read/Write the core CONTROL register
JTAG_ wrt _DIV JTAG_rea_DIV	0x13 0x13	0x90 0x91	Read/Write the FREQUENCY register

TMS buffer registers:

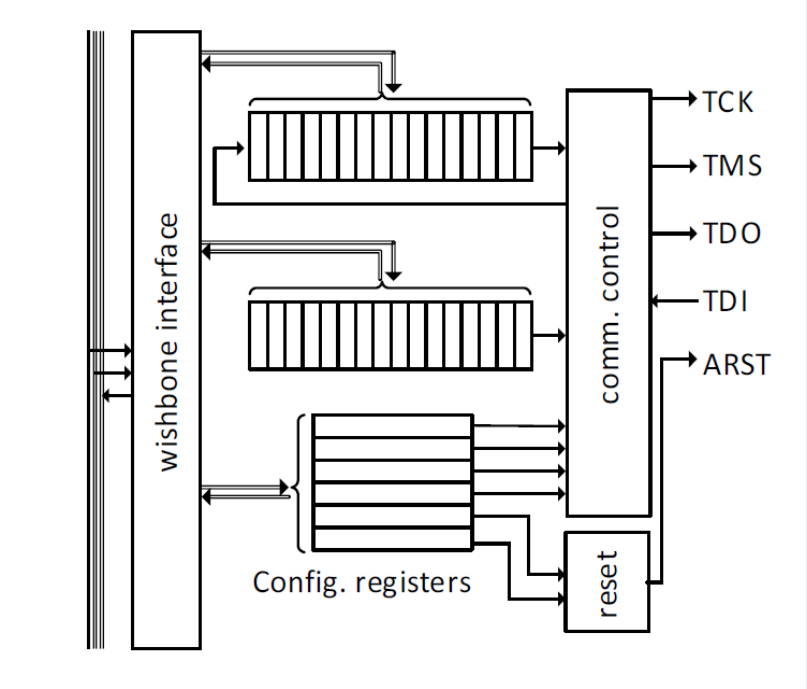
Command Name	CH	CMD	Description
JTAG_ TMS _wrt_Tx0 JTAG_ TMS _rea_Tx0	0x13 0x13	0x40 0x41	Read/Write the TMS register bits from 0 to 31
JTAG_ TMS _wrt_Tx1 JTAG_ TMS _rea_Tx1	0x13 0x13	0x50 0x51	Read/Write the TMS register bits from 32 to 63
JTAG_ TMS _wrt_Tx2 JTAG_ TMS _rea_Tx2	0x13 0x13	0x60 0x61	Read/Write the TMS register bits from 64 to 95
JTAG_ TMS _wrt_Tx3 JTAG_ TMS _rea_Tx3	0x13 0x13	0x70 0x71	Read/Write the TMS register bits from 96 to 127

TDO buffer registers:

Command Name	CH	CMD	Description
JTAG_ TDO_wrt_Tx0 JTAG_ TDO_rea_Tx0	0x13 0x13	0x00 0x01	Read/Write the TDO register bits from 0 to 31
JTAG_ TDO_wrt_Tx1 JTAG_ TDO_rea_Tx1	0x13 0x13	0x10 0x11	Read/Write the TDO register bits from 32 to 63
JTAG_ TDO_wrt_Tx2 JTAG_ TDO_rea_Tx2	0x13 0x13	0x20 0x21	Read/Write the TDO register bits from 64 to 95
JTAG_ TDO_wrt_Tx3 JTAG_ TDO_rea_Tx3	0x13 0x13	0x30 0x31	Read/Write the TDO register bits from 96 to 127

TDI buffer registers:

Command Name	CH	CMD	Description
JTAG_ TDI _rea_Rx0	0x13	0x01	Read the TDI register bits from 0 to 31
JTAG_ TDI _rea_Rx1	0x13	0x11	Read the TDI register bits from 32 to 63
JTAG_ TDI _rea_Rx2	0x13	0x21	Read the TDI register bits from 64 to 95
JTAG_ TDI _rea_Rx3	0x13	0x31	Read the TDI register bits from 96 to 127



Interfaces

- **JTAG : Loading FPGA configuration**

Configuration registers:

Command Name	CH	CMD	Description
JTAG_GO	0x13	0xA2	Starts JTAG transmission
JTAG_wrt_CTRL JTAG_rea_CTRL	0x13 0x13	0x80 0x81	Read/Write the core CONTROL register
JTAG_ wrt _DIV JTAG_rea_DIV	0x13 0x13	0x90 0x91	Read/Write the FREQUENCY register

TMS buffer registers:

Command Name	CH	CMD	Description
JTAG_ TMS _wrt_Tx0 JTAG_ TMS _rea_Tx0	0x13 0x13	0x40 0x41	Read/Write the TMS register bits from 0 to 31
JTAG_ TMS _wrt_Tx1 JTAG_ TMS _rea_Tx1	0x13 0x13	0x50 0x51	Read/Write the TMS register bits from 32 to 63
JTAG_ TMS _wrt_Tx2 JTAG_ TMS _rea_Tx2	0x13 0x13	0x60 0x61	Read/Write the TMS register bits from 64 to 95
JTAG_ TMS _wrt_Tx3 JTAG_ TMS _rea_Tx3	0x13 0x13	0x70 0x71	Read/Write the TMS register bits from 96 to 127

TDO buffer registers:

Command Name	CH	CMD	Description
JTAG_ TDO_wrt_Tx0 JTAG_ TDO_rea_Tx0	0x13 0x13	0x00 0x01	Read/Write the TDO register bits from 0 to 31
JTAG_ TDO_wrt_Tx1 JTAG_ TDO_rea_Tx1	0x13 0x13	0x10 0x11	Read/Write the TDO register bits from 32 to 63
JTAG_ TDO_wrt_Tx2 JTAG_ TDO_rea_Tx2	0x13 0x13	0x20 0x21	Read/Write the TDO register bits from 64 to 95
JTAG_ TDO_wrt_Tx3 JTAG_ TDO_rea_Tx3	0x13 0x13	0x30 0x31	Read/Write the TDO register bits from 96 to 127

TDI buffer registers:

Command Name	CH	CMD	Description
JTAG_ TDI _rea_Rx0	0x13	0x01	Read the TDI register bits from 0 to 31
JTAG_ TDI _rea_Rx1	0x13	0x11	Read the TDI register bits from 32 to 63
JTAG_ TDI _rea_Rx2	0x13	0x21	Read the TDI register bits from 64 to 95
JTAG_ TDI _rea_Rx3	0x13	0x31	Read the TDI register bits from 96 to 127

Adaptive Equalizer Tests

Mitigation of permanent faults in adaptive equalizers