university of groningen

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Readout of the PANDA Electromagnetic Calorimeter

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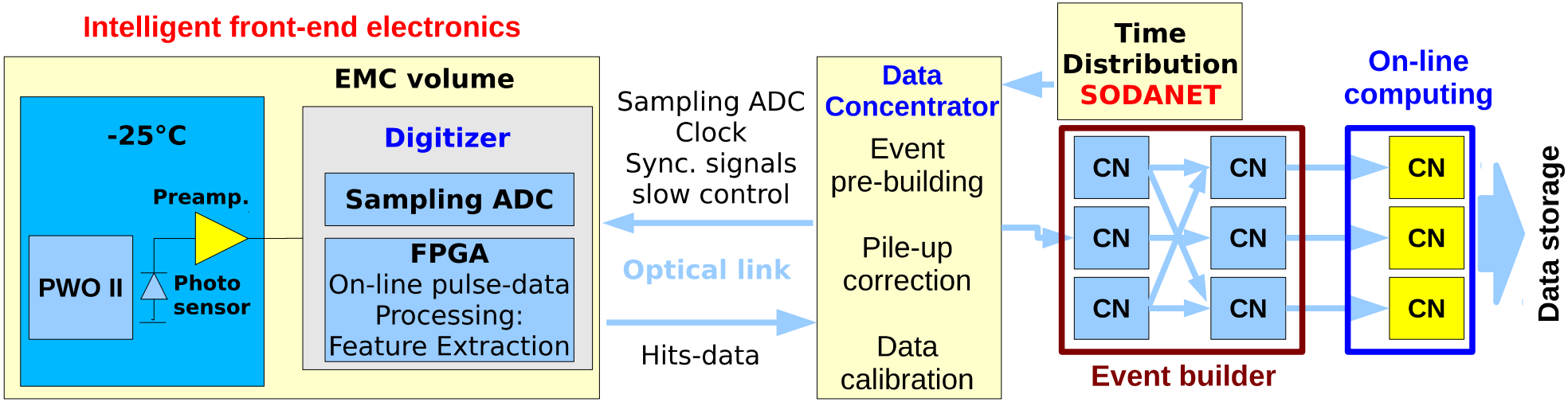
for the PANDA collaboration

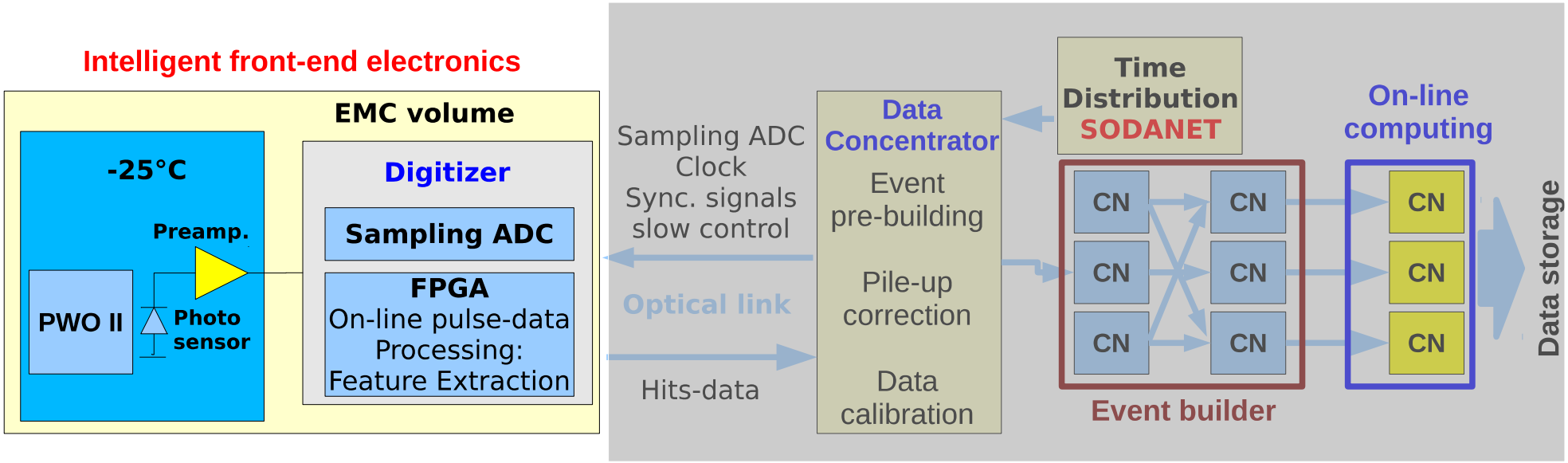
EMC-Readout Scheme

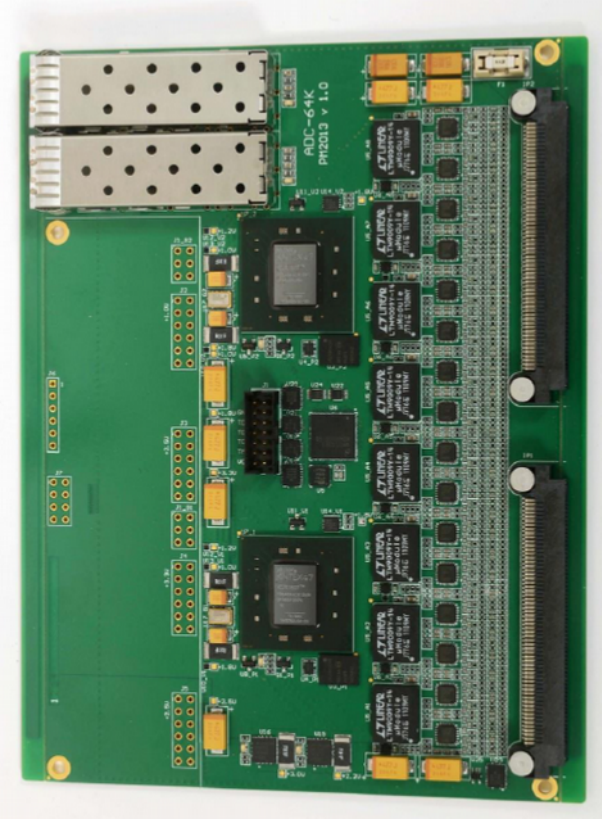


Components of the EMC readout:

- Intelligent front-end: **digitizer**
- Time-distribution system
- Data concentrators
- Burst-building network
- On-line computing

EMC Front-End Electronics



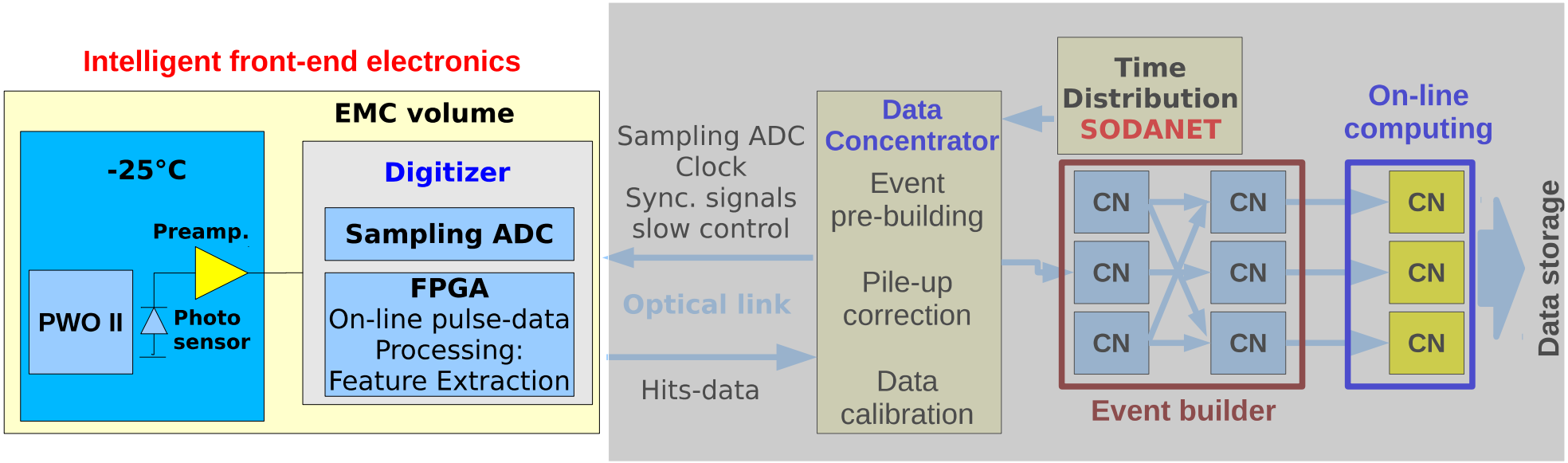


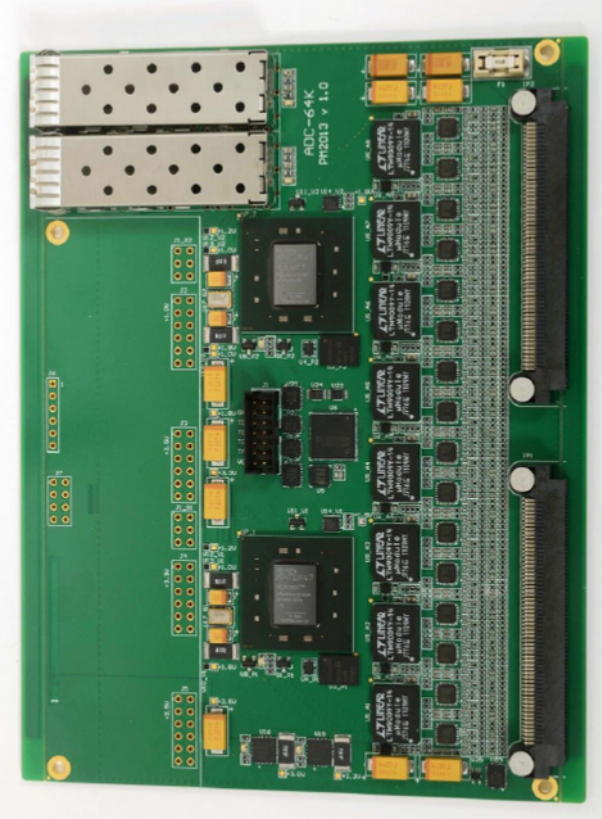
EMC digitizer:

- 64 ADC channels (32 dual-gain readout channels)
- 14 bit resolution
- 80-125 MHz sampling rate
- On-line detection of hits, extraction of hit information, pulse pile-up recovery by two Xilinx Kintex-7 FPGAs

Digitizers are located in radiation area → precautions have to be taken against configuration changes and SEU in FPGAs

EMC Front-End Electronics

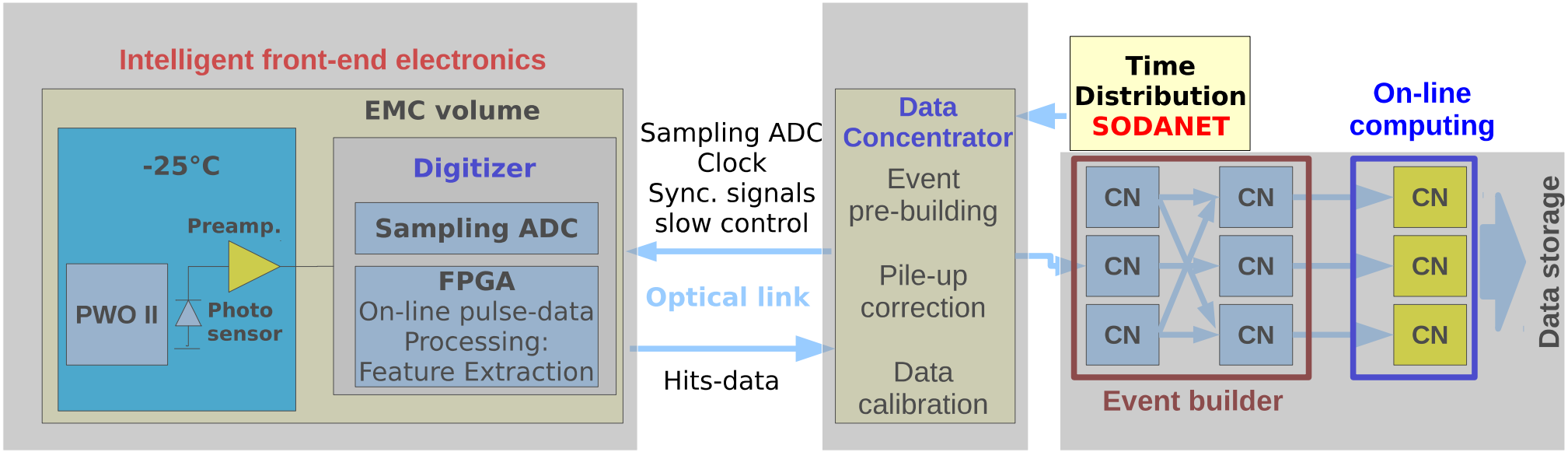




Feature Extraction:

- Base-line follower
- Pulse detection
- Pile-up detection (output waveforms)
- Precise time
- Precise energy
- Diagnostics: Possibility to readout raw ADC data (access to the noise-level measurement)
- **To be done**: self-monitoring for configuration errors, triple redundancy

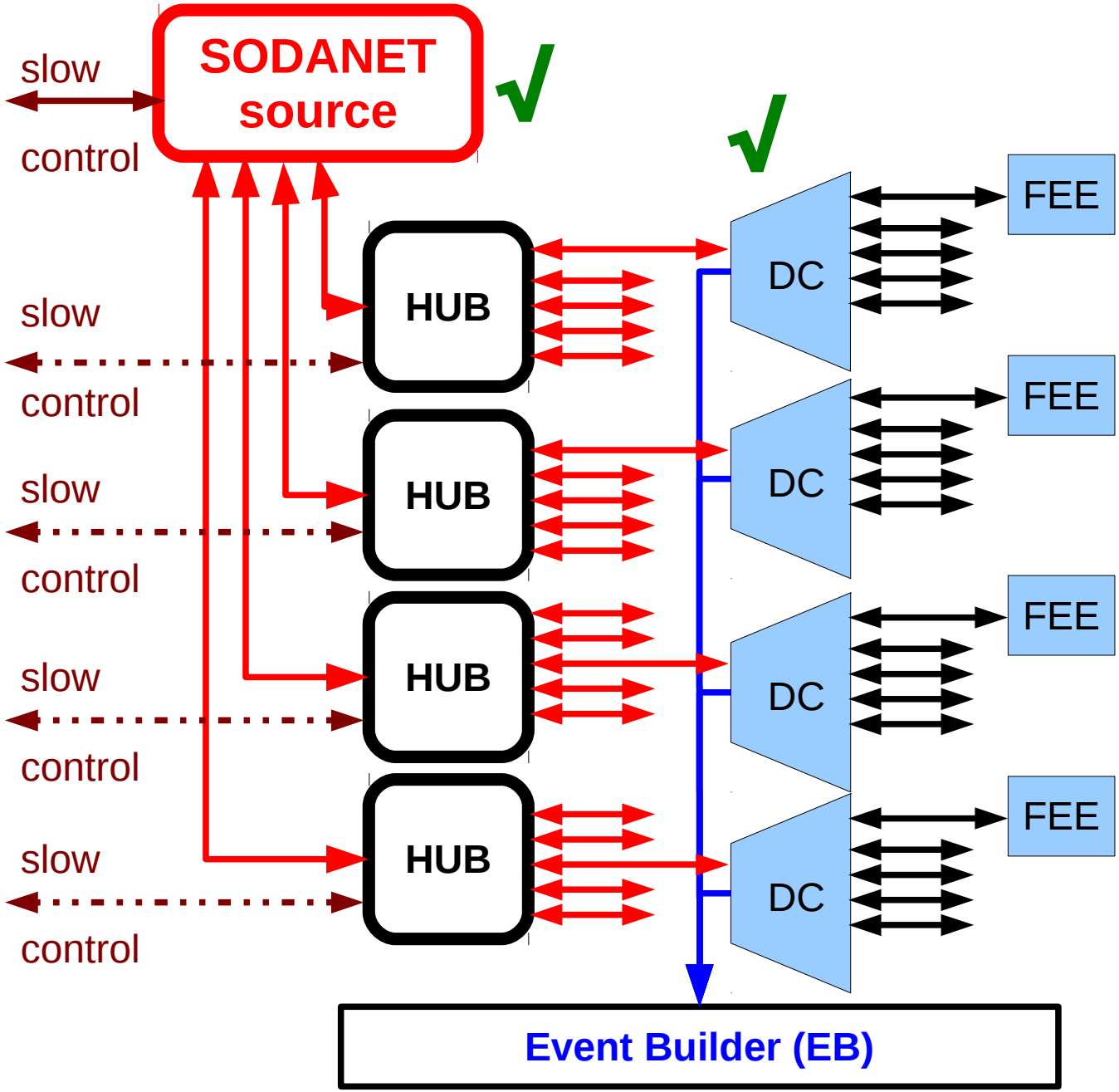
Time Distribution



SODANET provides:

- synchronization of the FEE
- Continuous monitoring of the Data Concentrator (**DC**) or FEE functionality
- Initial rough (~10ns) time calibration of the propagation time of the synchronization signal
- Transfer of a slow-control (FEE configuration/status) information

SODANET Topology



SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
  - DC → source: slow control, used for time calibration

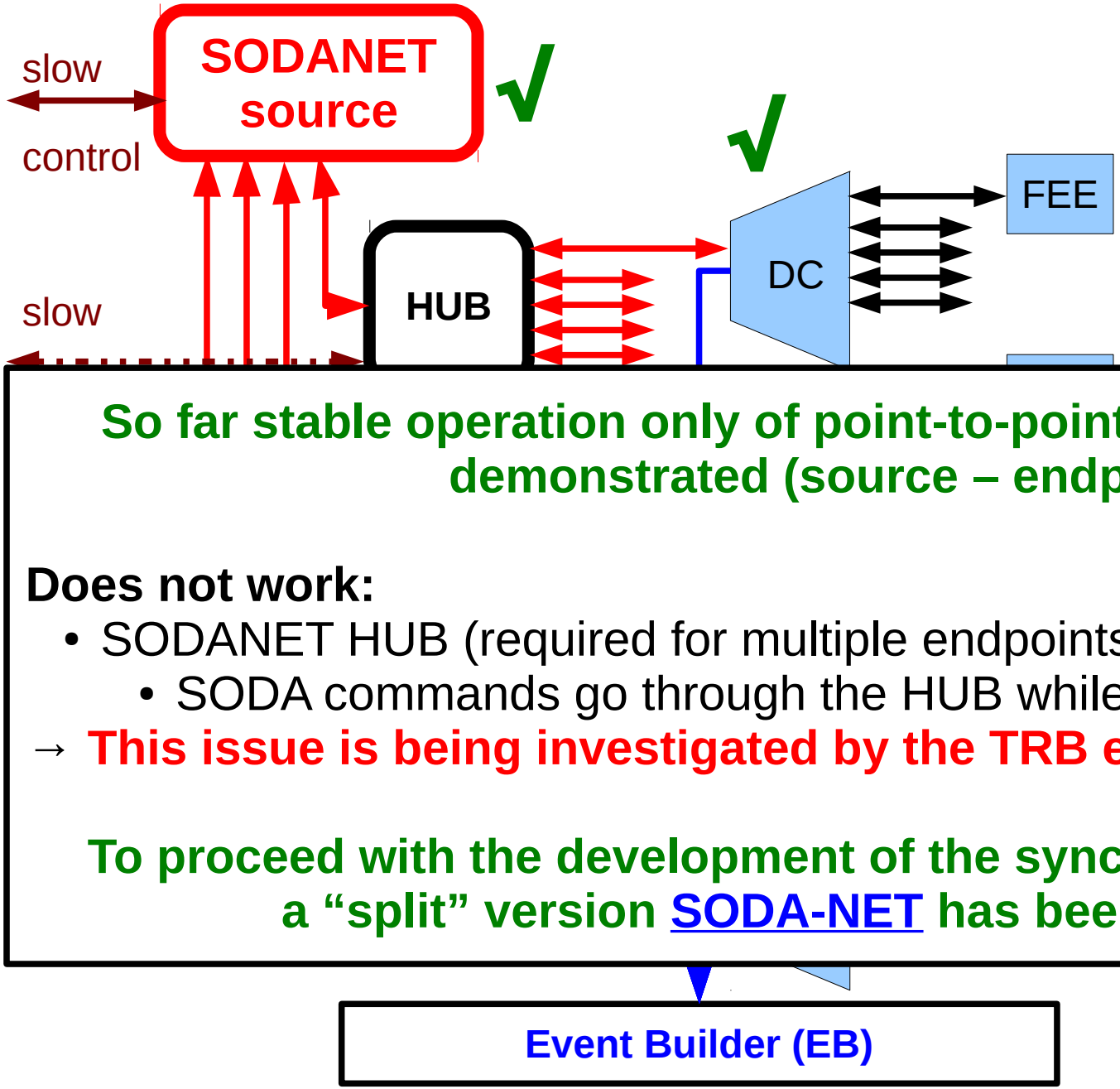
Data link (DC → EB):

- Unidirectional Ethernet

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

SODANET Topology



SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC:
    synchronous
- Protocol up to subsystem

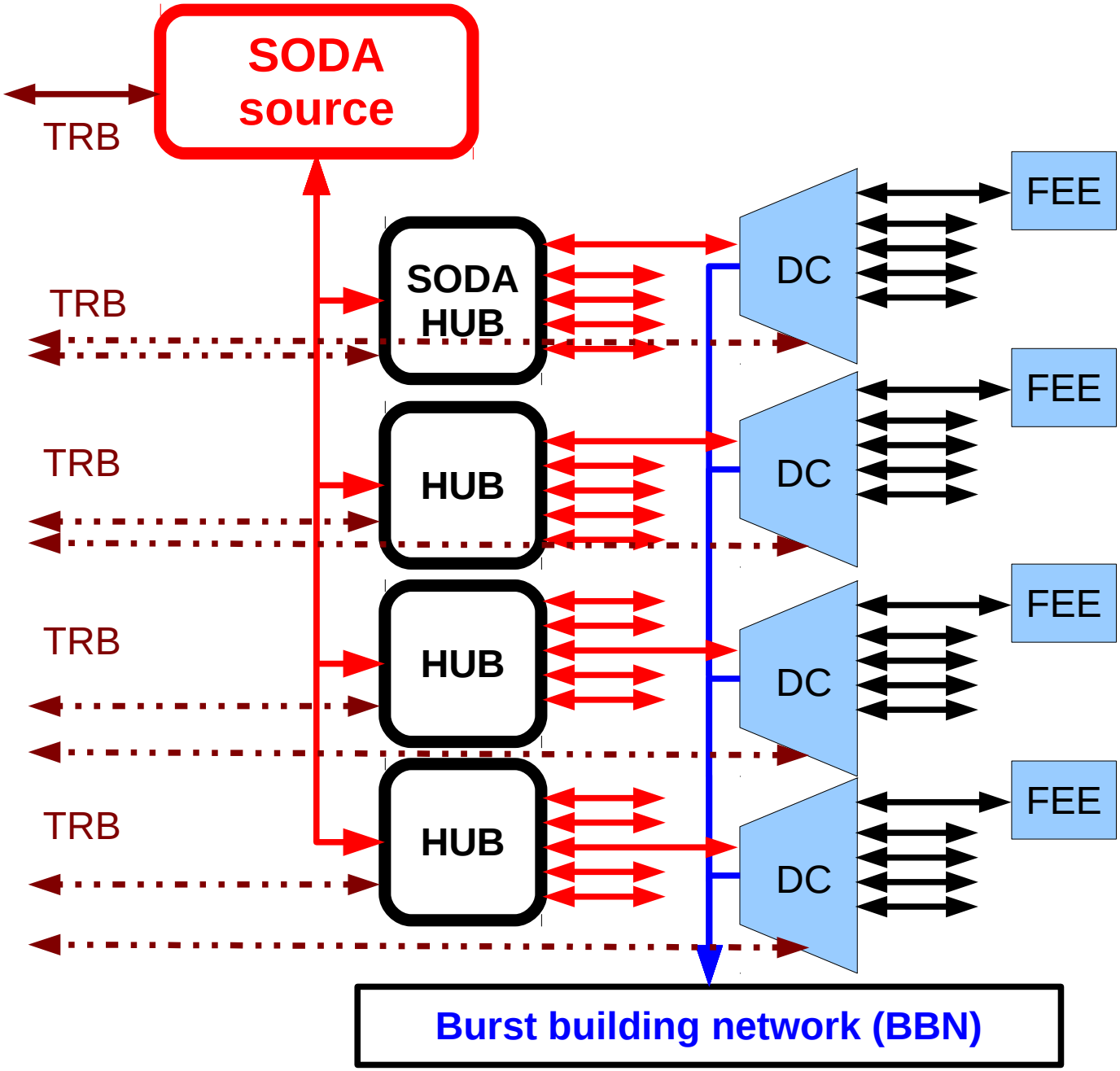
So far stable operation only of point-to-point SODANET link was demonstrated (source – endpoint)

Does not work:
- SODANET HUB (required for multiple endpoints):
  - SODA commands go through the HUB while the TRB hub is hanging

→ **This issue is being investigated by the TRB expert (Jan Michel)**

To proceed with the development of the synchronization protocol a "split" version SODA-NET has been developed

SODA-NET



SODA link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information
  - DC → source: slow control, used for time calibration

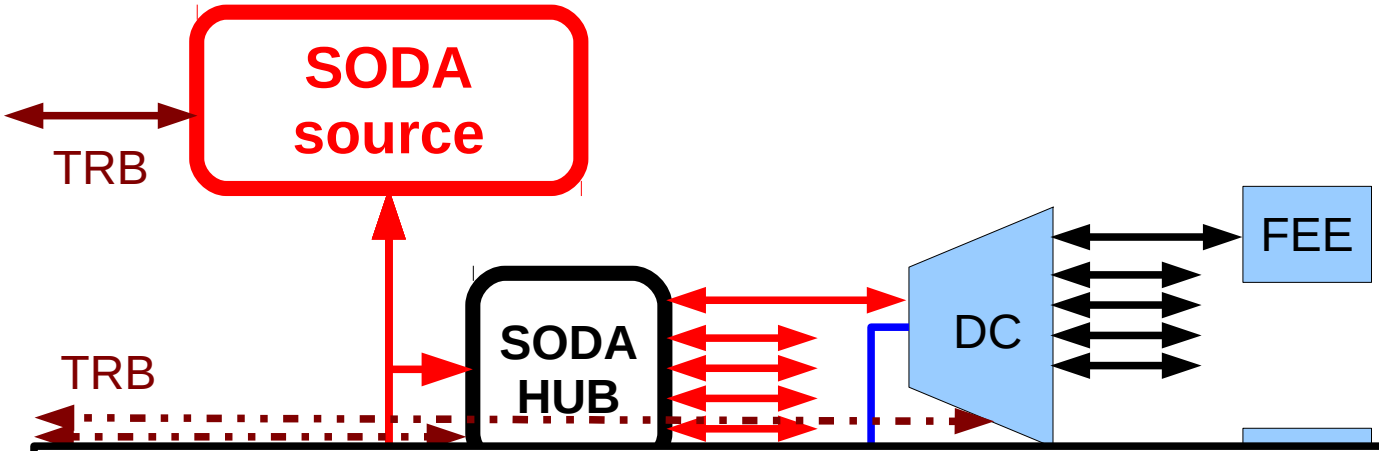
Data link (DC → BBN):

- Unidirectional

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

SODA-NET



SODA link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC:

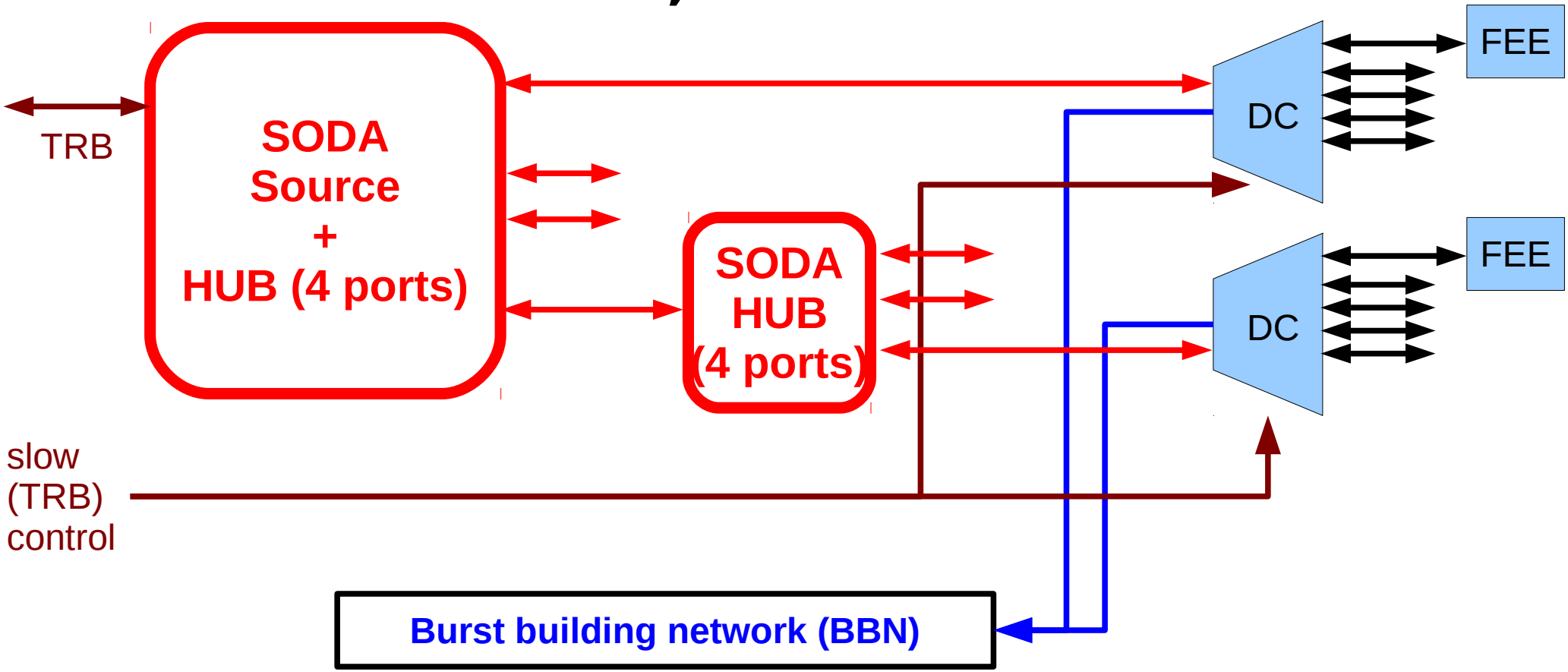
SODA-NET allows:

- To test performance of the time-distribution network in terms of jitter, scalability of the system
- To develop data concentrator firmware (migration from SODA-NET to SODANET is straightforward)
- To build complex readout systems with multiple DC/FEE modules

subsystem

Burst building network (BBN)

SODA-NET, Current Status

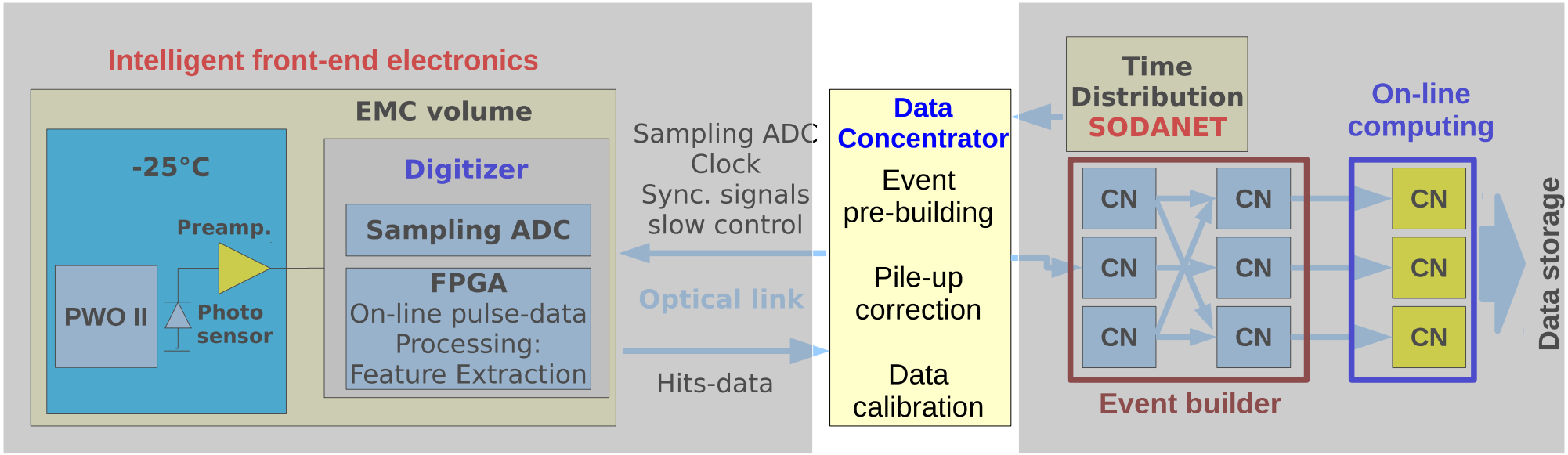


Prototype of the system with all components (two TRB boards and two EMC digitizers) operates stable: first tests are successful.

After completion of the tests with a small-scale system, larger system is required for scalability tests (>ten TRB board)

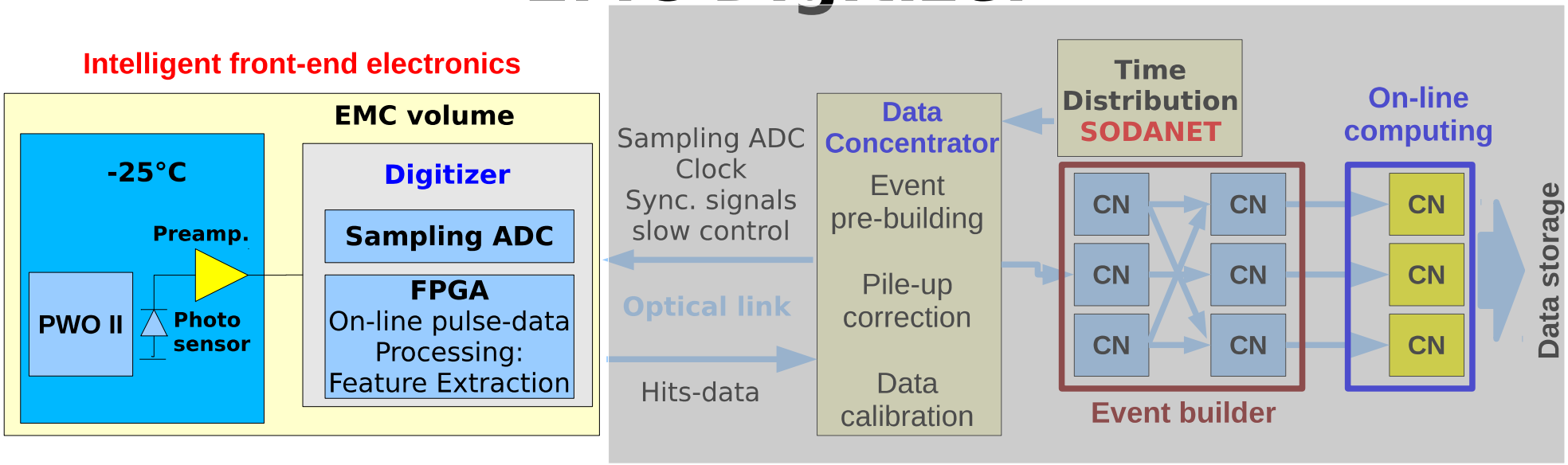
All subsystems should start using the SODA-NET

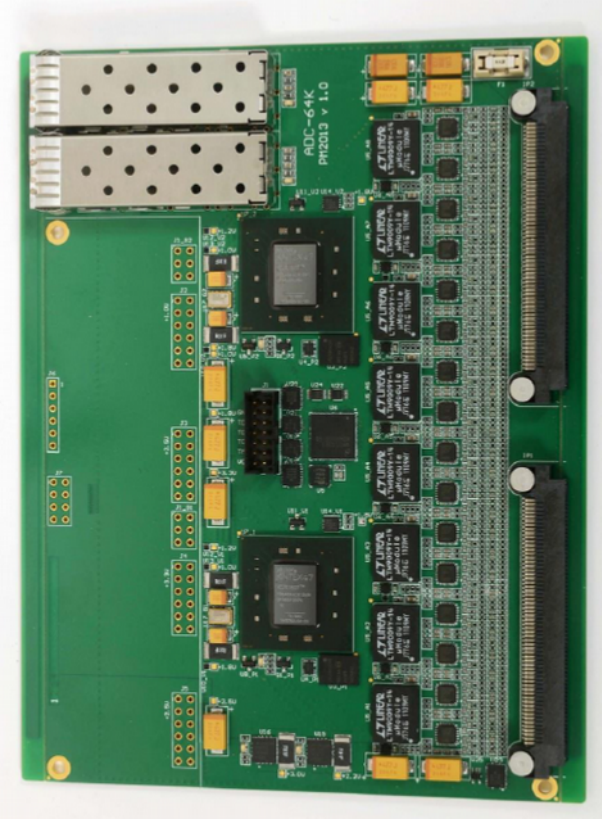
Data Concentrator



- **Data concentrator:**
  - Running on TRB3 board and WASA VME board (Virtex 6)
  - Receiving Waveforms and Hit-data over fiber from FEE
  - **Energy calibration for each ADC channel (low and high gain separately)**
  - **Superburst building**
  - Put each Waveform in one Panda data-packet (debugging mode)
  - Send Panda data-packets over fiber to UDP translator
  - **Slow Control with SODANET**
  - **Combine hits from two digitizers corresponding to the same crystal**
  - Additional features: on-line histogram, data monitoring (hits and waveforms), error detection and counting

EMC Digitizer



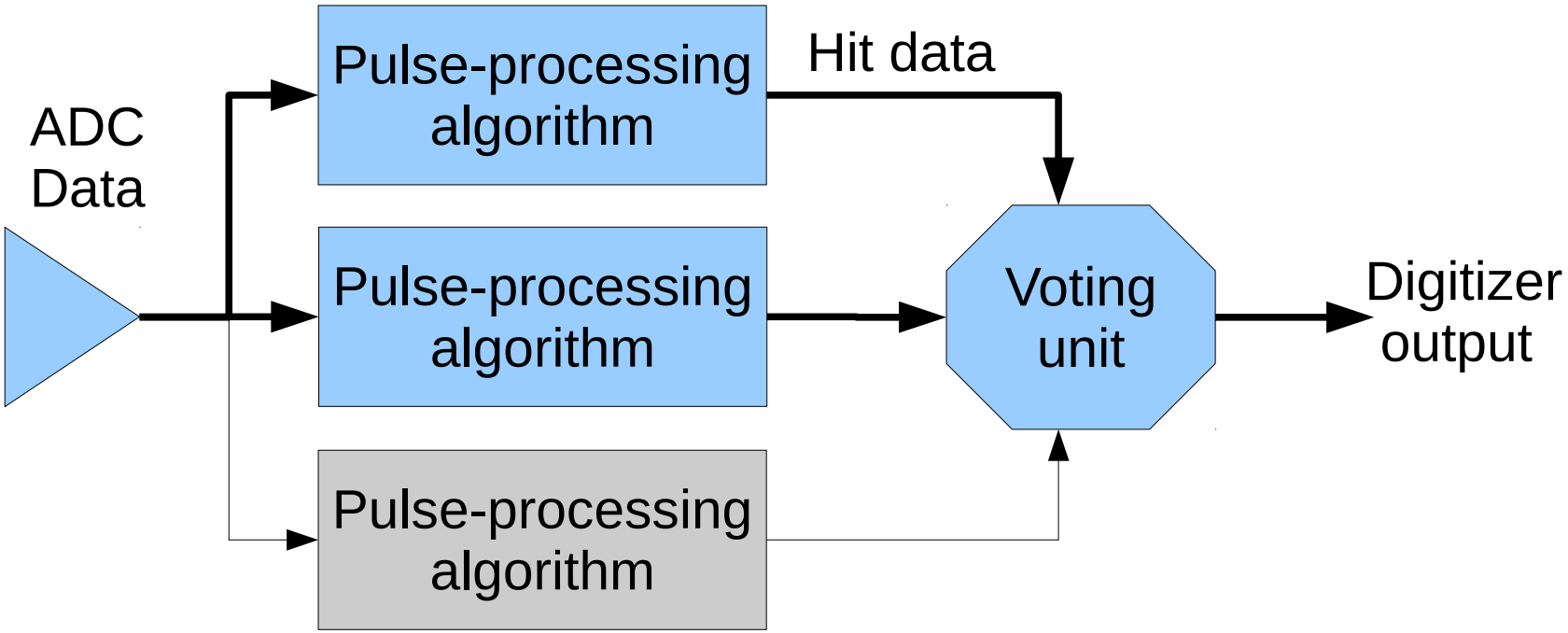


EMC digitizer, new developments:

- Triple Modular Redundancy
- Fast reboot sequence
- Measured SEU probability

Triple Modular Redundancy (TMR)

Current implementation contains double redundancy:
in case of SEU, the output of one module will be corrupted.
Measurement: **~ 2 ms** recovery time after SEU error



TMR is feasible for implemented data-processing algorithm

The Virtex-6 version of the digitizer has not enough resources for TMR

Pulse-processing algorithm is occupying ~15% of Kintex-7 FPGA
→ **enough resources to implement TMR**

Radiation-Hardness Test

Irradiation of Virtex-5 and Kintex-7 FPGAs:

- Irradiations were performed at KVI-CART, Groningen, the Netherlands
  - Proton beam: 150 MeV
  - Homogeneous irradiation field covers complete FPGA package
  - Fluence per irradiation cycle of about 10s: 10^7 – 10^8 P/cm^2

- FPGAs were configured to constantly compare content of registers and memory blocks (SEU check)

- At the end of irradiation cycle number of configuration errors were measured, FPGA was reconfigured

- Some configuration changes, induced by radiation damage, disabled readout of SEU number; such irradiation cycles were discarded for the measurement of the SEU probability

- SEUs were observed only in combination with configuration changes

  → measured SEU probability corresponds to the upper limit

Radiation-Hardness Test, Summary

- **Radiation hardness**
  - Kintex-7 is less prone for the configuration changes (factor 3) even without taking into account that is has much more resources (factor 10)
  - During the measurements it was never observed SEU without a single configuration change →
    SEU is much less probable then the configuration change
  - Digitizer, based on standard FPGA, can be used in PANDA EMC (54 min operation without reconfiguration with safety factor 10)

- **Issues:**
  - Flash memory of the digitizers may be corrupted by ionizing radiation → determine lifetime
  - SFP modules are not radiation hard → determine lifetime

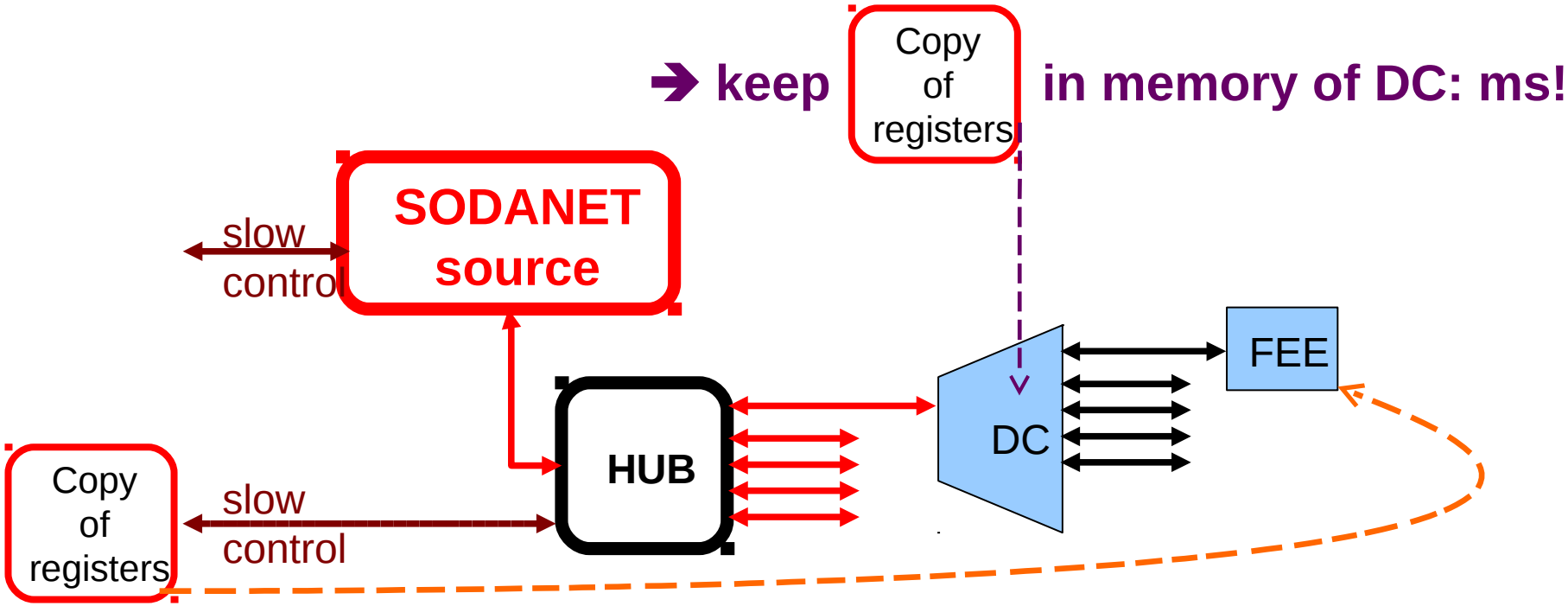
Recovery of EMC Digitizer

configuration change requires restart:

- reconfigure FPGA
- reprogram registers used by the on-line feature-extraction algorithm

Fast reprogramming is crucial for decreasing the dead time:

too slow (~seconds) via slow control



Together with a fast reload of configuration from a flash memory: implemented reboot procedure should take ~ 10 ms

Summary

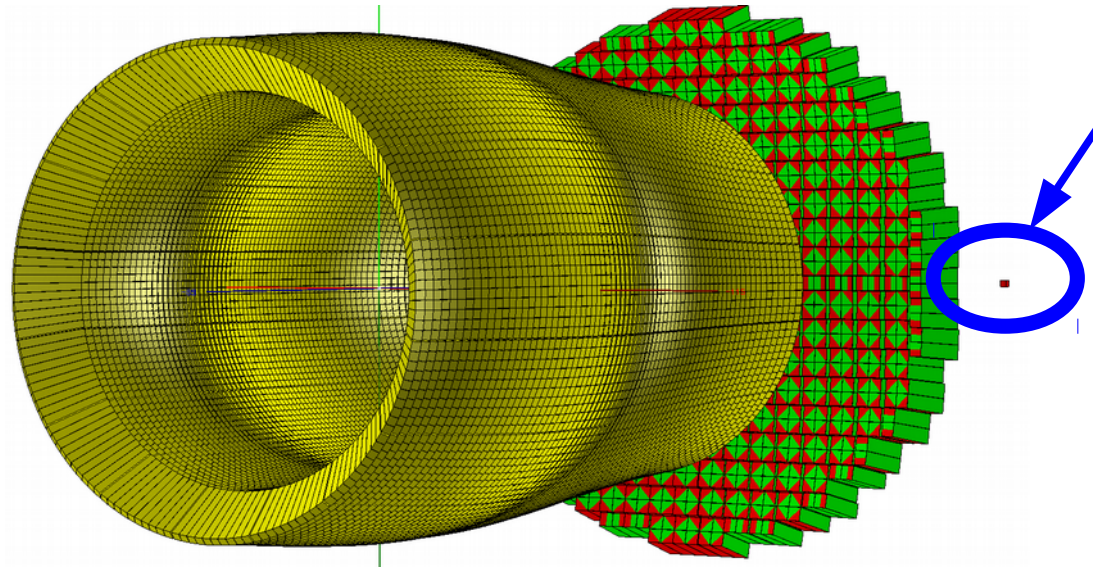
- **The EMC readout prototype is ready for larger-systems tests**
  → require more available hardware

- **SODA-NET is ready for implementation for ALL PANDA subsystems**

Expected Particle-Flux at FPGA Location

Monte Carlo input:

- Flux of charge particles and neutrons

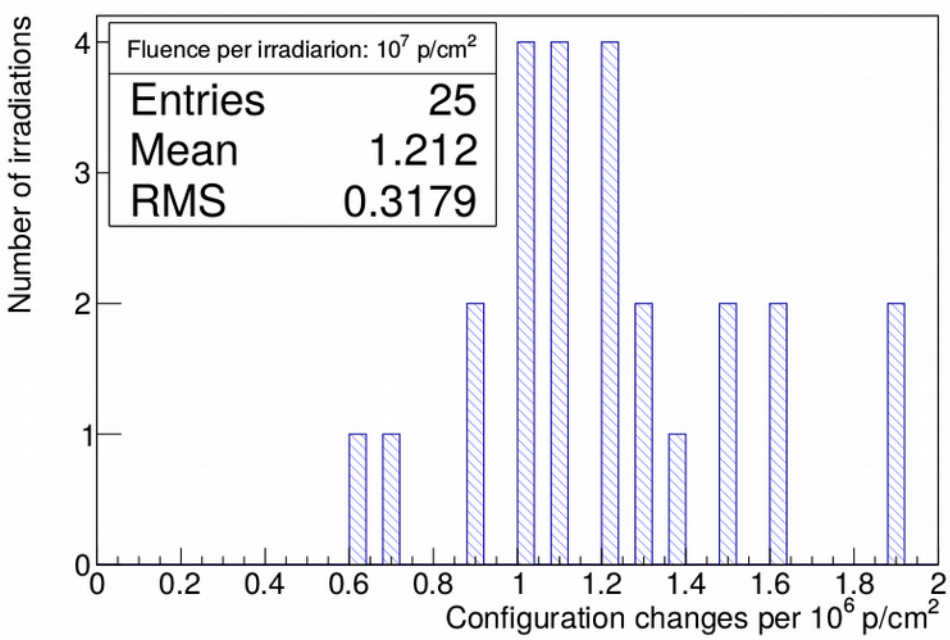


- FPGA on the EMC digitizer implemented in PANDAroot
- Estimated flux of charge particles: ~ 70 particles/s/cm^2
- **Neutron flux to be estimated:** FLUKA simulation is required

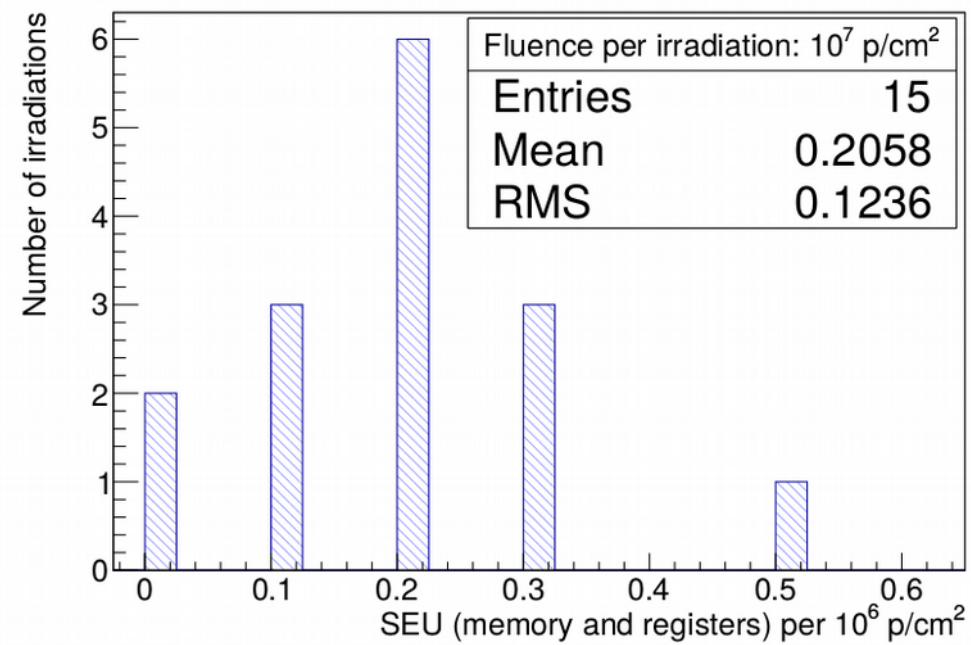
Hossein Moeini, Ganesh Tambave

Irradiation of Virtex-5
(XC5VLX50T)

Configuration changer per 10^6 p/cm^2



SEU per 10^6 p/cm^2



Experiment conditions:

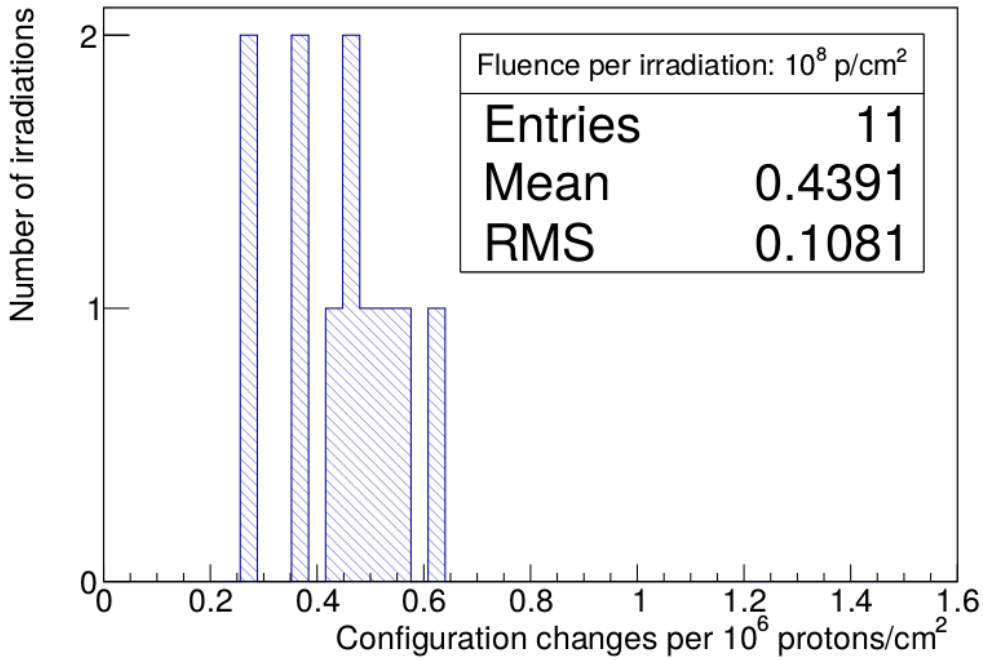
- Number of irradiation cycles: **25**
- Resources involved in the SEU test:
  - Registers: **64%** ($1.8 \cdot 10^4$ kB)
  - Block ram: **55%** ($1.1 \cdot 10^3$ kB)

Averaged number of:

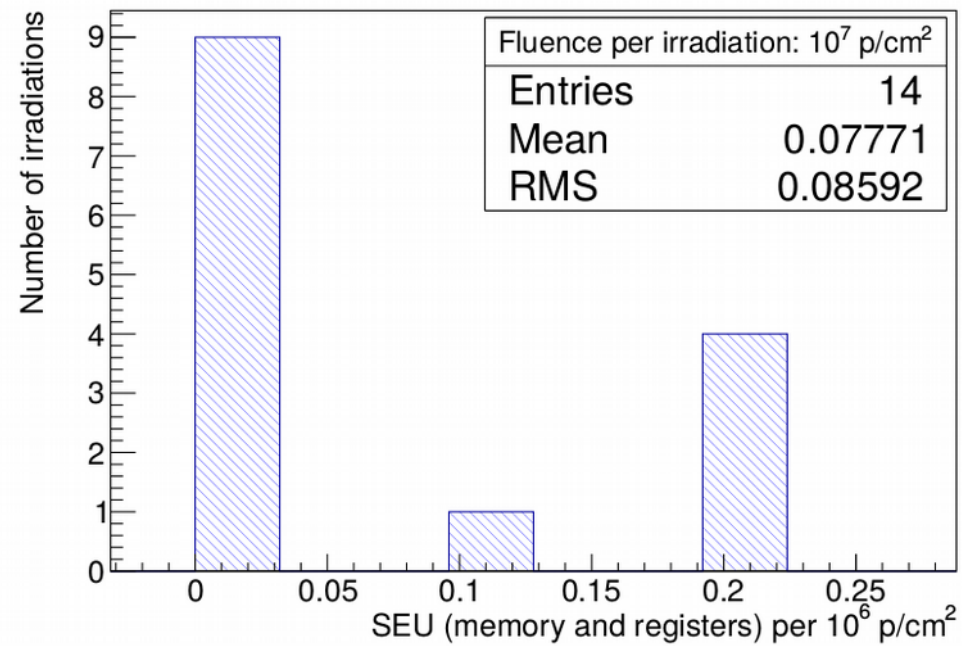
- configuration changes: 1.2(3) pre 10^6 p/cm^2
- SEU events: 0.2(1) pre 10^6 p/cm^2

Irradiation of Kintex-7
(XC7K325T)

Configuration changer per 10^6 p/cm^2



SEU per 10^6 p/cm^2



Experiment conditions:

- Number of irradiation cycles: **11**
- Resources involved in the SEU test:
  - Registers: **54%** ($2.2 \cdot 10^5$ kB)
  - Block ram: 86**%** ($1.4 \cdot 10^4$ kB)

Averaged number of:

- configuration changes: 0.46(13) pre 10^6 p/cm^2
- SEU events: 0.08(8) pre 10^6 p/cm^2

~54 minutes of operation before reconfigure with safety factor of 10

Synchronous Packages

- Have highest priority (interrupt any other transfer)
- Each received SODANET packed – acknowledged:
  continuous monitoring of the readout
  - Malfunction of one of the DC/FEE → trigger slow control;
    the malfunction DC – added to the list of non-uses recipients

- Burst counting (within Super-burst) – at each DC
  Error handling:
  - DC checks if received super-burst number is sequential
  - In case of error:
    - the DC uses number distributed by the SODANET,
    - set special error bit in the output data,
    - informs slow-control system
  - If part of SODANET message is missing:
    - DC uses super-burst number from a local counter,
    - reports problem to the slow-control system.