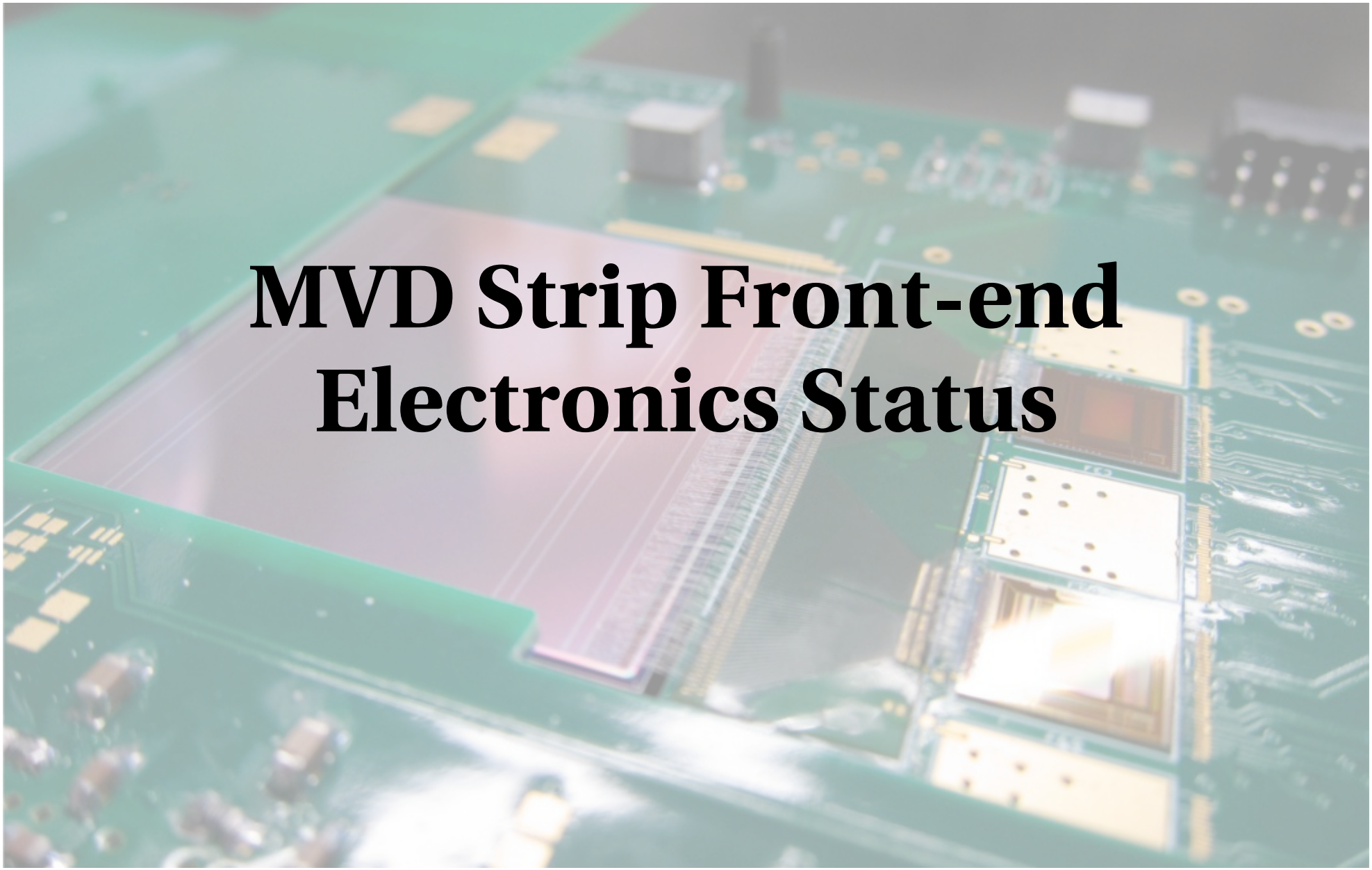
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

II. Physikalisches Institut

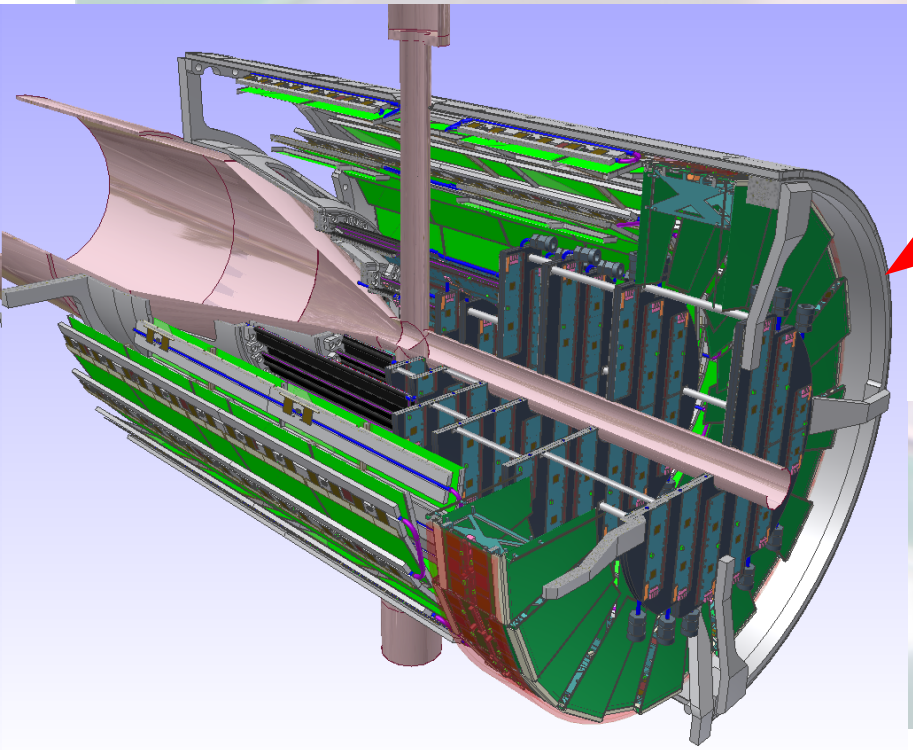


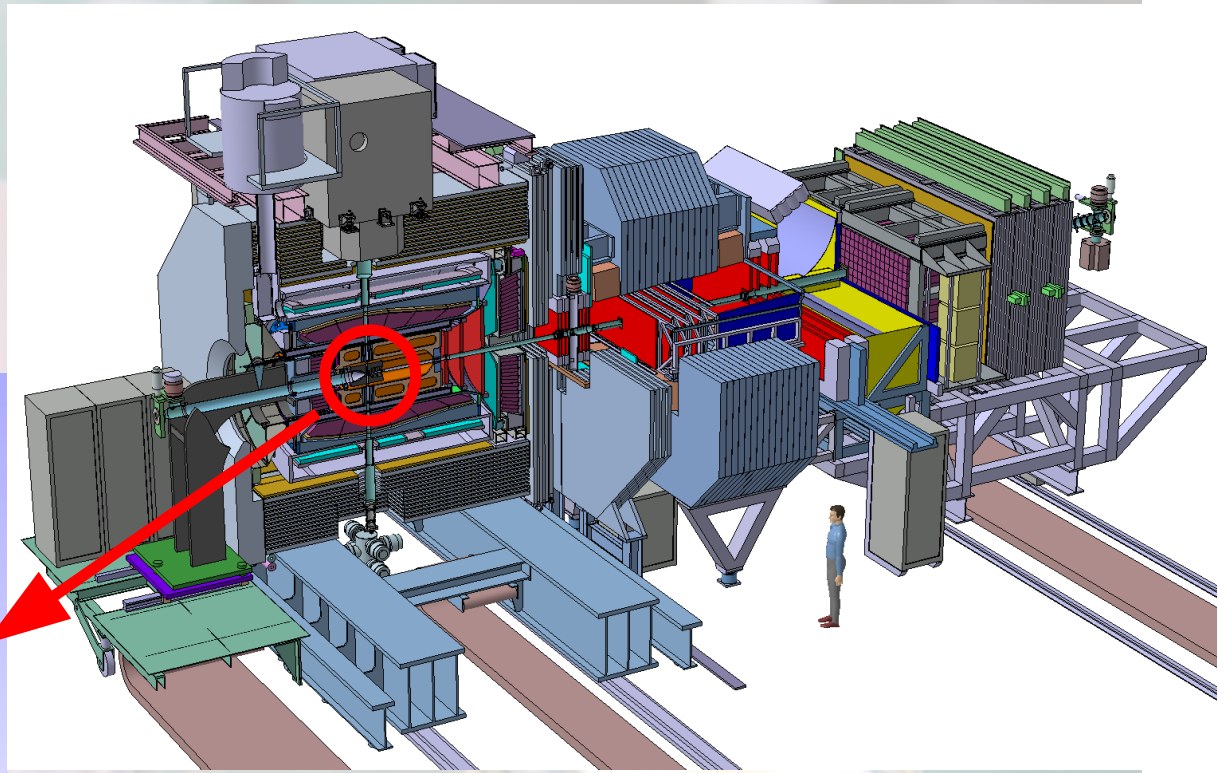
MVD Strip Front-end Electronics Status

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN
II. Physikalisches Institut

The $\overline{\text{P}}$ANDA MVD Strip Detector

-Innermost detector of the $\overline{\text{P}}$ANDA Target Spectrometer
-Located at the crossing of beam pipe and target pipe

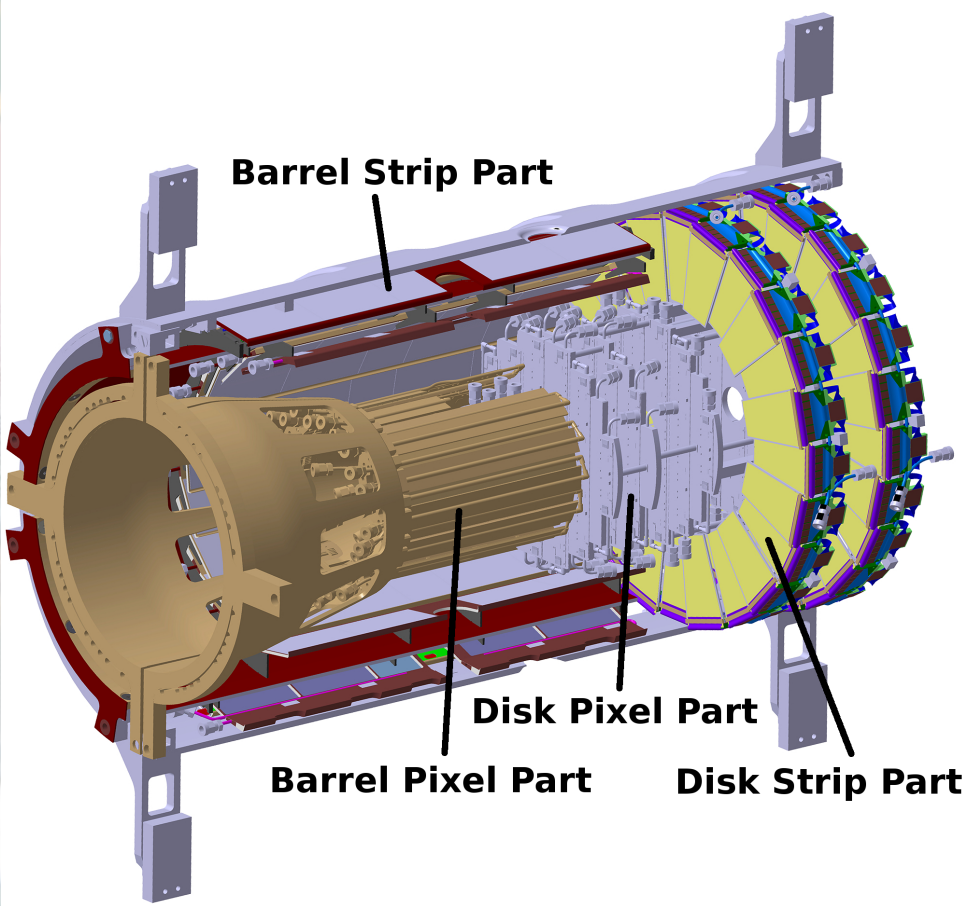




-Tracking of charged particles
-Vertex reconstruction for primary and secondary vertices
-Improvement of momentum resolution and PID

The $\overline{\text{P}}$ANDA MVD Strip Detector

- Hybrid silicon pixel sensors
- Double-sided silicon strip sensors
  - 4 barrel layers
    - 2 pixel barrels
    - 2 strip barrels
  - 6 disk layers
    - 4 pixel disks
    - 2 mixed disks (inner pixel, outer strips)



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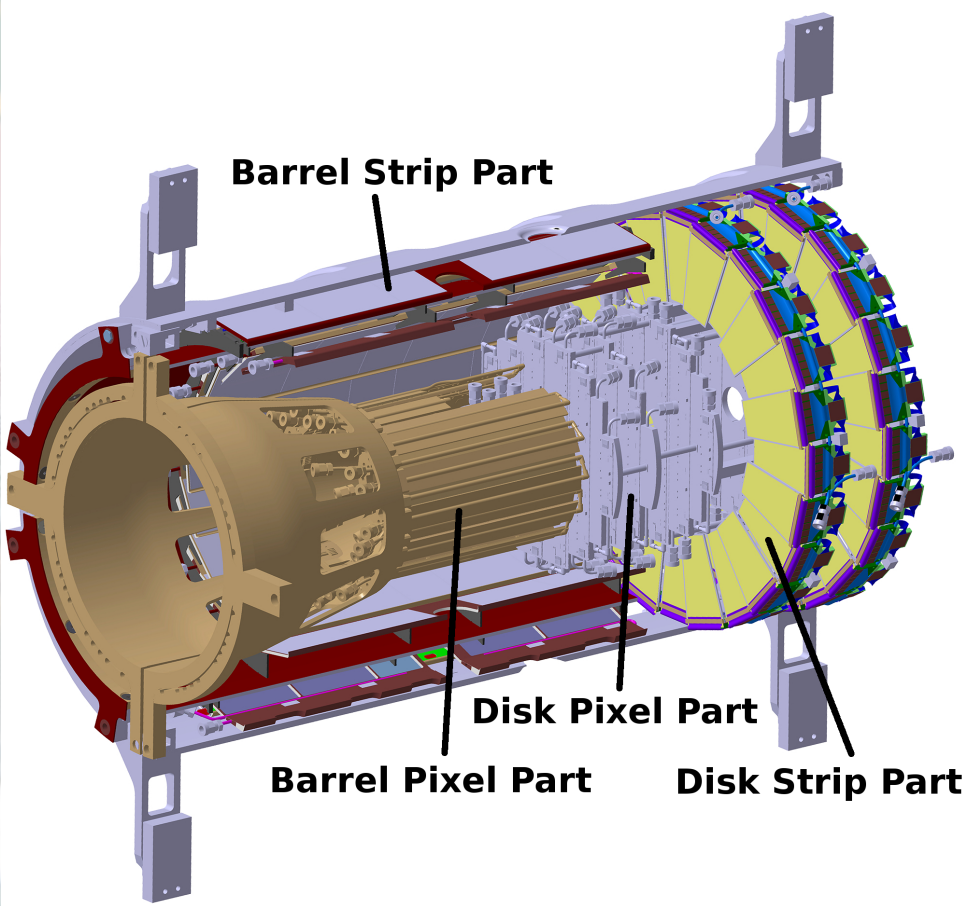
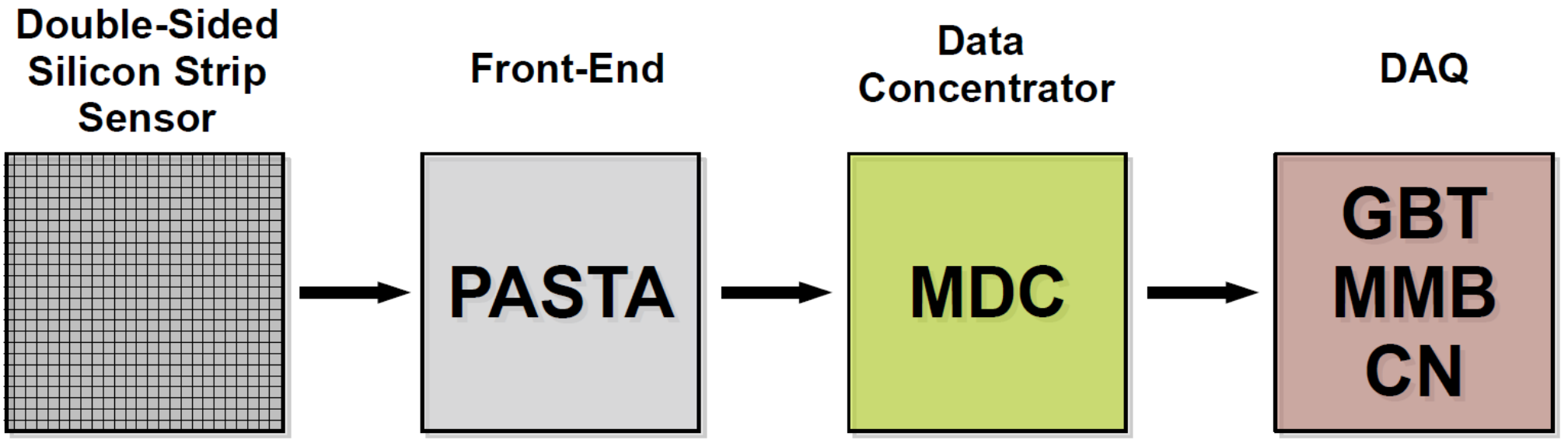
- Double-sided silicon strip sensors
  - 4 barrel layers
    - 2 pixel barrels
    - 2 strip barrels
  - 6 disk layers
    - 4 pixel disks
    - 2 mixed disks
      (inner pixel, outer strips)

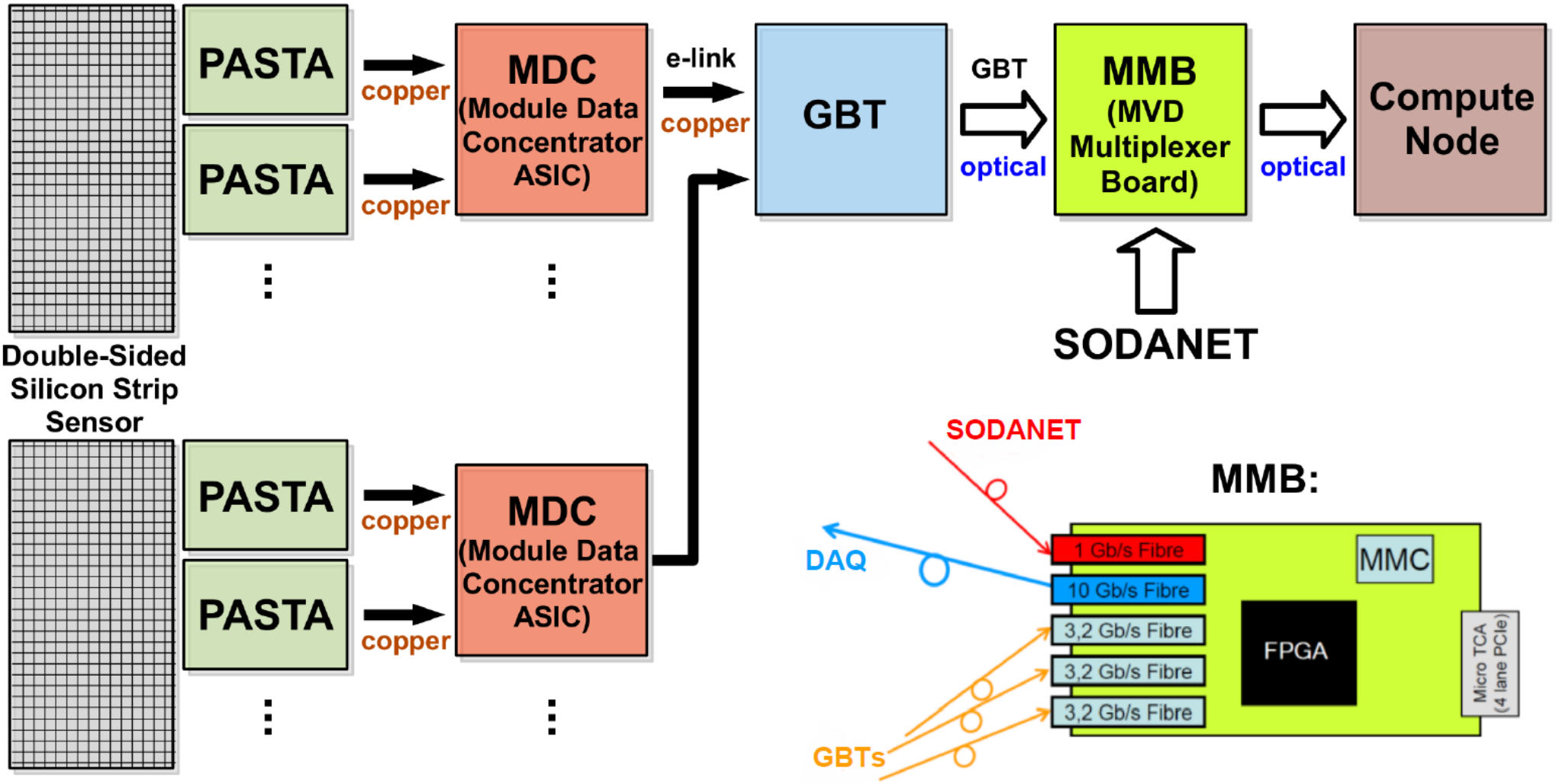
  - 200,000 strip channels
    → 3112 front-ends (64 chn.)
    self-triggering readout!



Strip DAQ Chain



Strip DAQ Chain

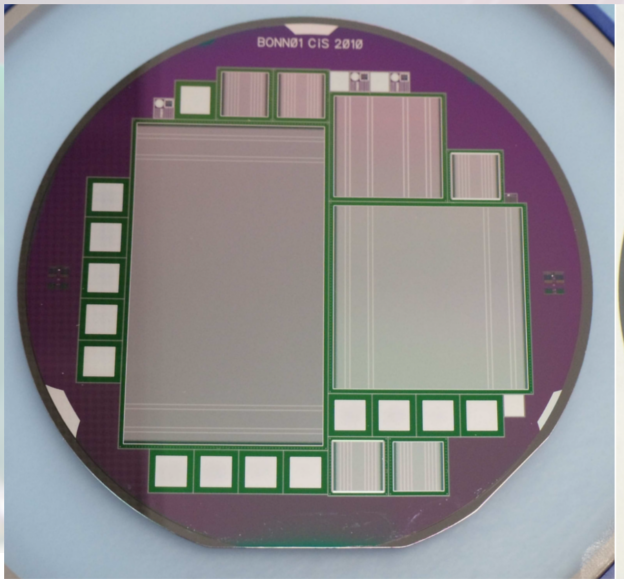


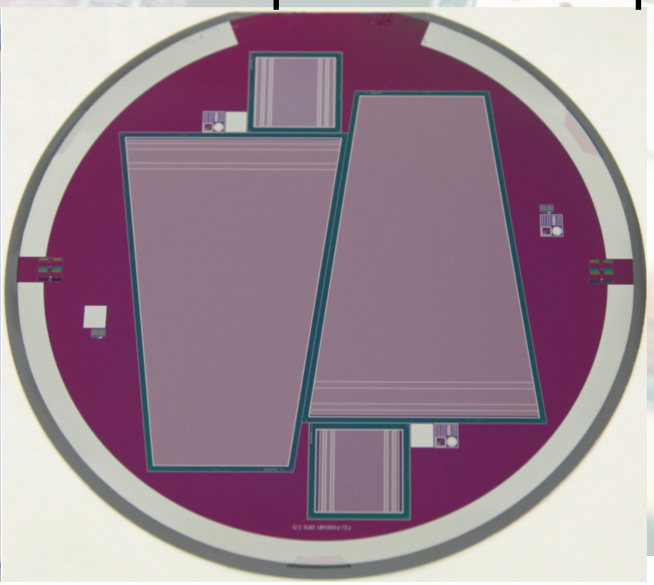
Strip Detectors

- Barrel sensors
  - rectangular 60x35 mm²
    896+512 strips
  - square 35x35 mm²
    512+512 strips
- 65 µm strip pitch
  → 130 µm readout pitch

- Disk sensors
  - trapezoidal
    58 mm high, 37 mm long side
  - 768+768 strips
- 15° stereo angle
- 45 µm strip pitch
  → 90 µm readout pitch

JLU Gießen





IKP Jülich

Strip Detectors

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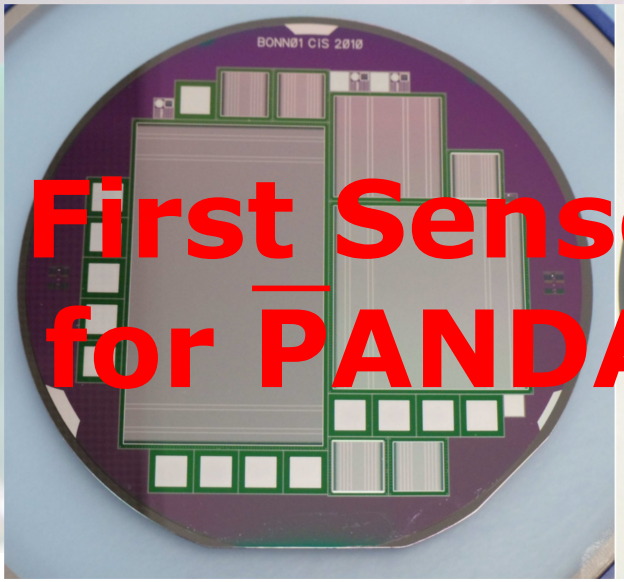
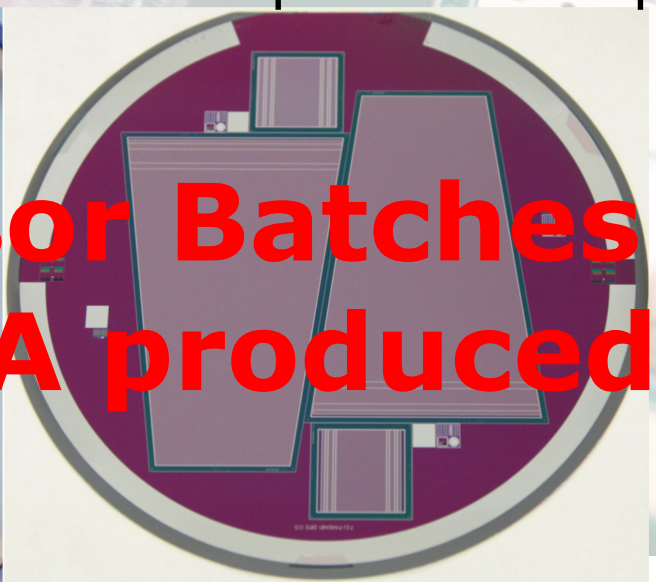


First Sensor Batches for PANDA produced



IKP Jülich

PASTA

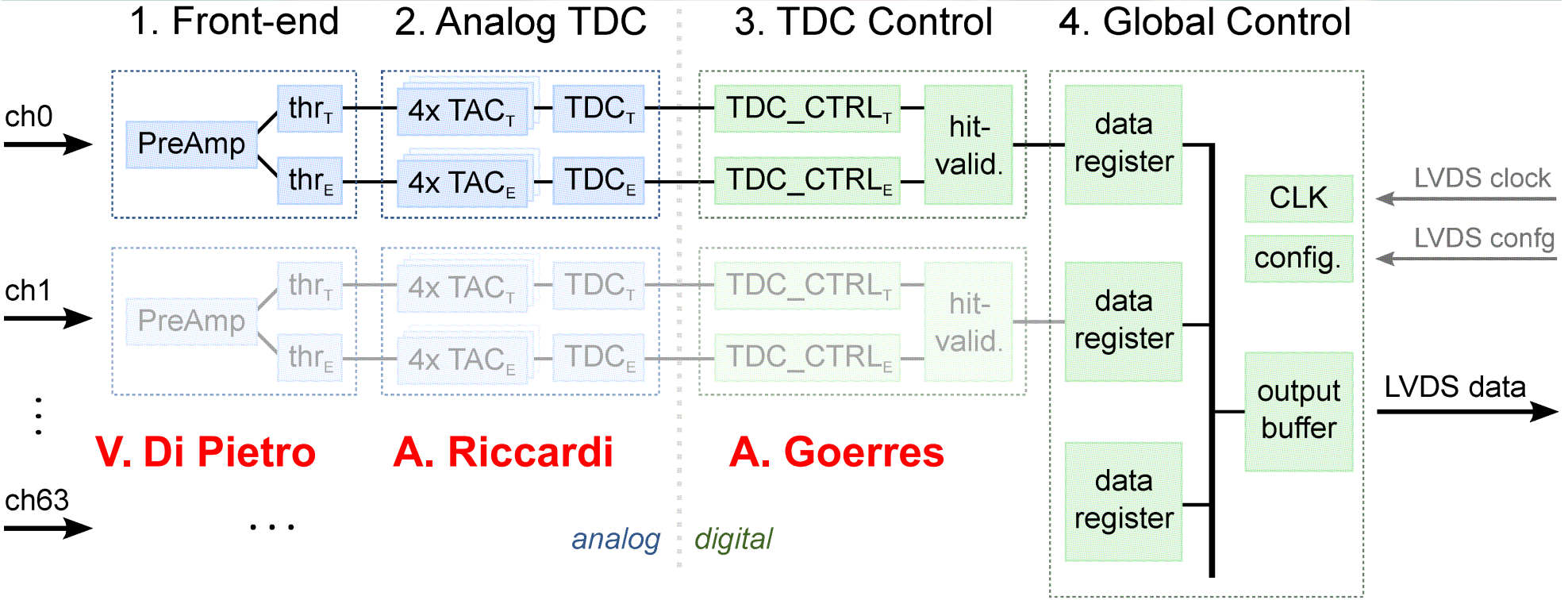
- 200,000 channels on 296 sensors need to be read out
- **PASTA – $\overline{\text{P}}$A**NDA **St**rip **A**SIC
  - Measurement concept inspired by TOFPET architecture
    - ASIC for SiPM readout from EndoTOFPET-US collaboration
    - self-triggering, fully digital back-end
  - Complete redesign of analog stage for strip detectors
  - Time-over-Threshold (ToT) using analog interpolators
    - multiple ToT stages to reduce pile-up
    - low power consumption
    - precise time resolution
  - Joint development of:
    - University Gießen
    - Forschungszentrum Jülich
    - INFN Torino

PASTA

- Requirements:
  - event rate up to 40 kHz per strip
  - detector capacitance 10-25 pF
  - input charge 1-40 pC (10 MIPs)
- Goals:
  - linear time measurement with input charge
  - 8 bit dynamic range
  - 50-200 ps time bin width
  - noise < 1500 e^-
  - power consumption < 4 mW/chn

PASTA

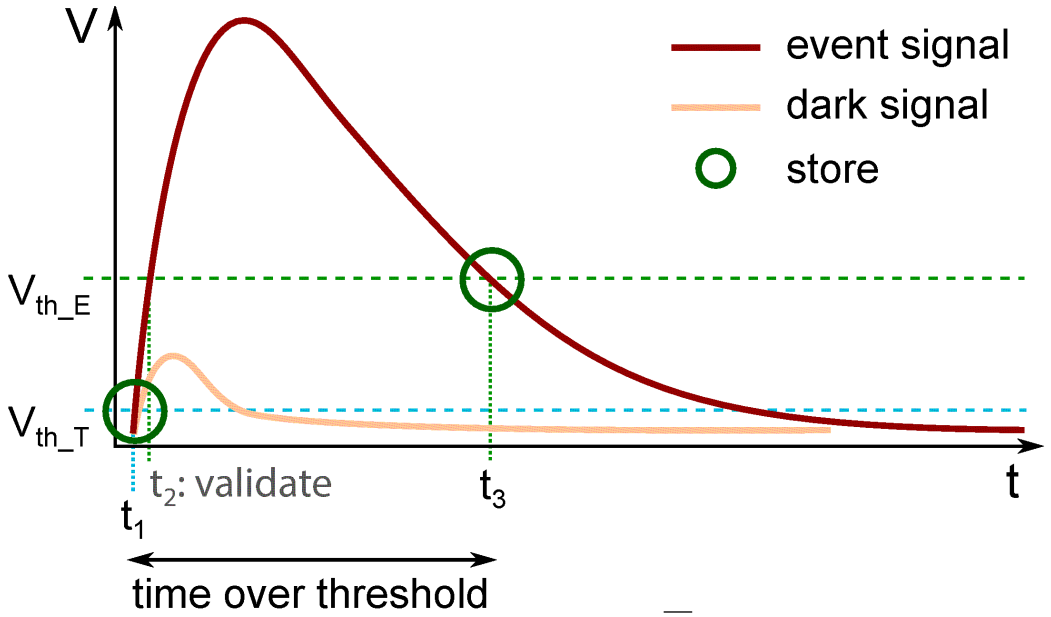
- Architecture of the chip
  - 2 discriminators for each of the 64 channels
  - 4 time-to-analog converters (TAC) per discriminator

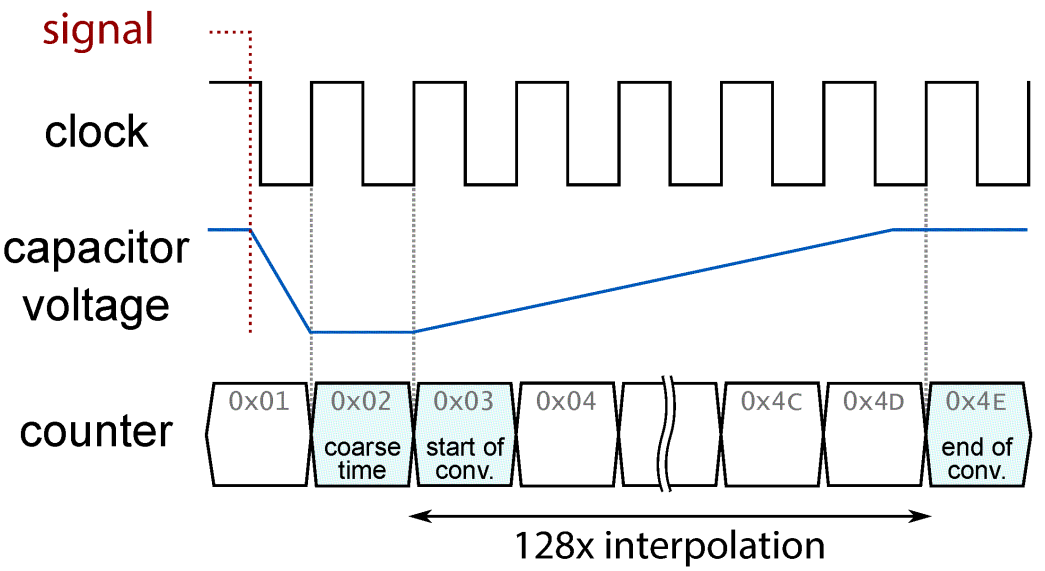


technical advisors: A. Rivetti, M. Rolo

PASTA Features

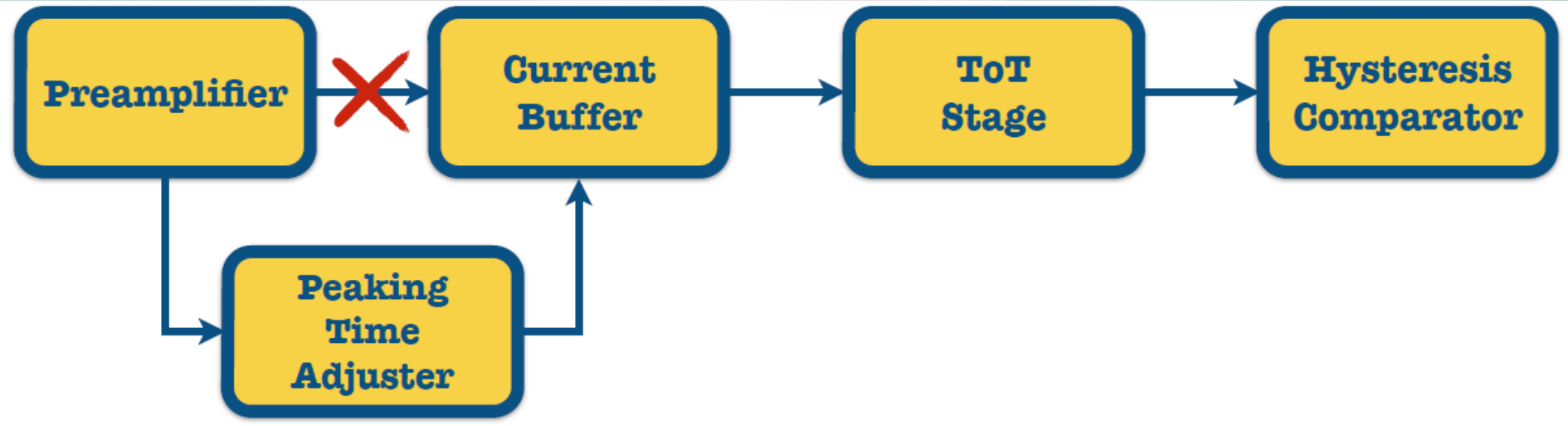
- Dual threshold concept
  - time information t_1 from lower threshold V_{th_T} → reduce time-walk
  - hit validation from higher threshold V_{th_E}
  - ToT: t_1 to t_3
- Time measurement
  - coarse time from chip clock
  - fine time from interpolation (interpolation factor 128x @160 MHz → 50 ps bin size)





PASTA Front-end

- Analog front-end
  - Design carried out by Valentino Di Pietro



- Peaking Time Adjuster introduced
  - increases linearity
  - peaking time ~ 30 ns

PASTA Front-end

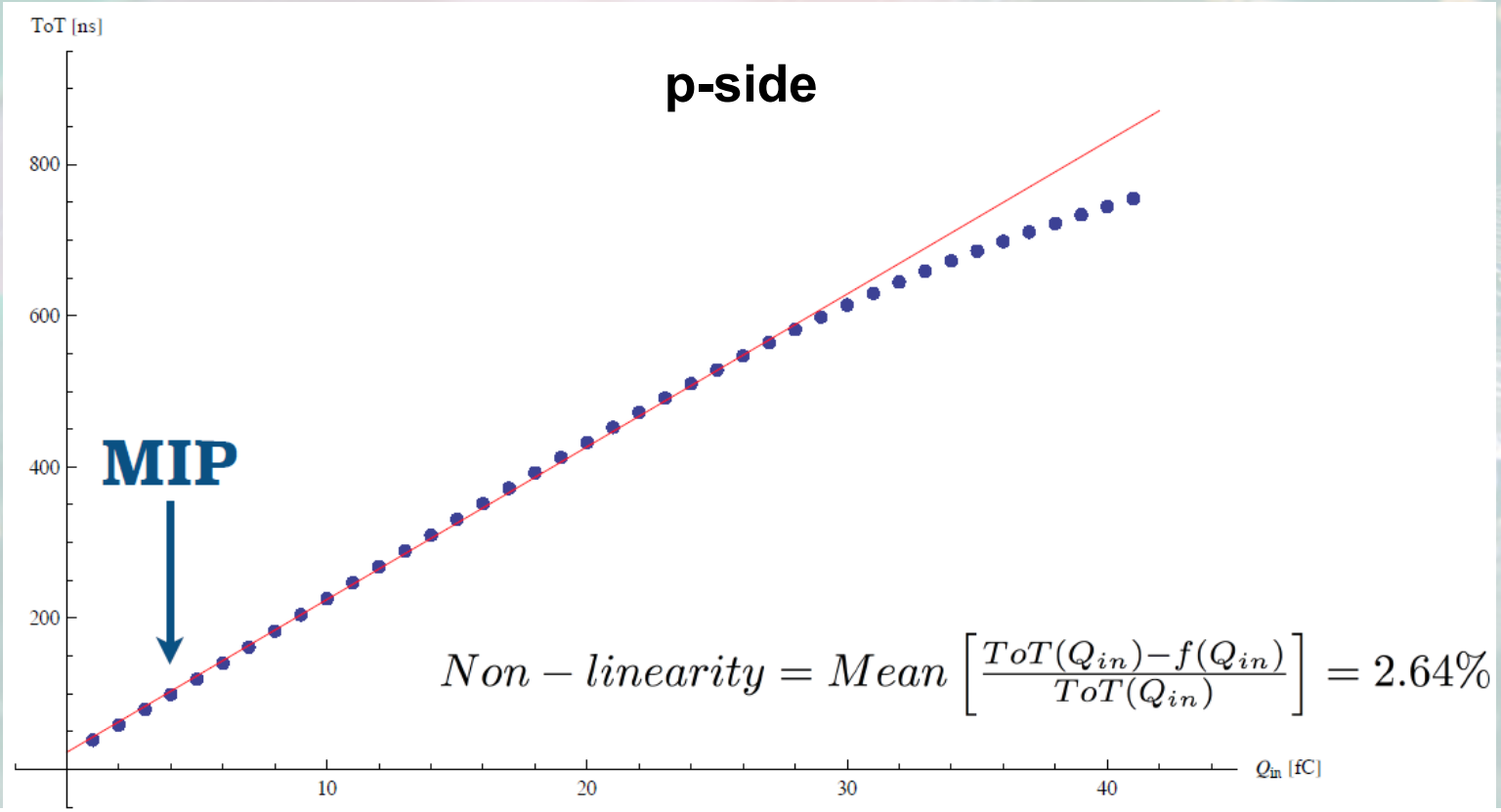
- Analog front-end
  - Design comprises
    - preamplifier
    - calibration circuit
    - peaking time adjuster
    - current buffer
    - ToT amplifier
    - baseline restorer
    - hysteresis comperators
    - delay line
    - local DACs

PASTA Front-end

- Analog front-end
  - Calibration pulse to front-end
    - amplitude controlled via 6 bit DAC
    - initiated by a test pulse
    - source of test pulse:
      - external signal from I/O pad
      - internal pulse generated by GCTRL
  - Test pulse to TDC controller
    - initiates TDC ramping without front-end
    - test readout independent of front-end input

PASTA Front-end

- Linearity from simulations
  - good linearity at low input charges
  - deviations compensated by calibration



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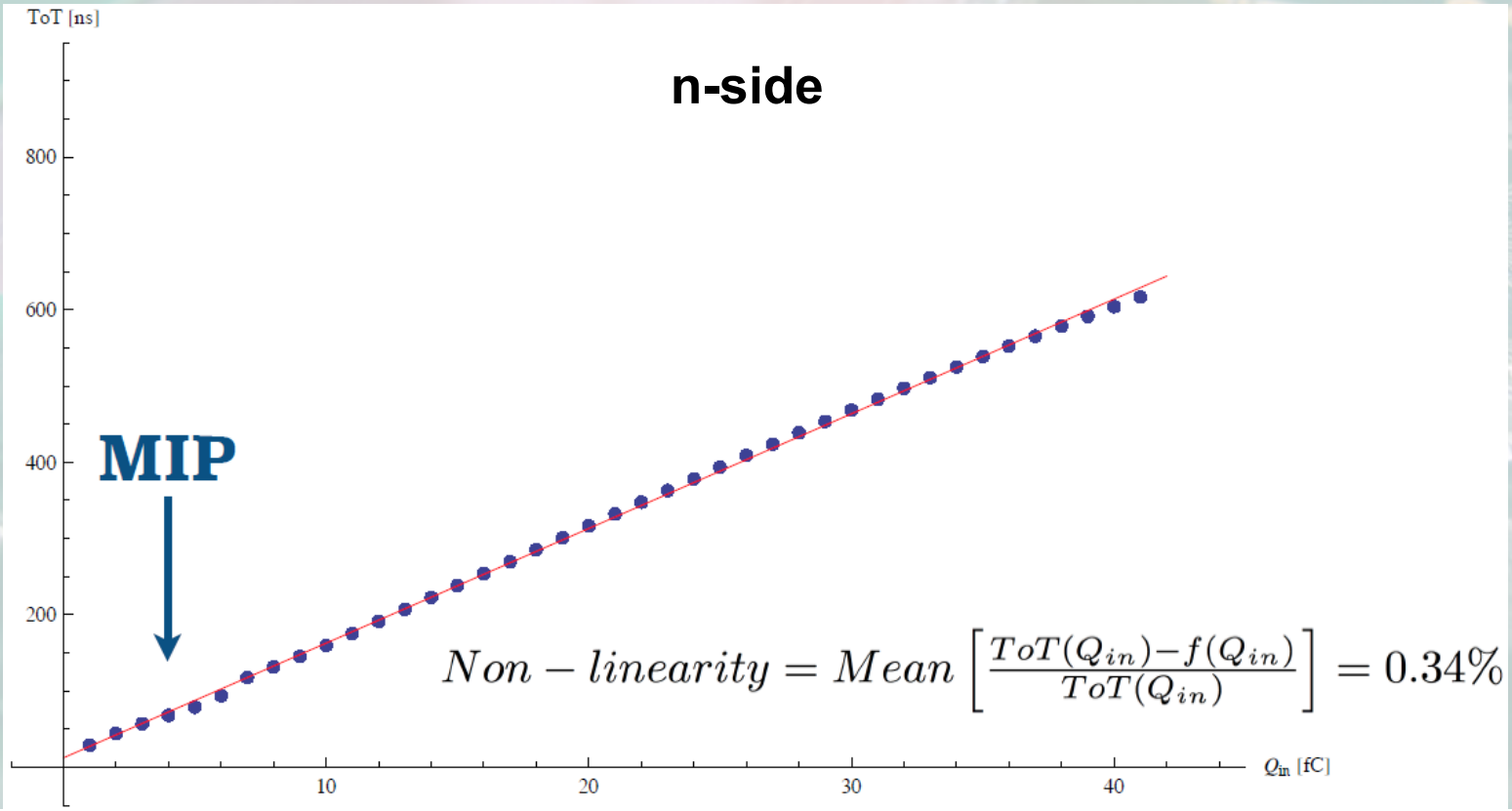
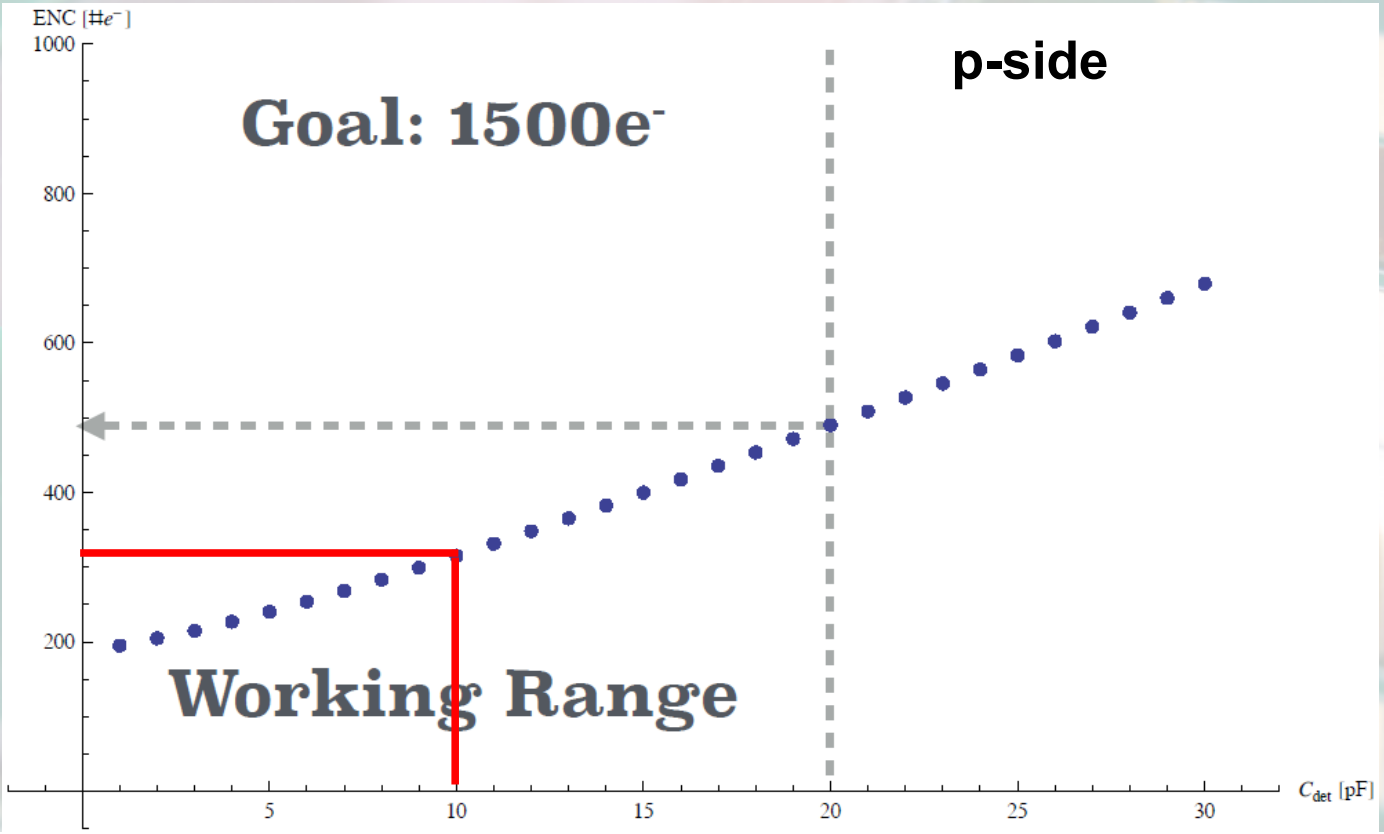


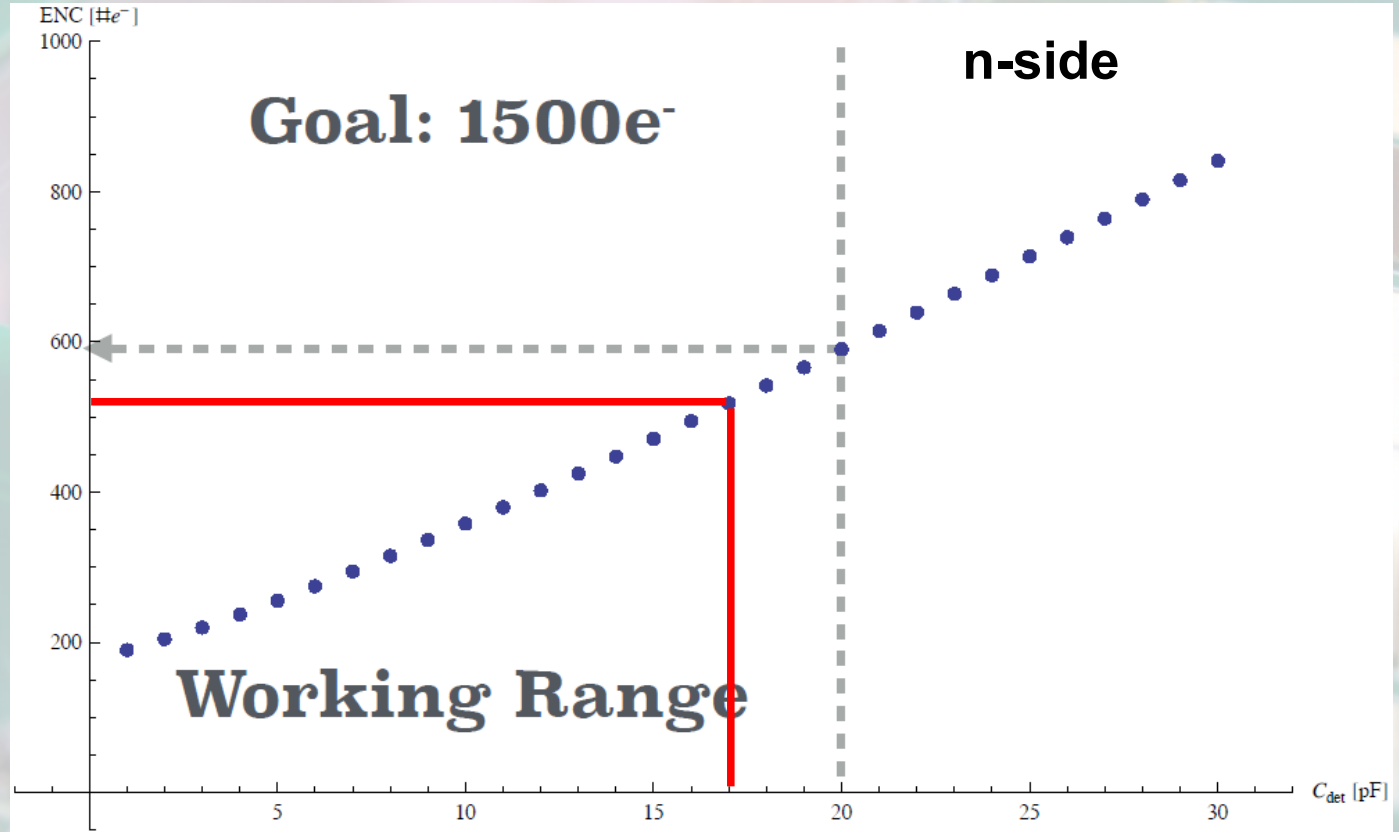
PASTA Front-end

- Noise (ENC) from simulations
  - p-side: 500 e^- @ 20 pF
  - case of application: 350 e- @ 10 pF



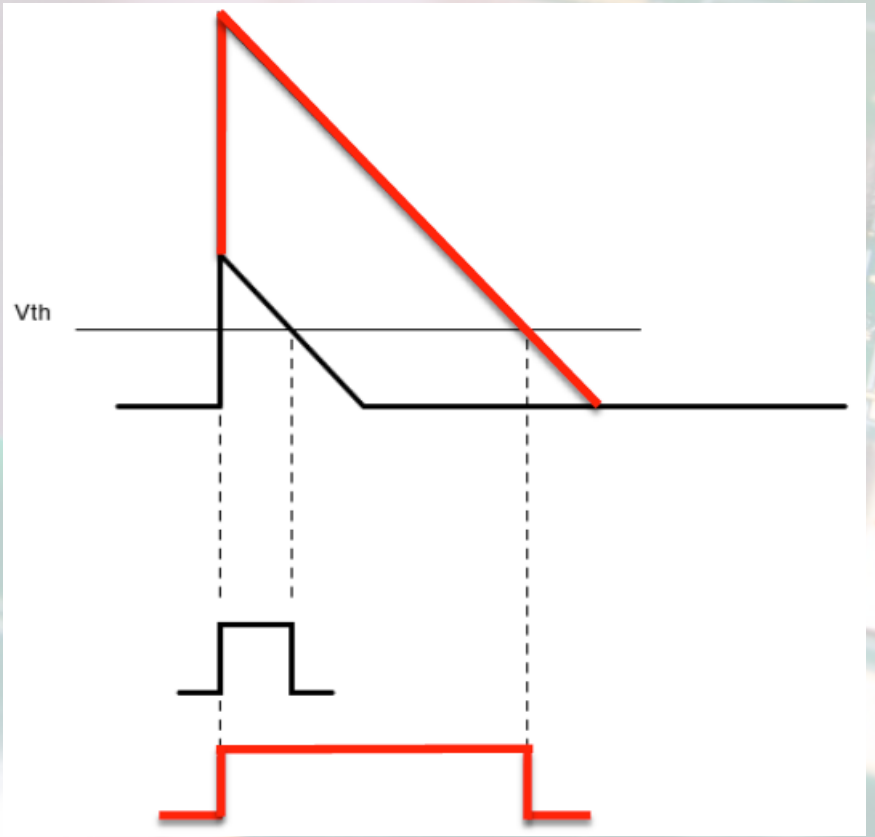
PASTA Front-end

- Noise (ENC) from simulations
  - n-side: 600 e⁻ @ 20 pF
  - case of application: 550 e- @ 17 pF



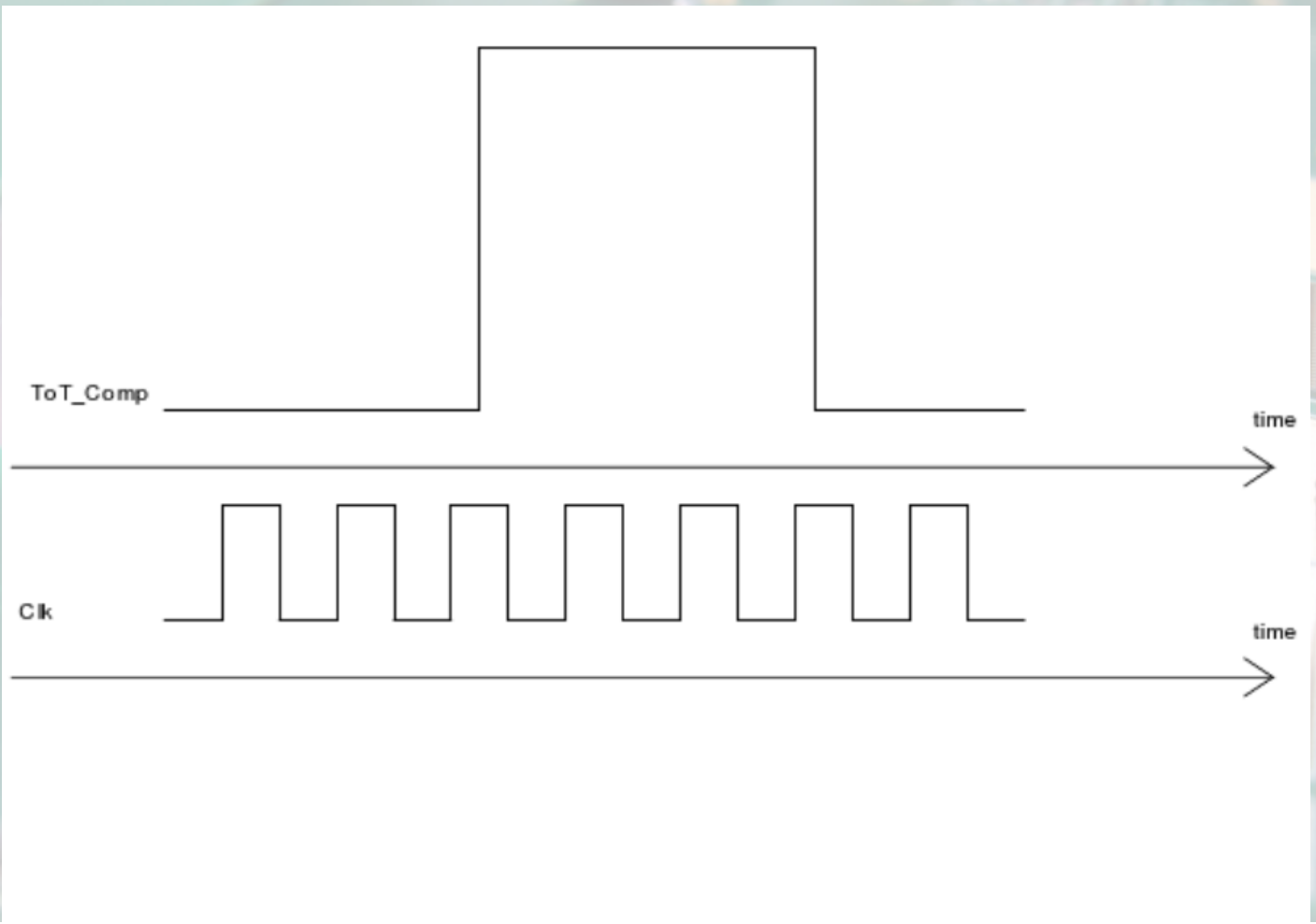
PASTA TDC

- Time-to-Digital-Converter
  - Design carried out by Alberto Riccardi



PASTA TDC

- Timing



PASTA TDC

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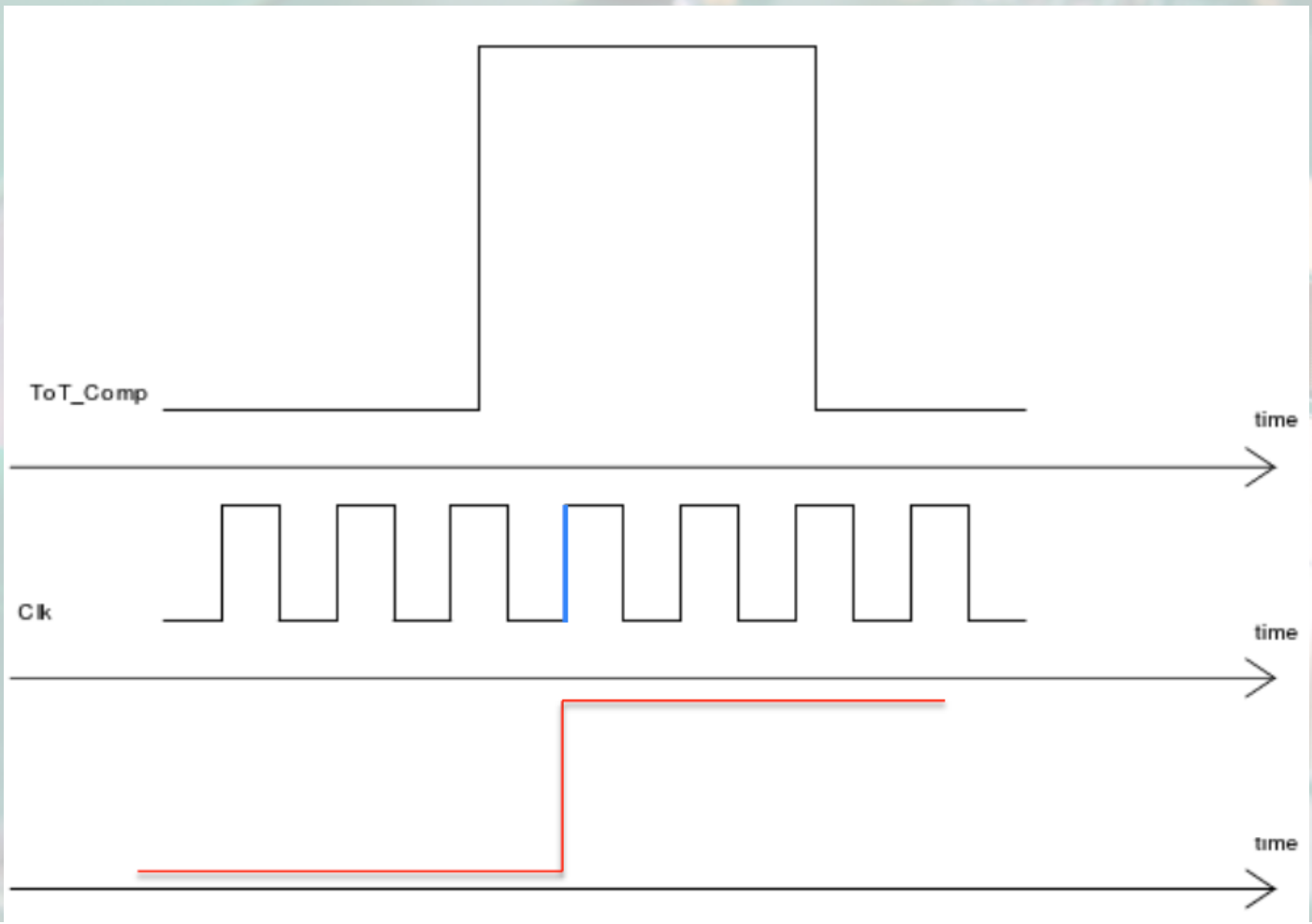

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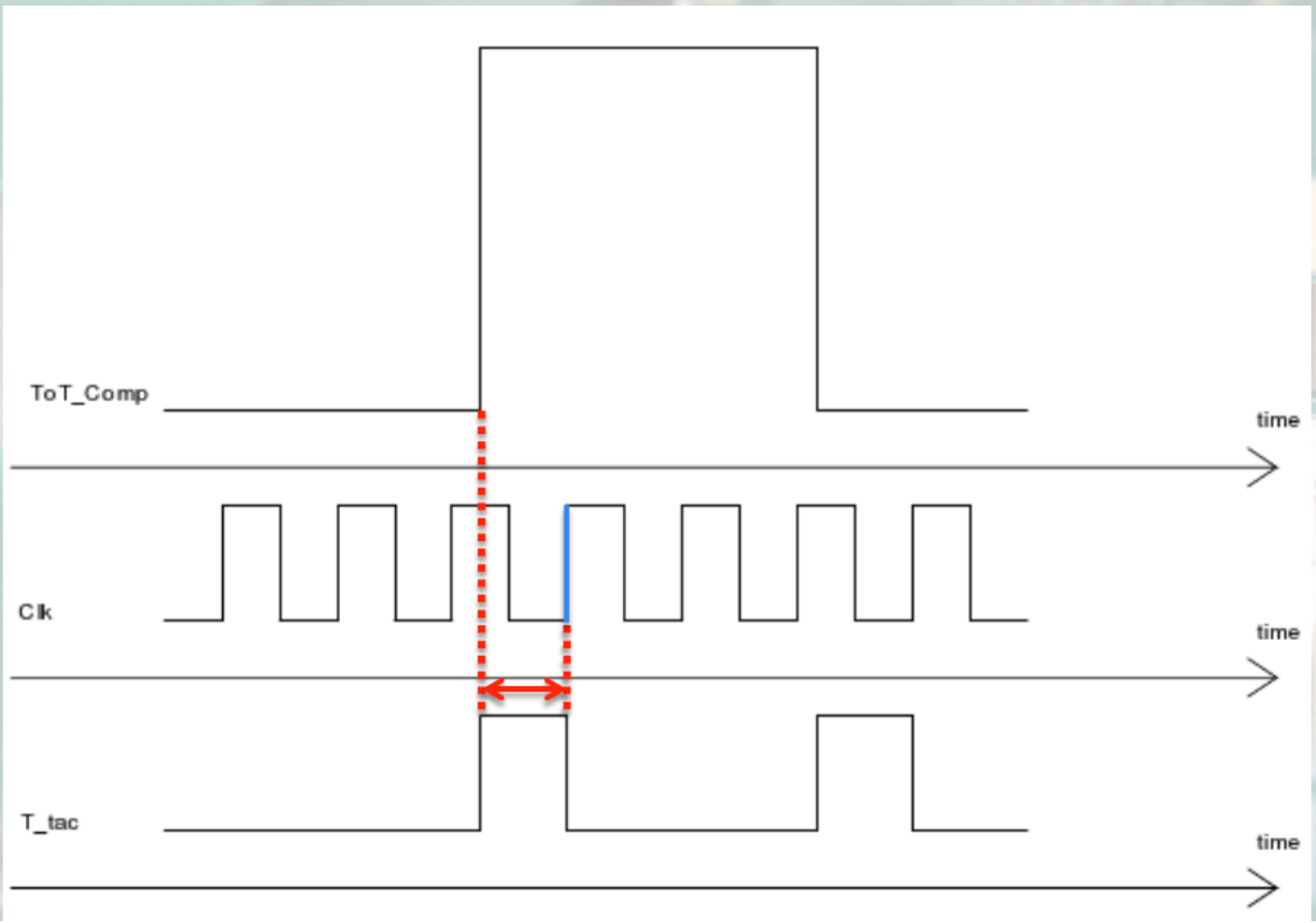
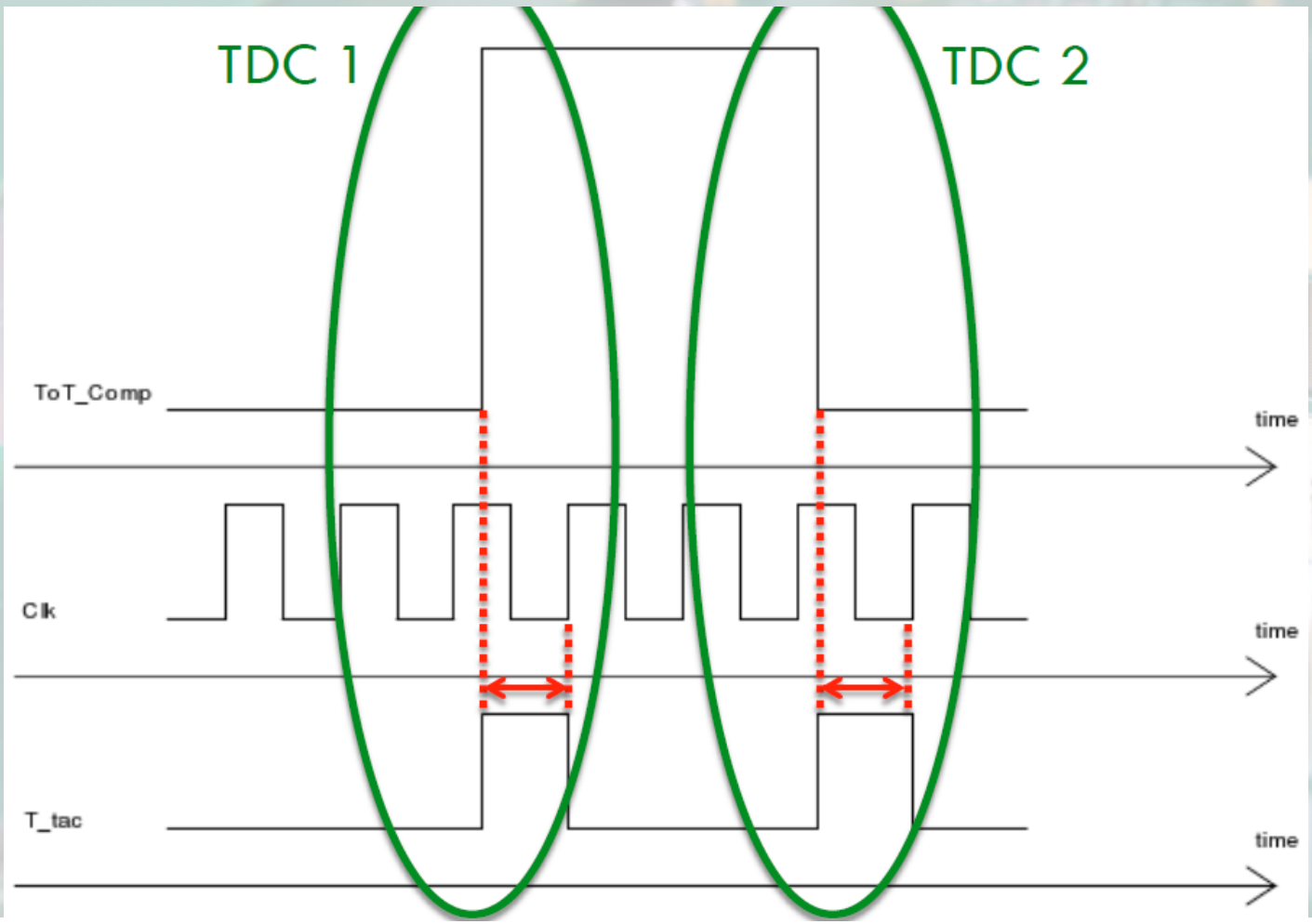


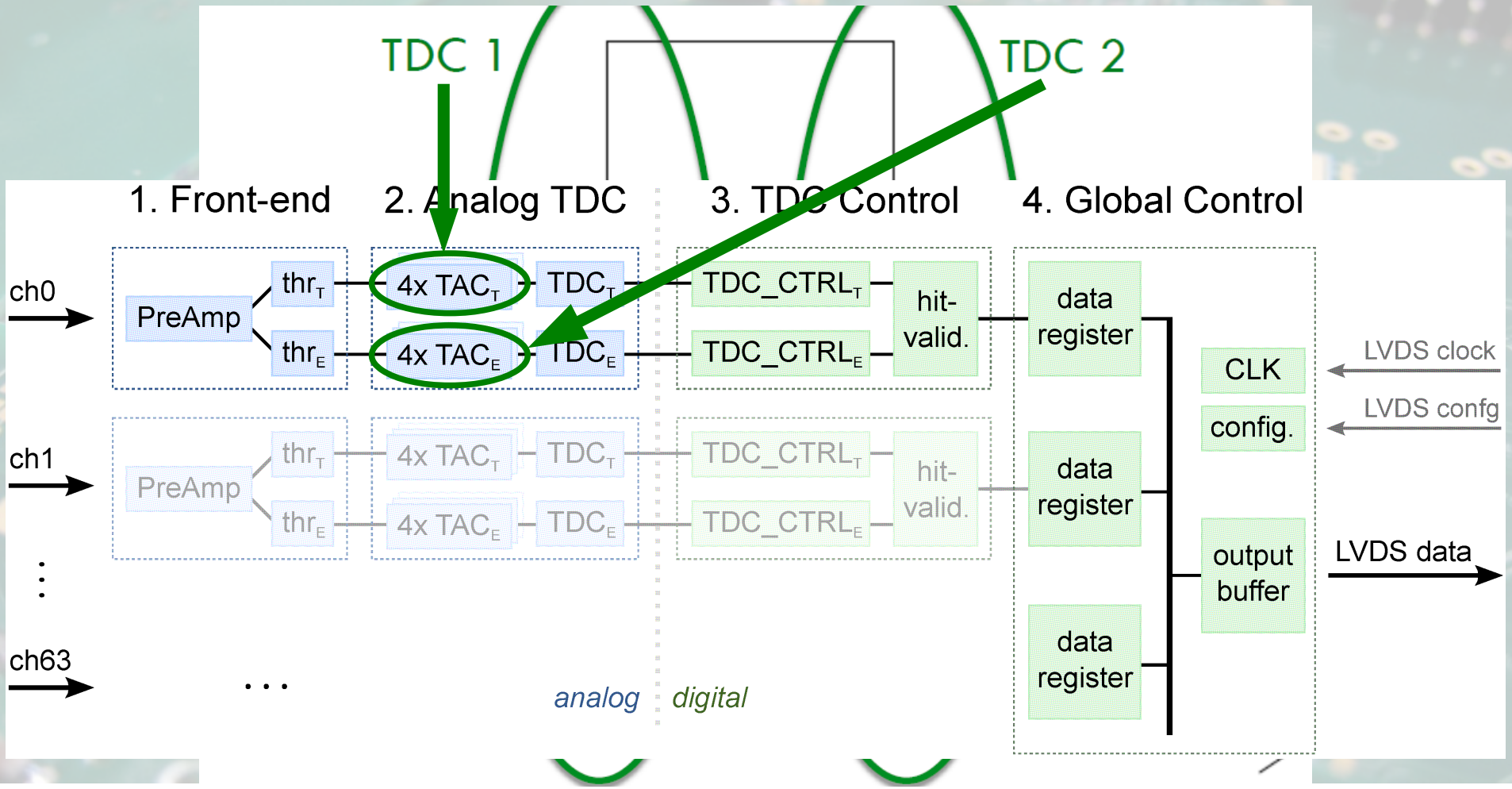
PASTA TDC

- Timing



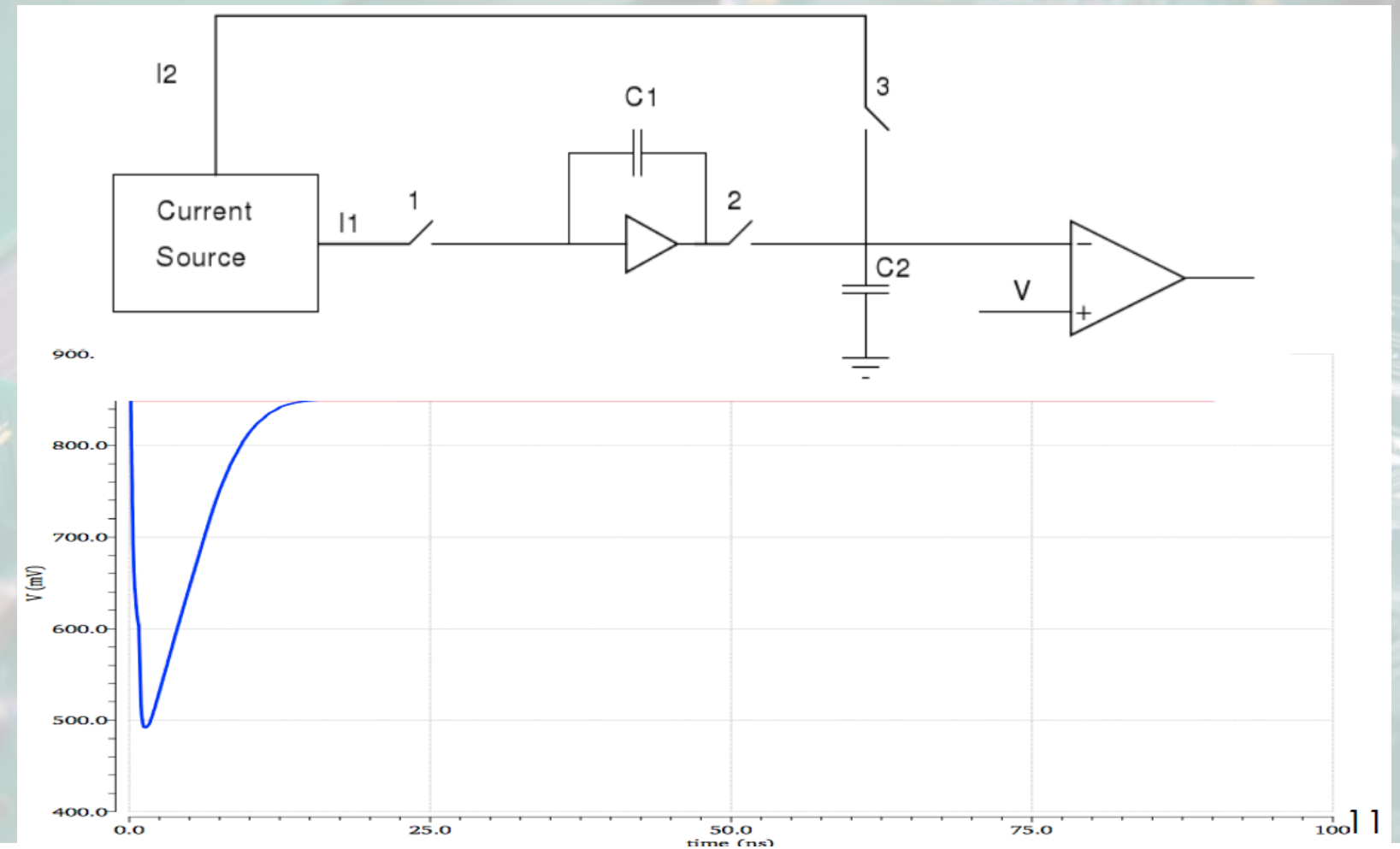
PASTA TDC

- Timing



PASTA TDC

- TDC Implementation



PASTA TDC

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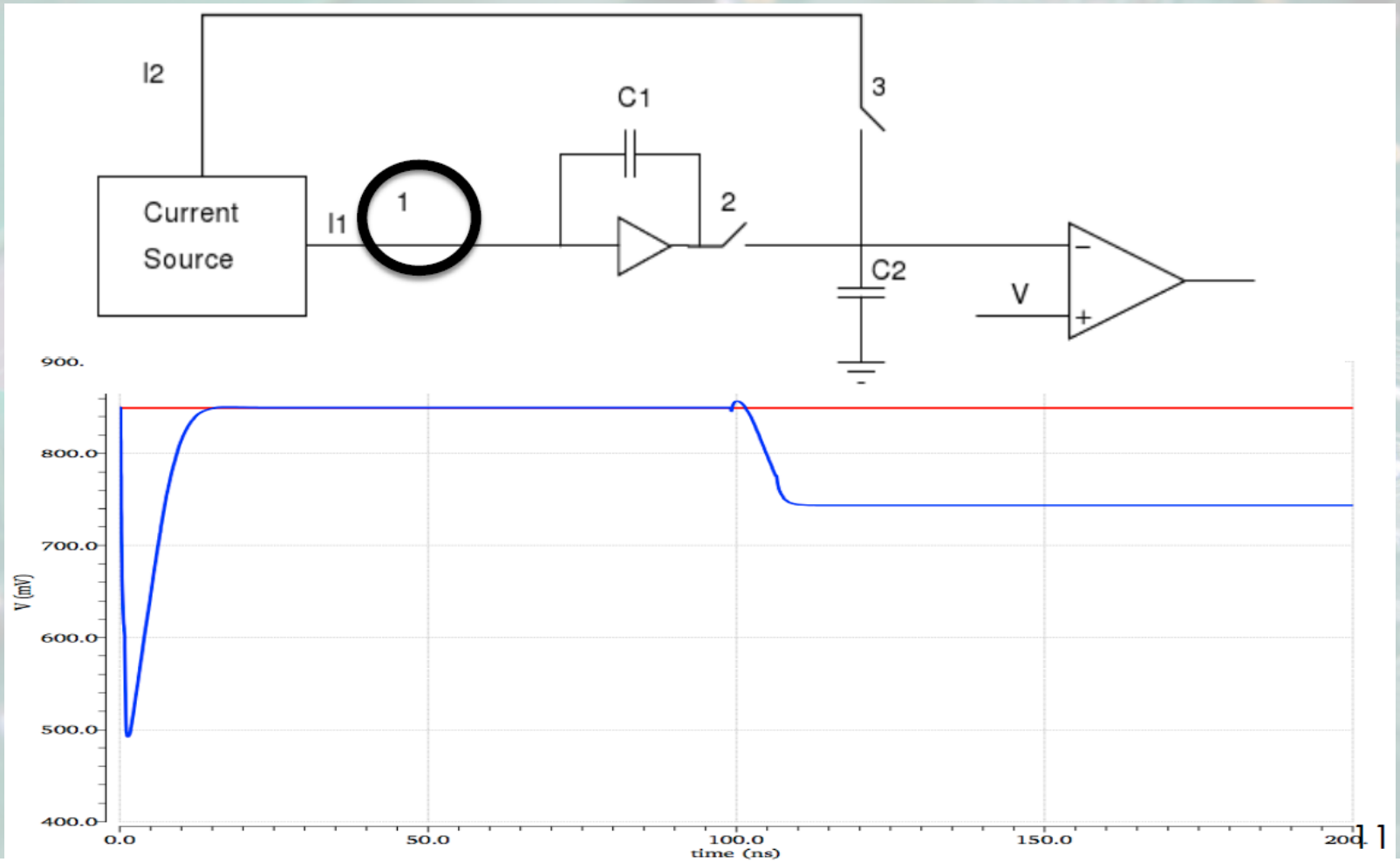

PASTA TDC

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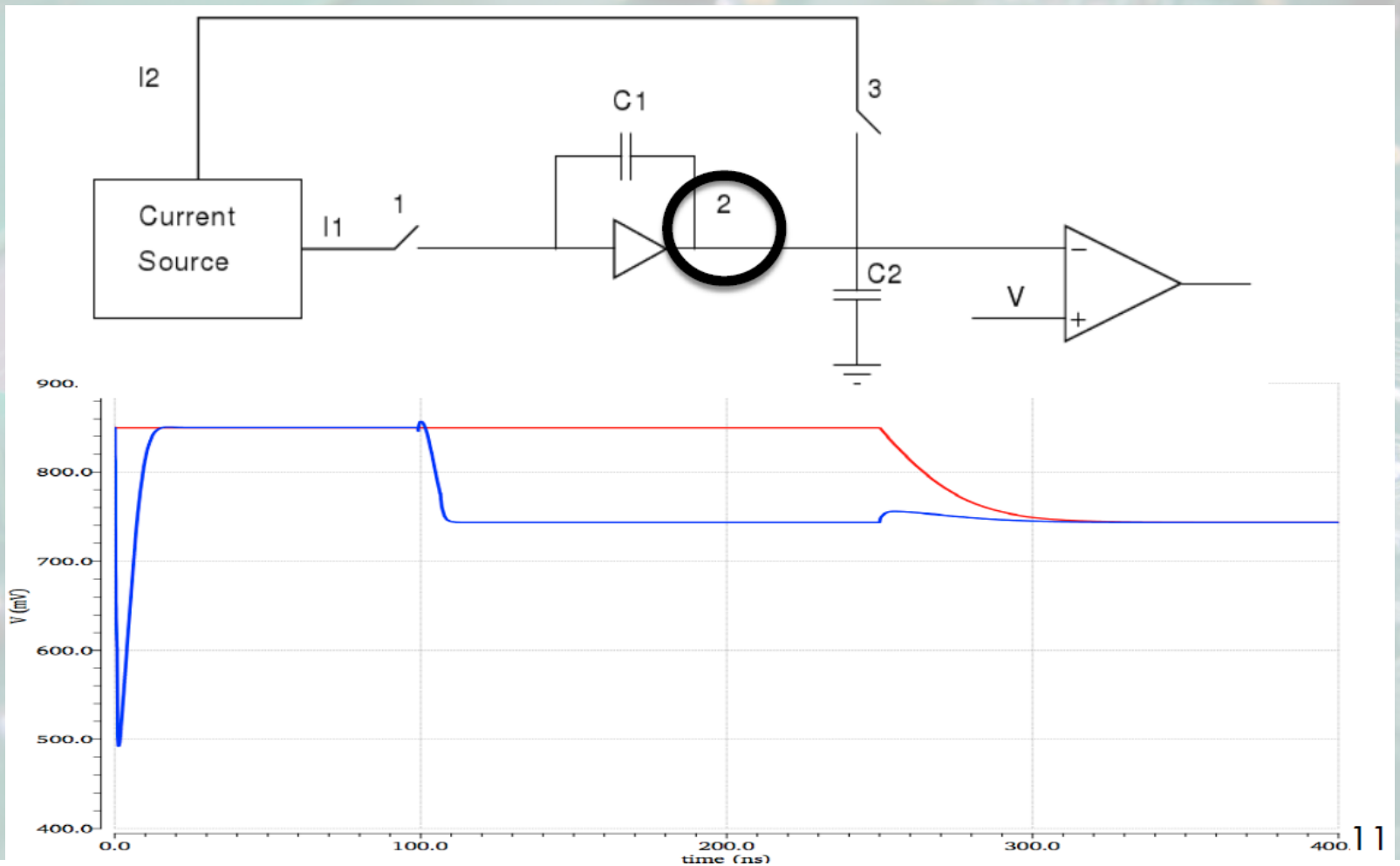

PASTA TDC

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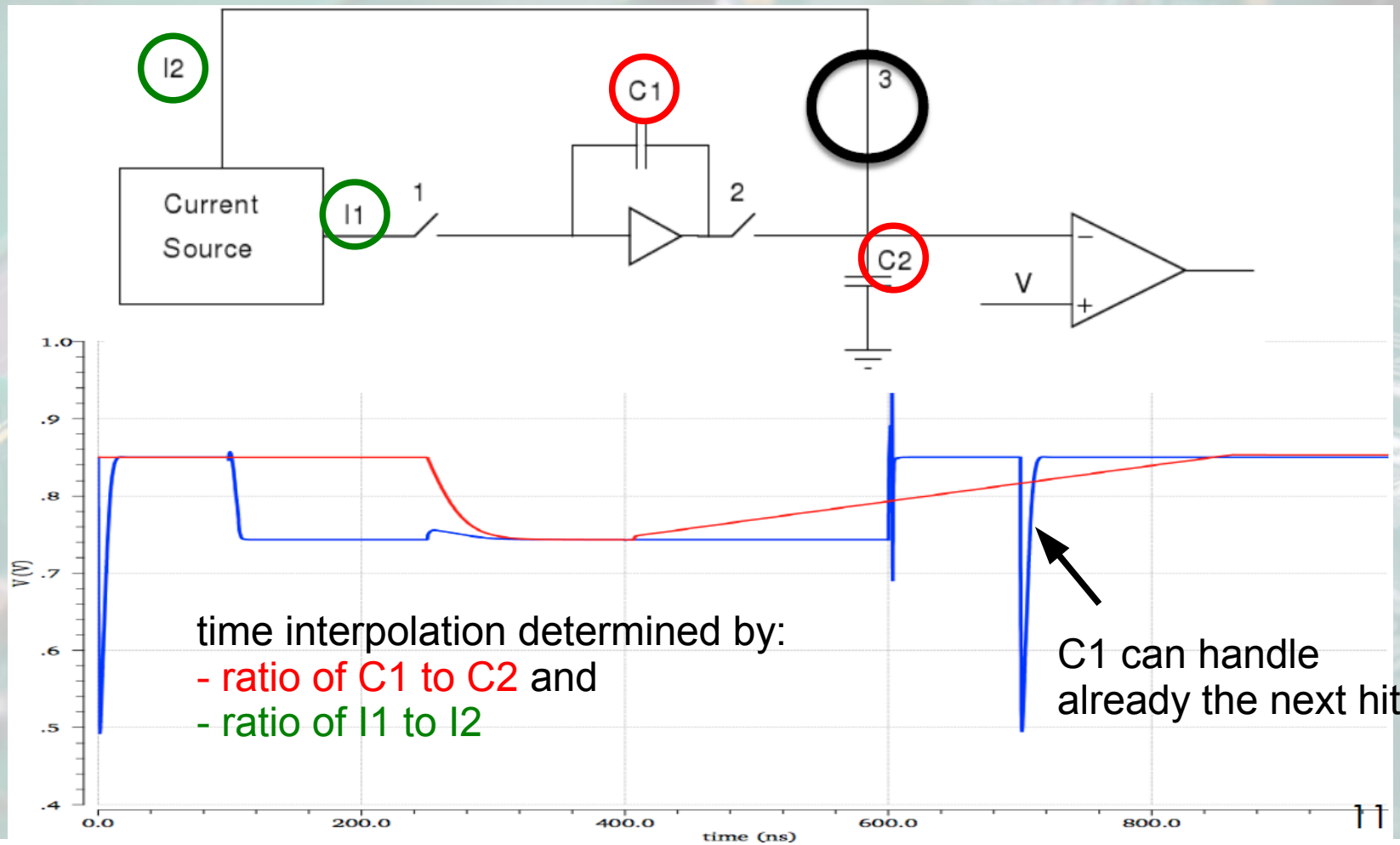
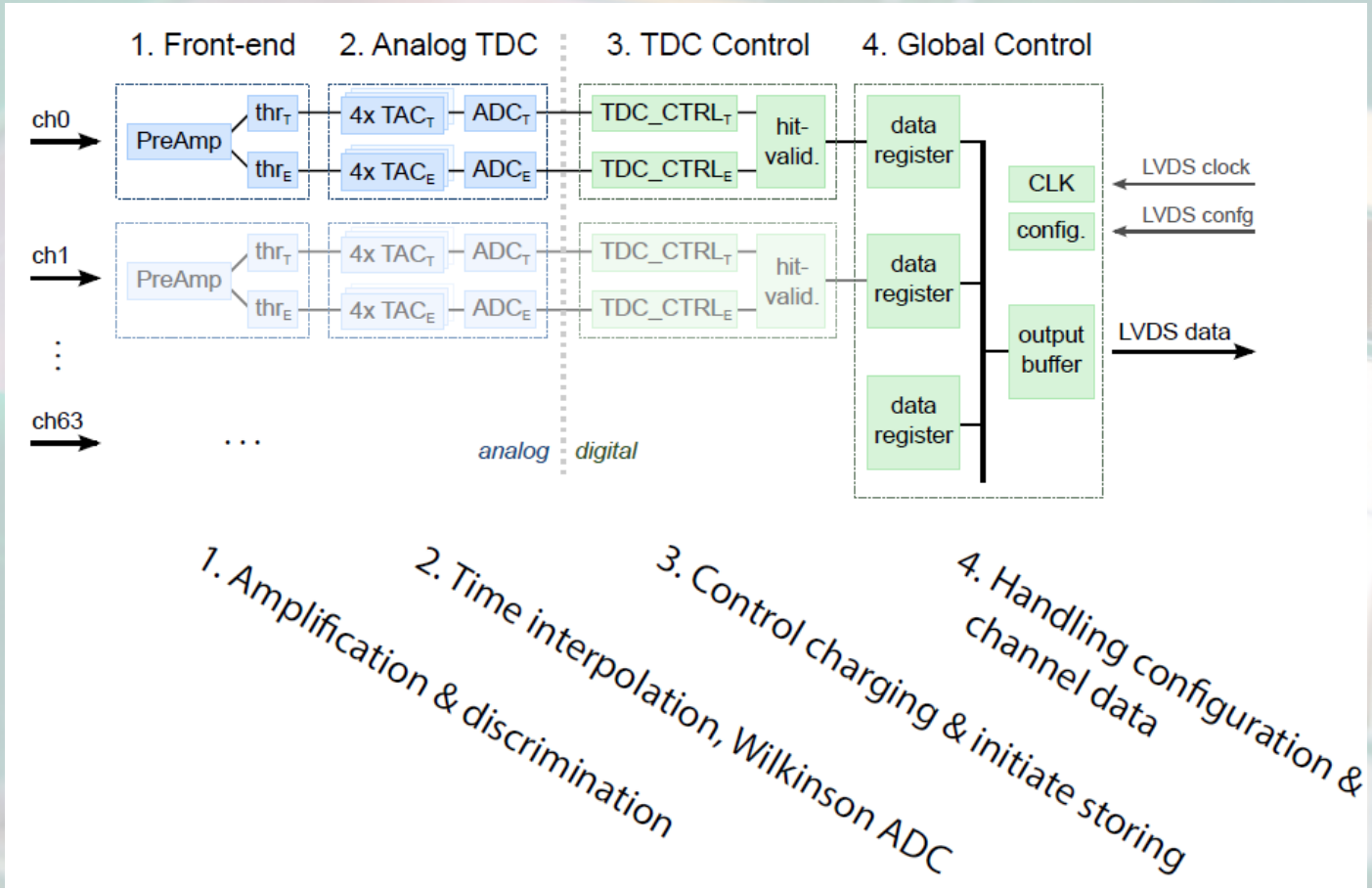


PASTA Digital Control

- TDC Control and Global Control
  - Design carried out by André Goerres



PASTA Digital Control

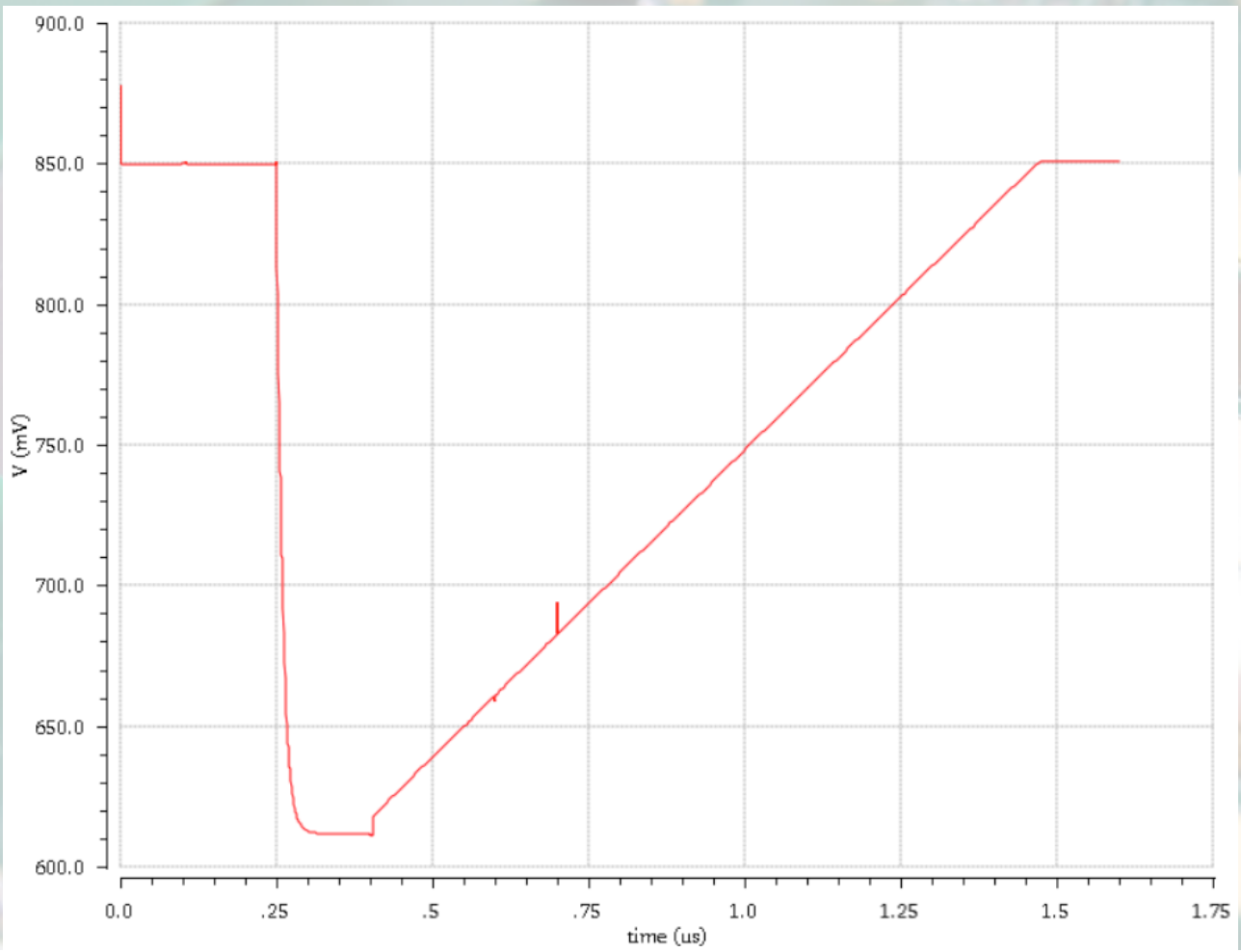
- TDC Control and Global Control
  - Design carried out by André Goerres
  - Rewritten TDC Control code with major simplification
    - area reduction: 0.11 µm² to 0.01 µm²
    - power reduction: 1.57 mW/chn to 0.25 mW/chn
  - Integration of SEU mitigation techniques
    - protect all state machines and device registers
    - Hamming encoding
    - triple-modular redundancy

PASTA Digital Control

- TDC Control and Global Control
  - New features/components included
    - (optinal) skip validation
    - (de-)select use of delay line
    - synchronization chain to prevent event losses
    - asynchronous FIFO for TX data
    - refresh control per TAC
    - internal clock divider

PASTA Bugfixing (1)

- Example on TDC Post-Layout Simulations



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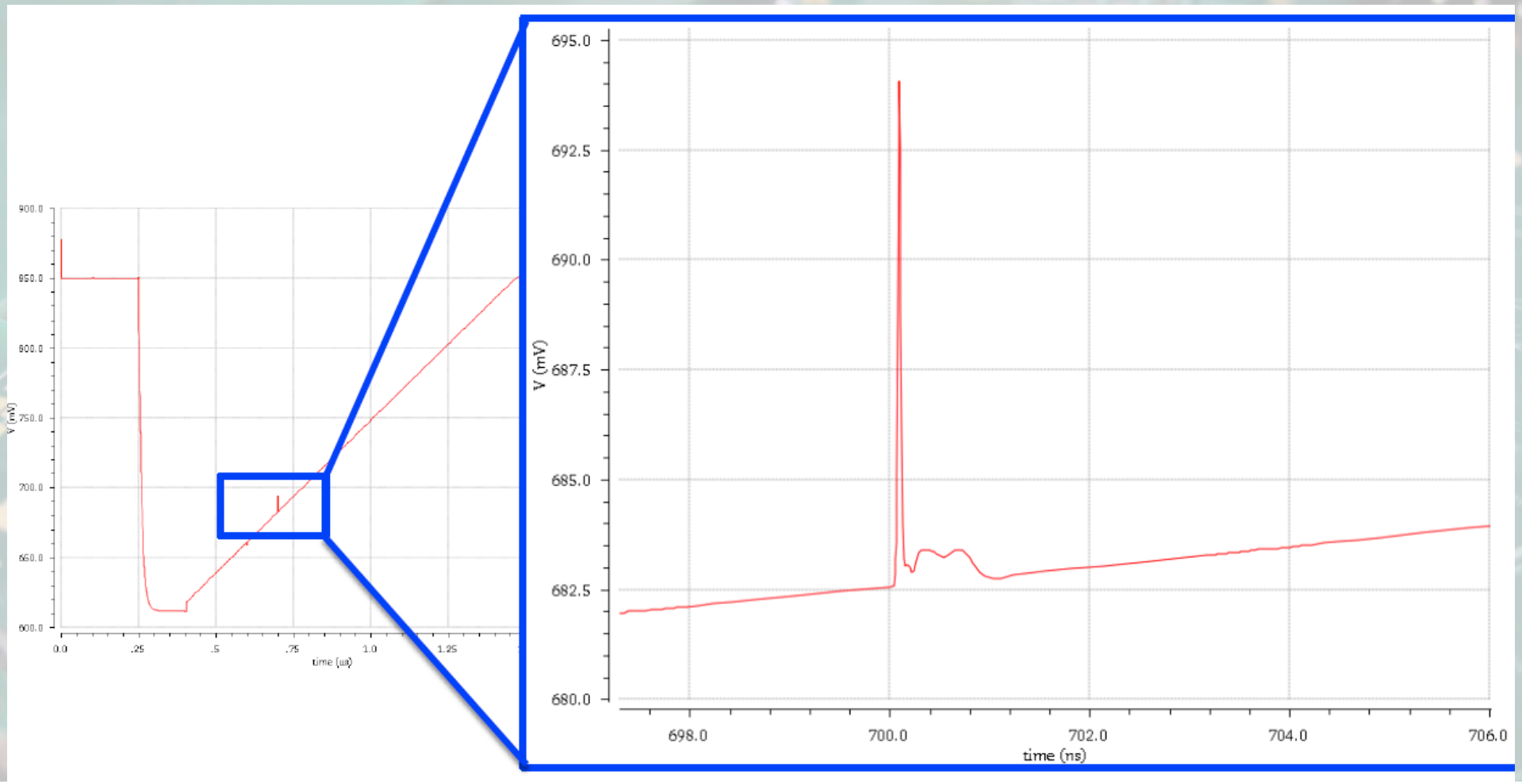

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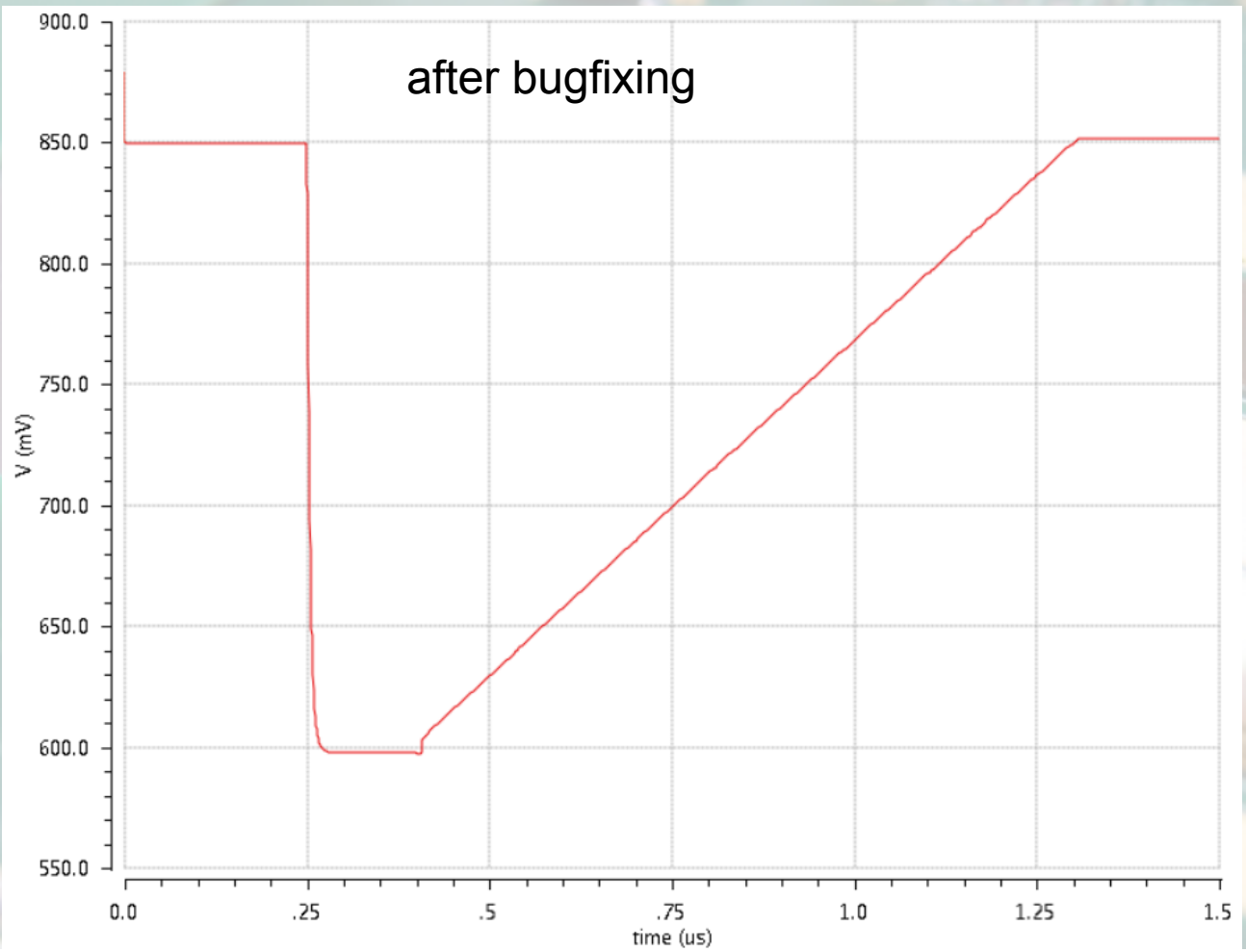
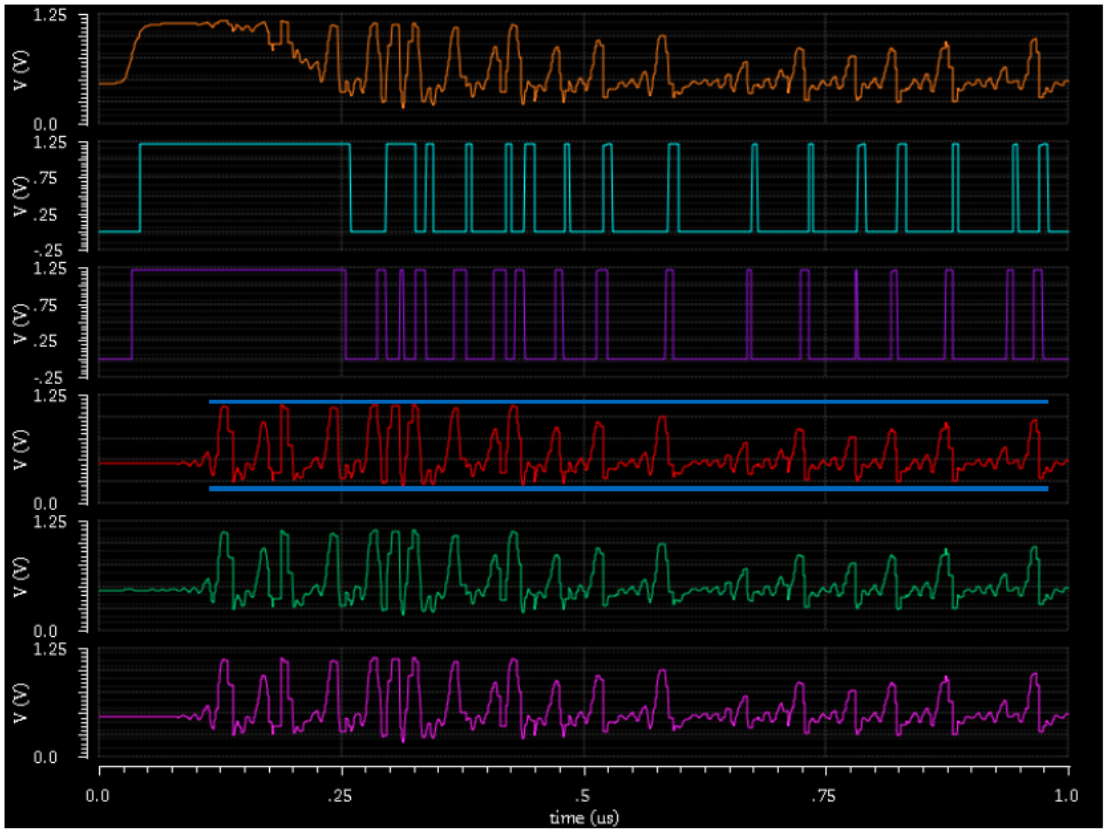


PASTA Bugfixing (2)

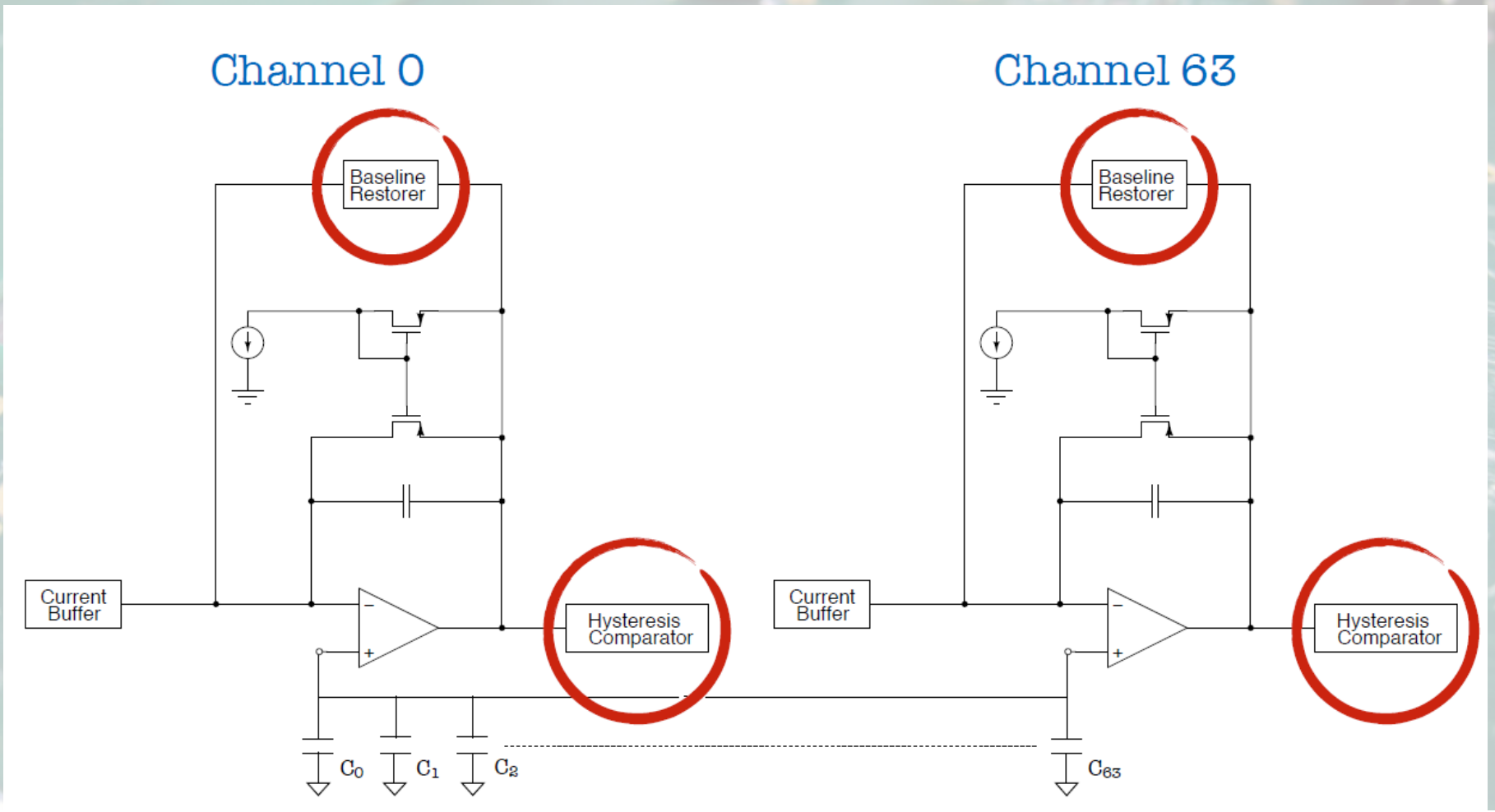
- Example on Front-end Post-Integration Simulations

16 Channels + Bias



PASTA Bugfixing (2)

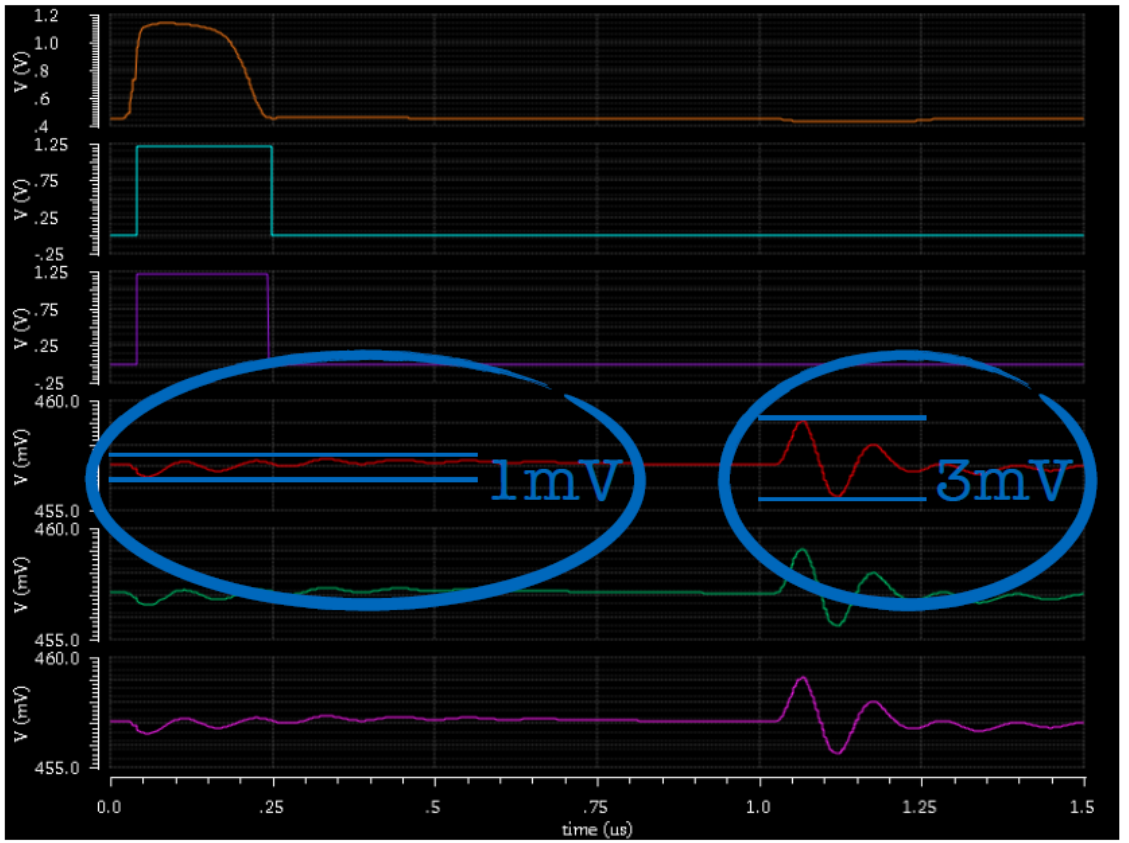
- Example on Front-end Post-Integration Simulations



PASTA Bugfixing (2)

- Example on Front-end Post-Integration Simulations

64 Channels + Bias



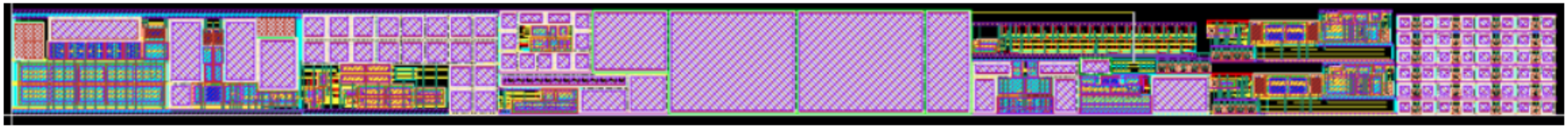
1.2V

1.2V

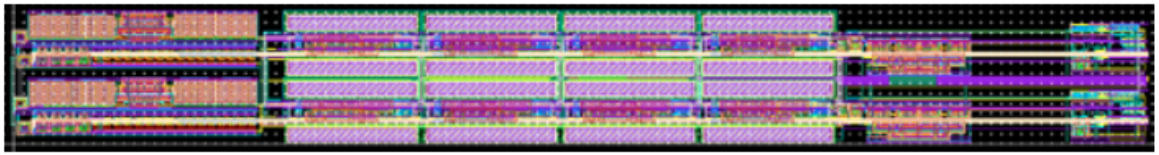
Residual bias pickup

Cross-talk

PASTA Chip

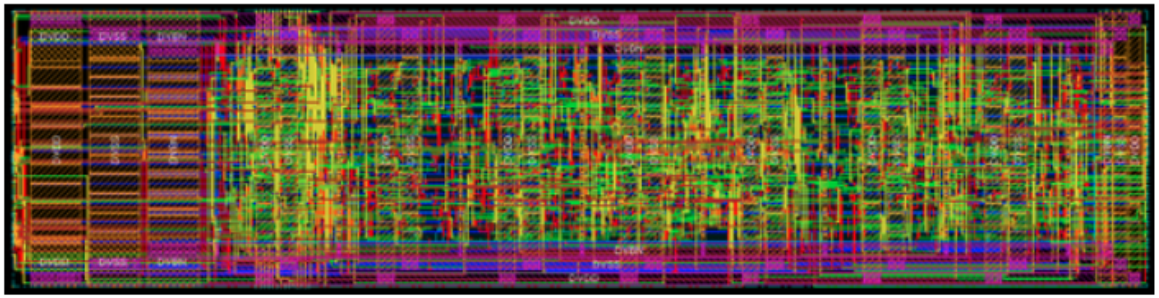


analog front-end



analog TDC

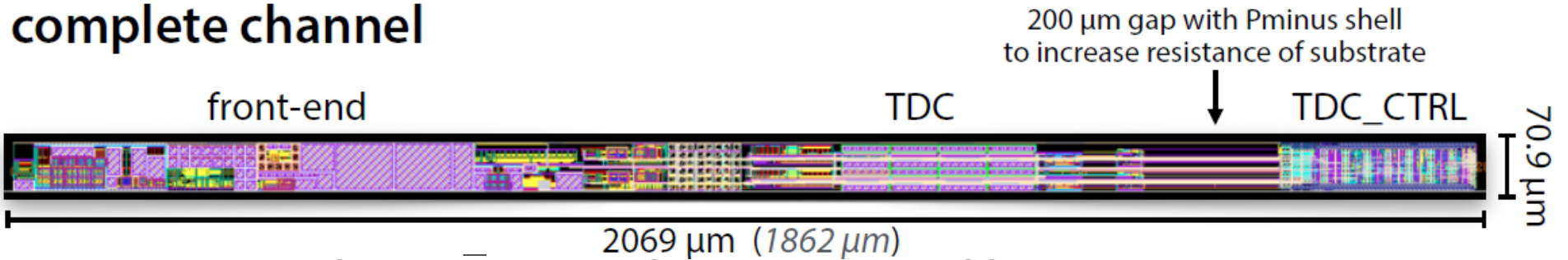
Layout screen-shots



digital
TDC controller

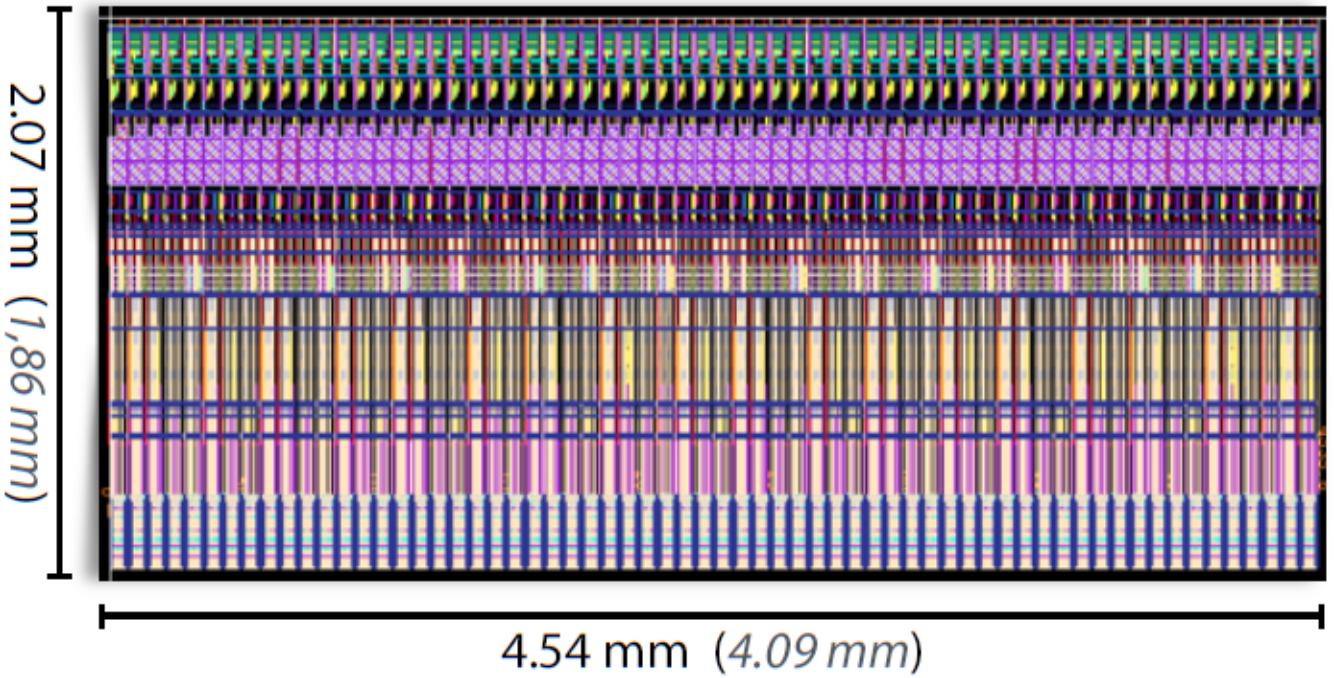
---

complete channel



PASTA Chip

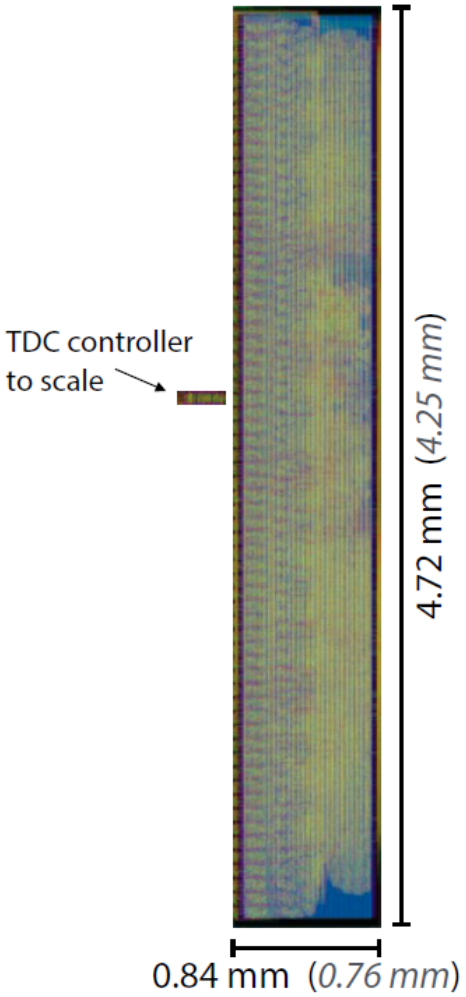
Layout screen-shots



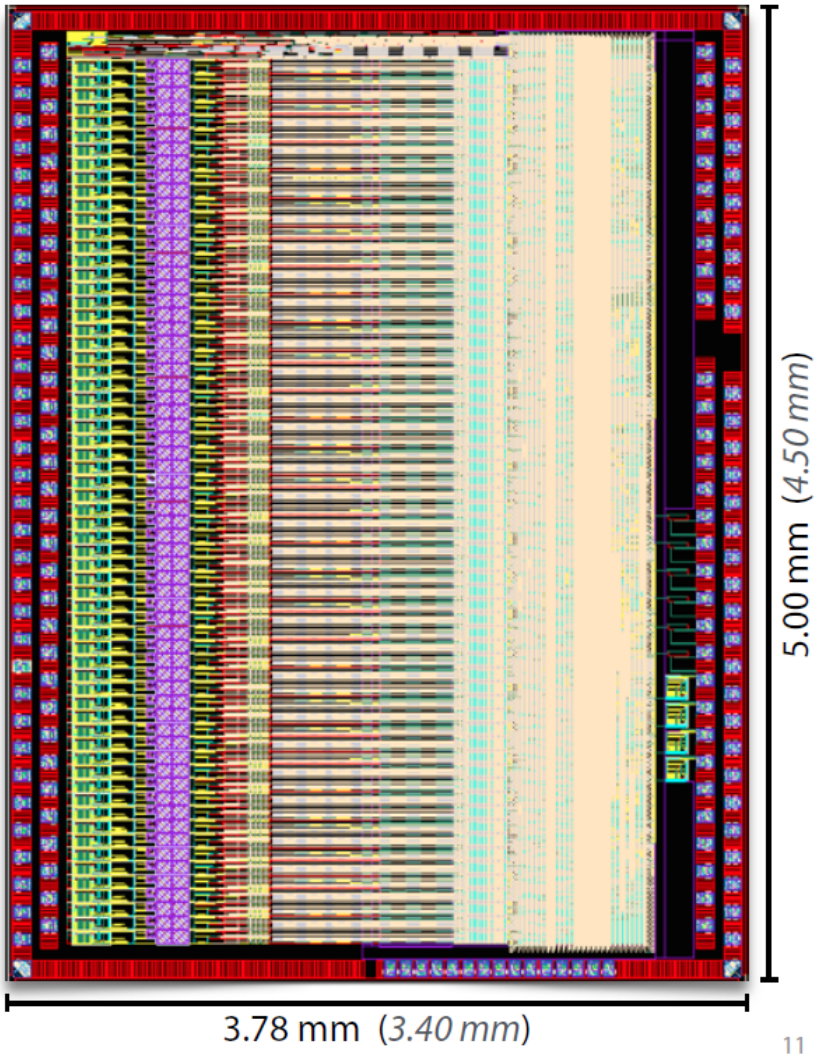
64 channels
(without global control)

PASTA Chip

global controller

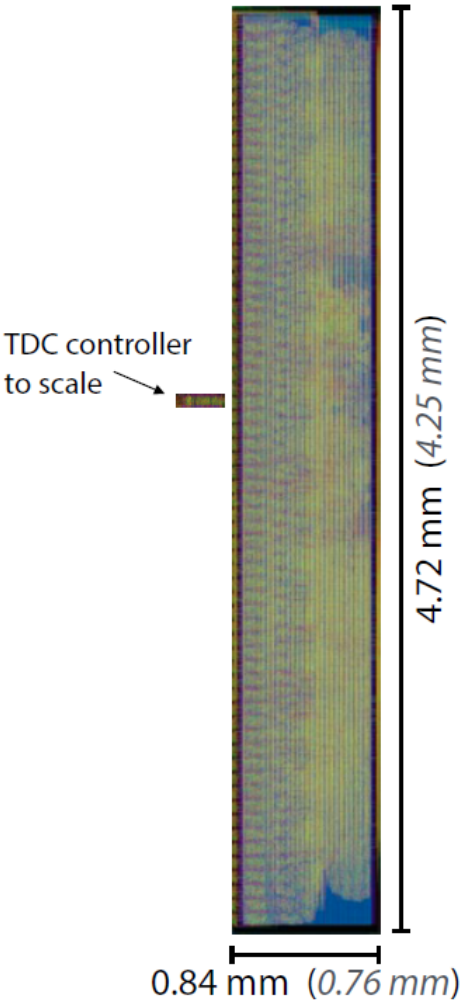


complete ASIC

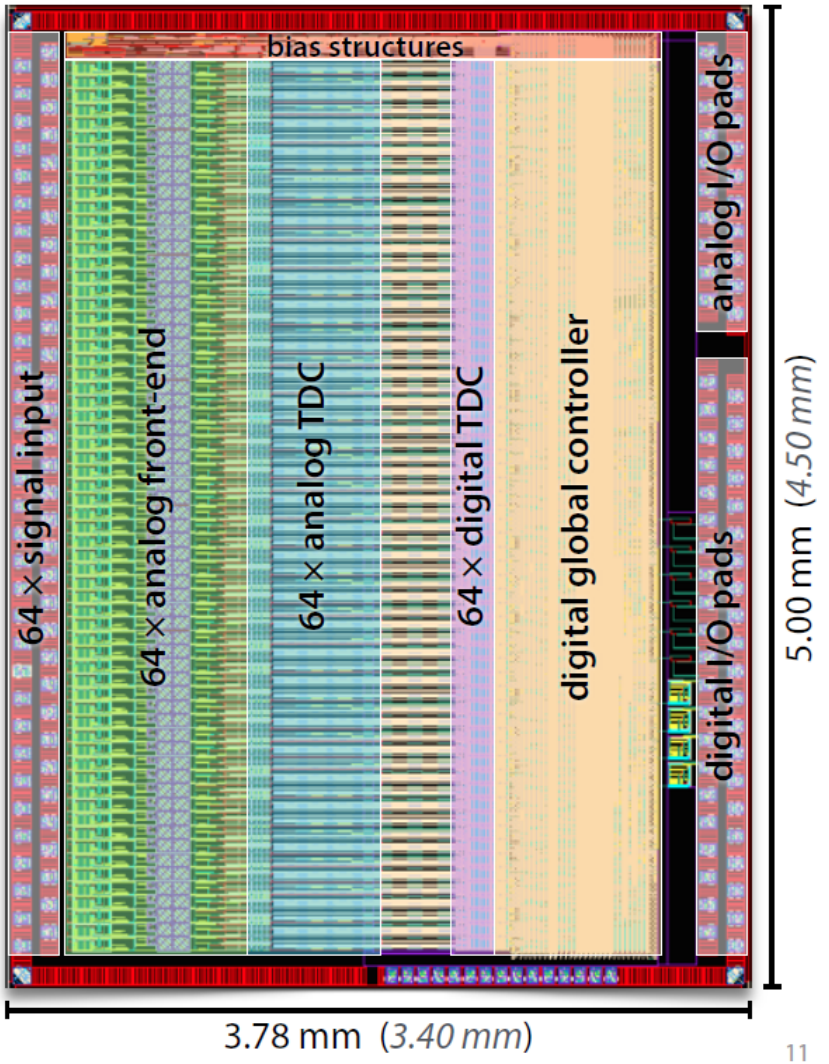


PASTA Chip

global controller



complete ASIC



PASTA Status

- Power consumption based on simulations

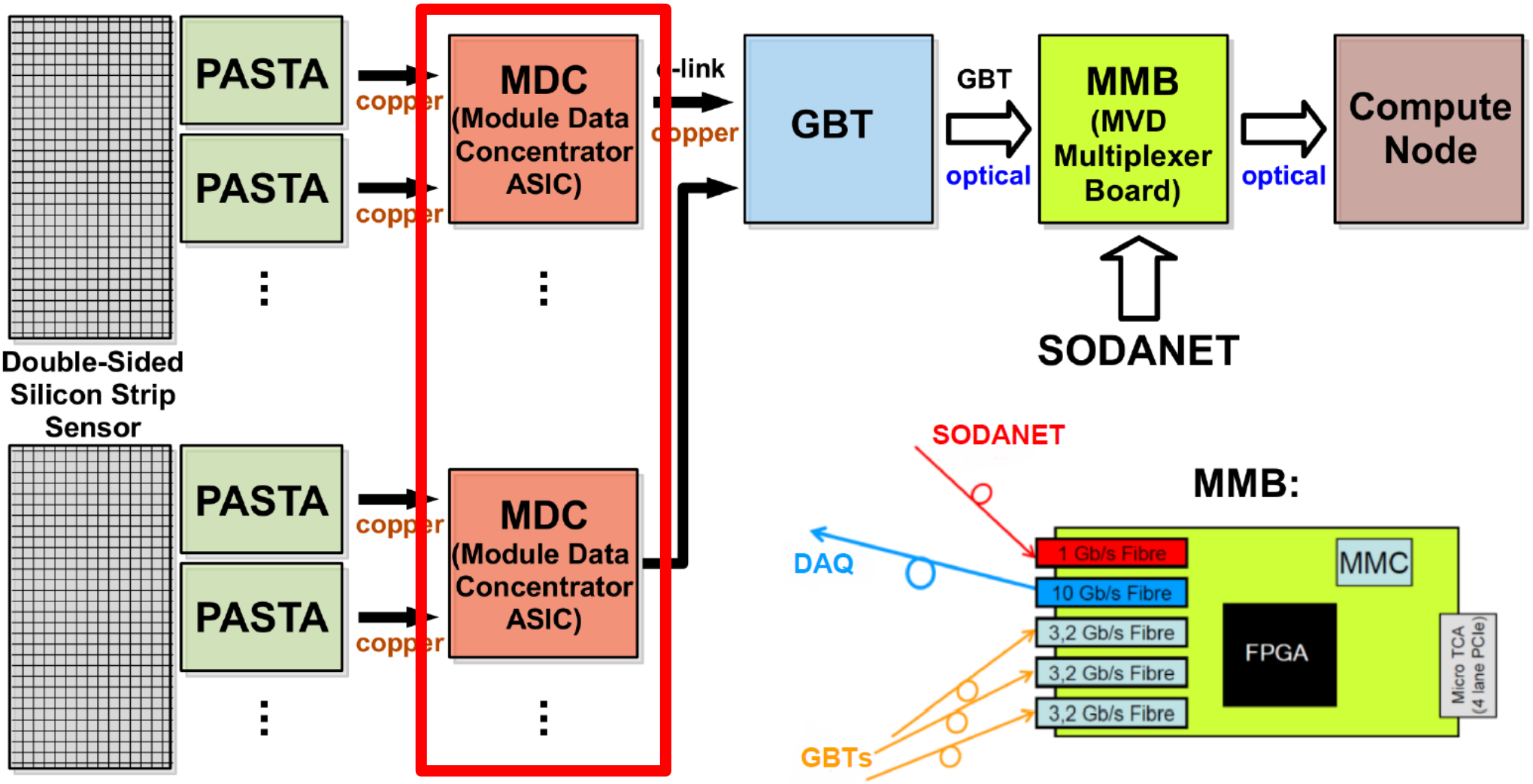
front-end	TDC	TDC ctrl	global ctrl	drivers	**total**
1.0 mW/ch	0.4 mW/ch	0.25 mW/ch	60.0 mW	4 x 8.5 mW	**3.12 mW/ch**

  - target value: < 4.0 mW/ch
  - (LVDS drivers instead of SLVS)

PASTA Outlook

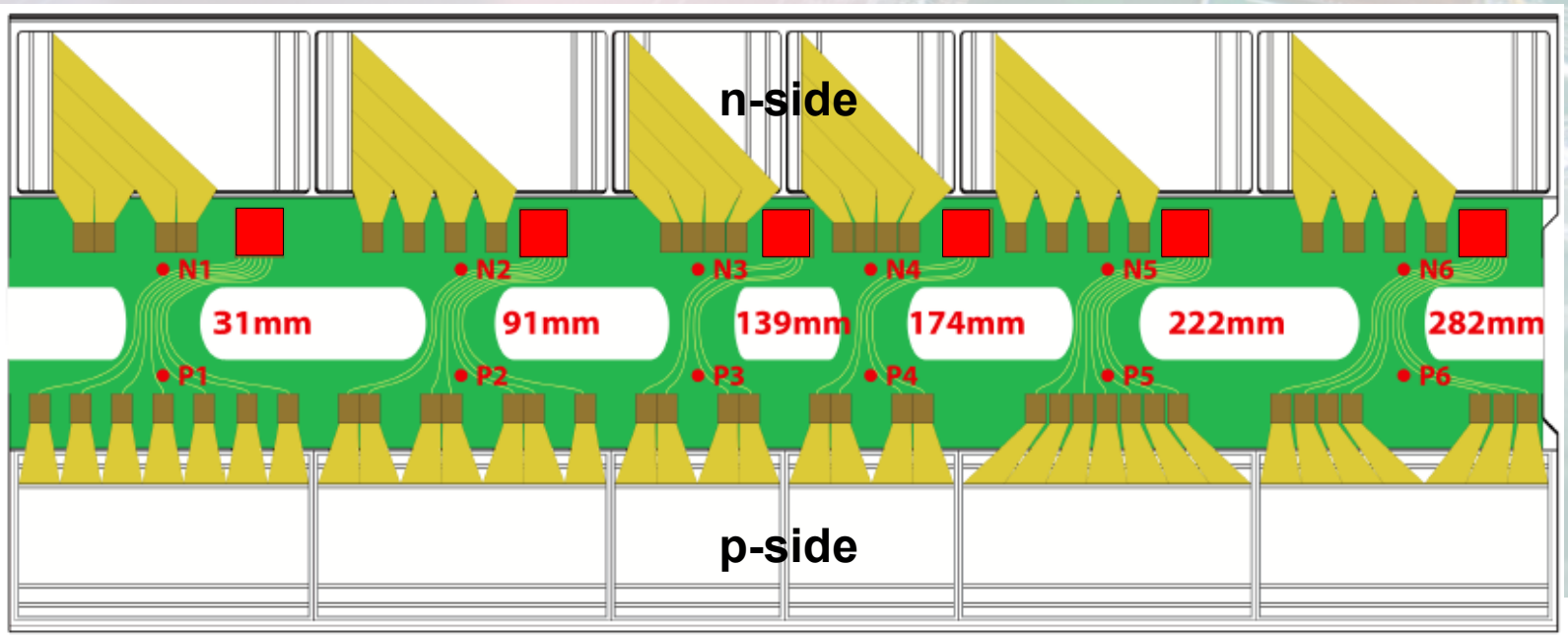
- Analog and digital designs combined
- Implement last modifications
- Complete fixing of issues detected from simulations
- Perform last post-integration simulations to verify design
- Submit the chip to the foundry in April 2015
  (3-4 months to get the first prototype)
- Prepare test system for PASTA prototype tests

Strip DAQ Chain

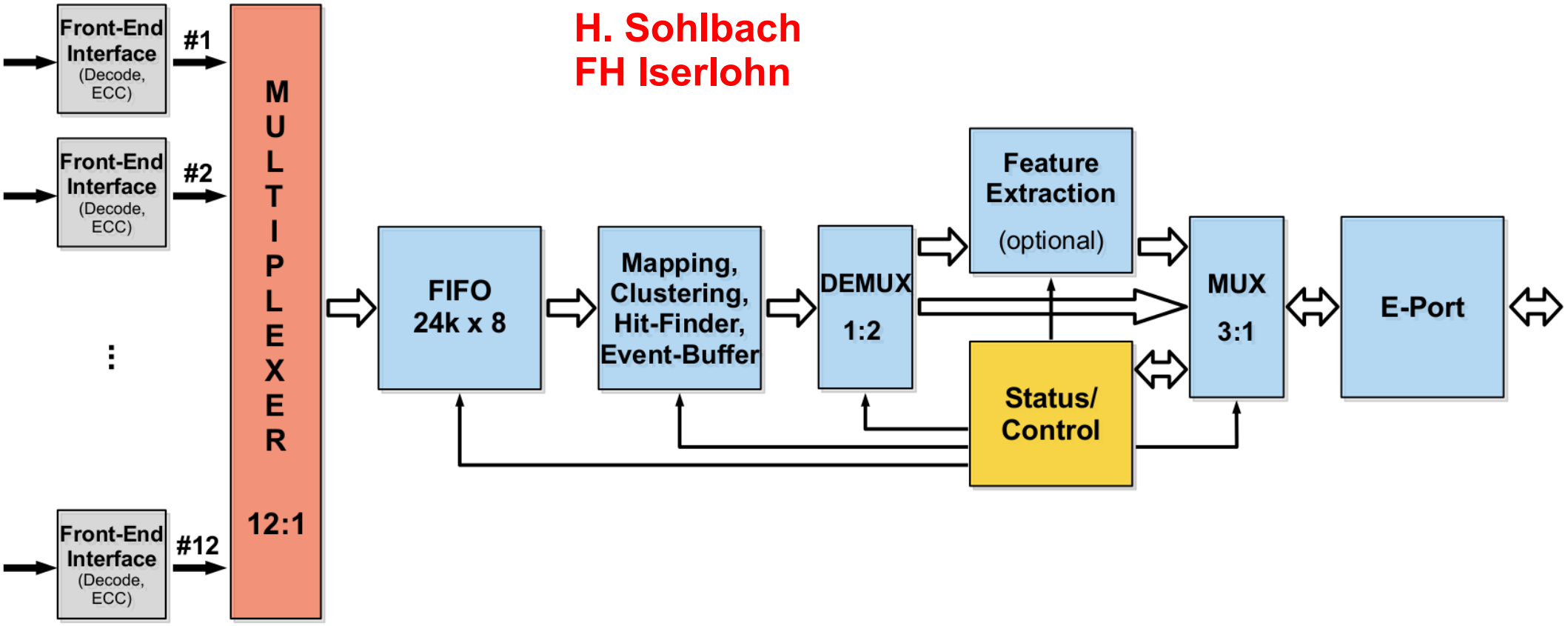


Module Data Concentrator (MDC)

- Data Concentrator ASIC at the stave level
  - Multiplexes all front-ends of one sensor
    - up to 12 front-ends per MDC
    - needs galvanic isolation of data lines, DC-balanced code
  - Slow control interface to front-end chips
  - Data concentration and feature extraction



Module Data Concentrator (MDC)



Module Data Concentrator (MDC)

- Power estimation

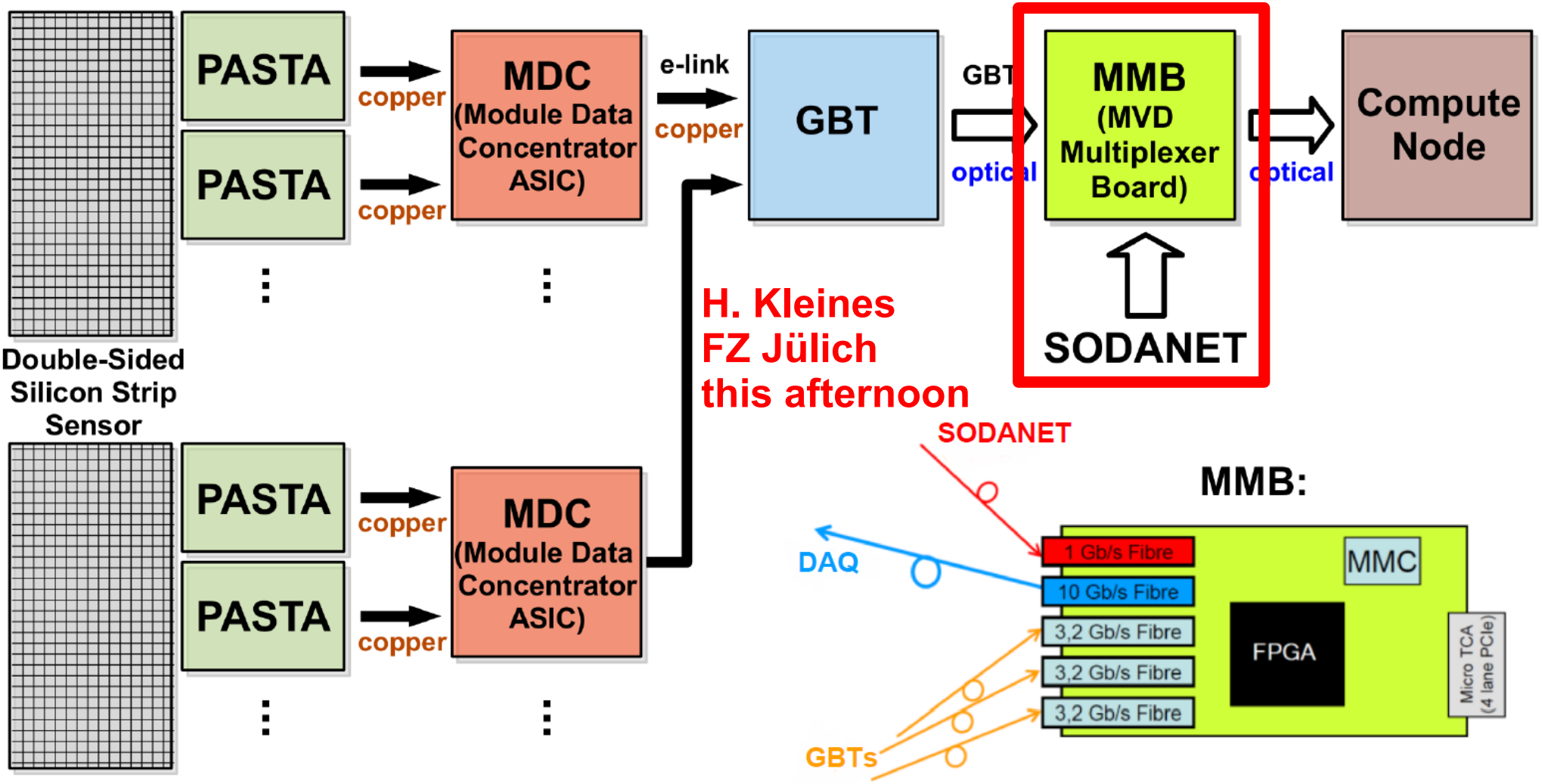
basic design	68 mW
full design	200 mW
SLVS-I/Os	93 mW
Total basic	161 mW
Total full	293 mW

- Chip size estimation
  - 5.0 MGates → approx. 22 mm² @ 230 kgates/mm²
  - 118 pads
- Use same commercial 110nm technology as PASTA
  - triple modular redundancy for all critical components

Module Data Concentrator (MDC)

- Status as of March 2015
  - designed versions with/without feature extraction
  - design and simulation of FPGA prototype (VHDL-based) is finished for:
    - 12:1 Multiplexer
    - FIFO
    - front-end interface
    - 10b/8b-decoding
    - triple redundancy
  - under simulation: triple redundancy
  - under design/simulation: clustering/hitfinder
  - to be done:
    - status and control
    - e-link
    - slow control

Strip DAQ Chain



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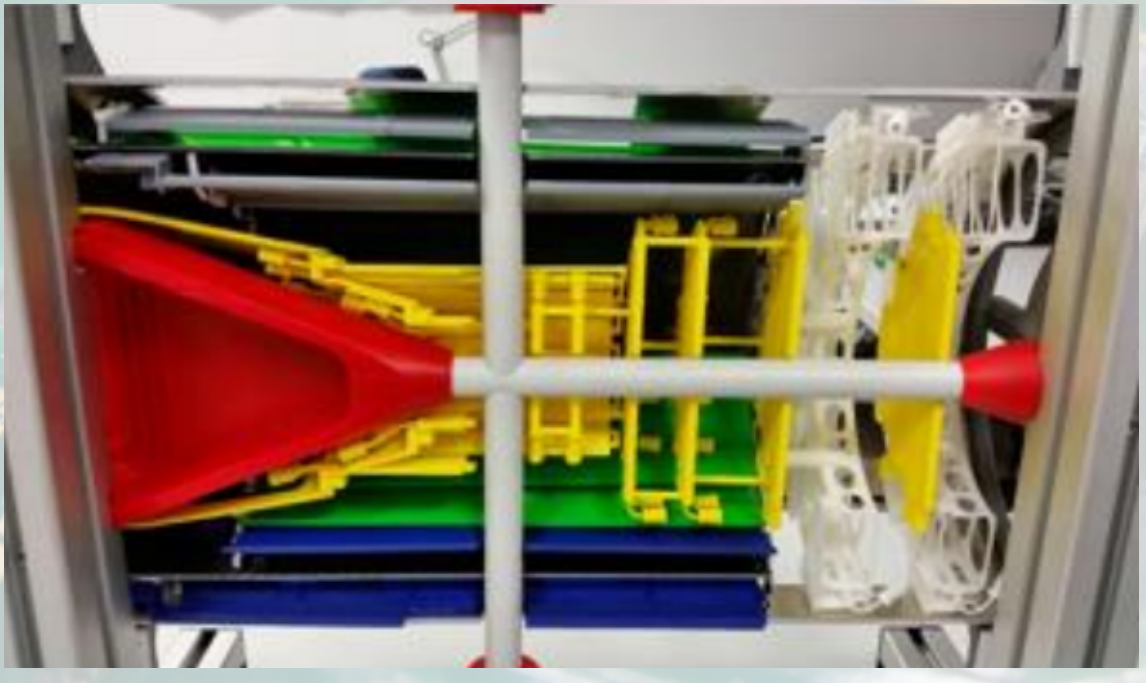
Thank you for your Attention



HIC for FAIR
Helmholtz International Center

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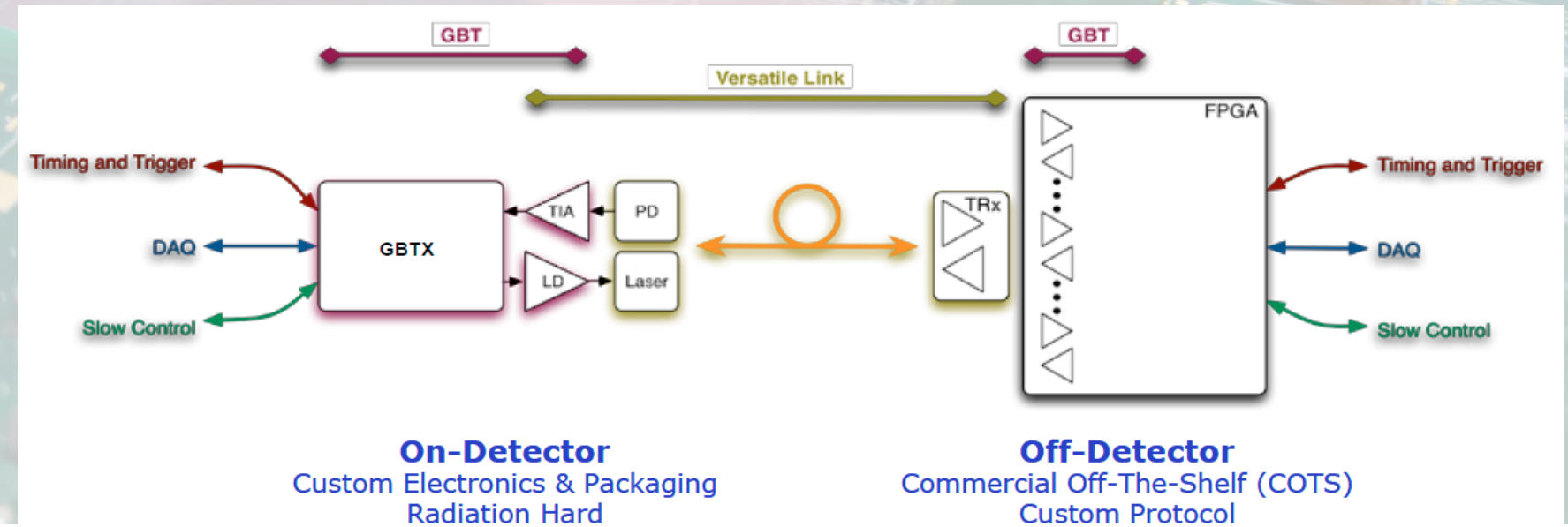
GBT

- Additional data concentration level
  - Multiplexes several MDCs connected via e-link protocol
  - Placed close to MVD
    - reduce length of electrical links
  - Fast optical links towards off-detector electronic
    - 3.2 Gbps user data rate



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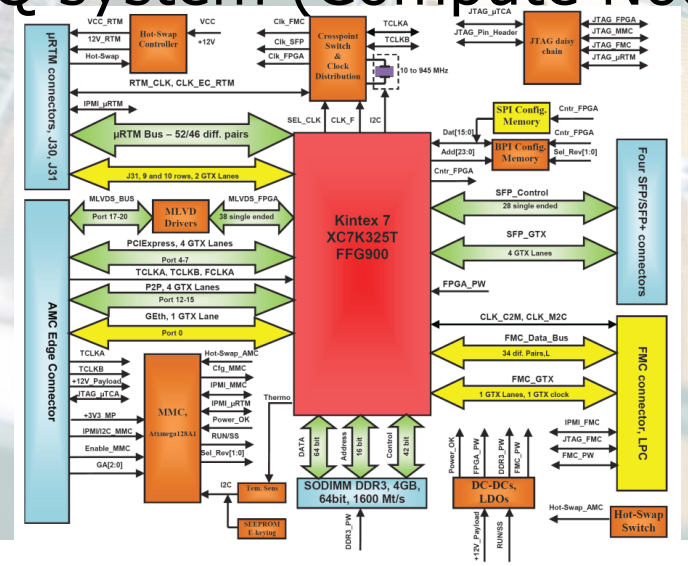
MVD Multiplexer Board (MMB)

- Off-detector electronics of the MVD

(Developed in the Helmholtz Association of German Research Centers)

- MTCA.4 compatible AMC module
  - based on Xilinx Kintex-7 FPGA
  - 4 SFP/SFP+ cages (GTX transceiver)
- Connection to PANDA time distribution system (SODANET)
- Sends data to global PANDA DAQ system (Compute Nodes)

H. Kleines, M. Drochner, P. Wüstner
ZEA-2, FZ Jülich

DAQ

GBTs