PANDA FEE-DAQT Workshop

Sezione di Torino

Status report on the MVD pixel detector electronic readout

G. Mazza
on behalf of the Torino MVD pixel group

Pixel Detector

Sezione di Torino

Pixel size	$100 \times 100\ \mu m^2$
Chip active area	$11.4 \times 11.6\ mm^2$ (116 rows, 110 columns)
dE/dx measurement	ToT, 12 bits dynamic range
Max input charge	50 fC
Noise floor	<32 aC (200 e^-)
Input clock frequency	160 MHz
Time resolution	6.25 ns (1.80 ns r.m.s.) 12.5 ns (3.61 ns r.m.s.)
Power consumption	< 800 mW/cm^2
Max event rate	$6.1 \cdot 10^6$
Total ionizing dose	< 100 kGy

Module readout

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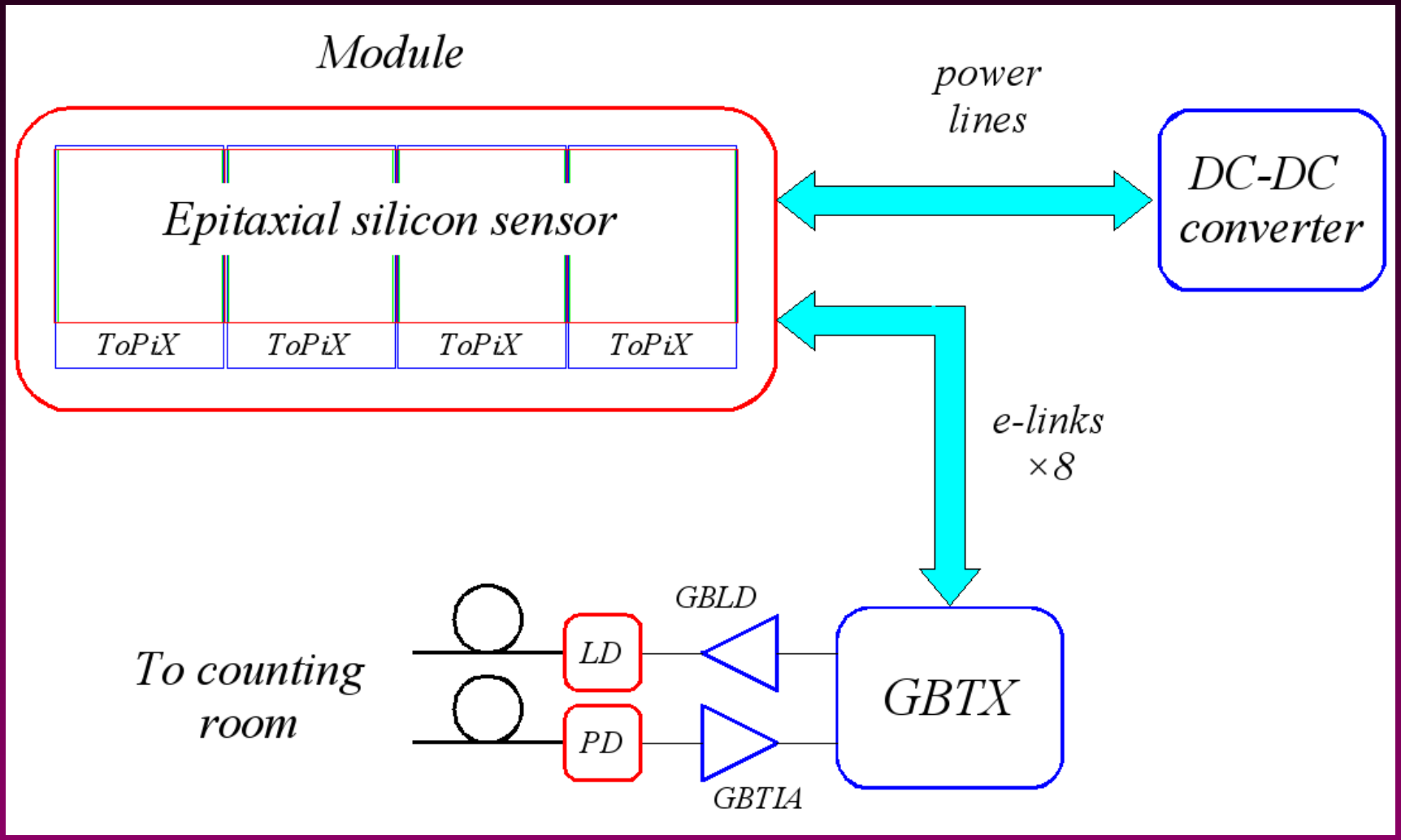

ToPiX prototype R/O architecture

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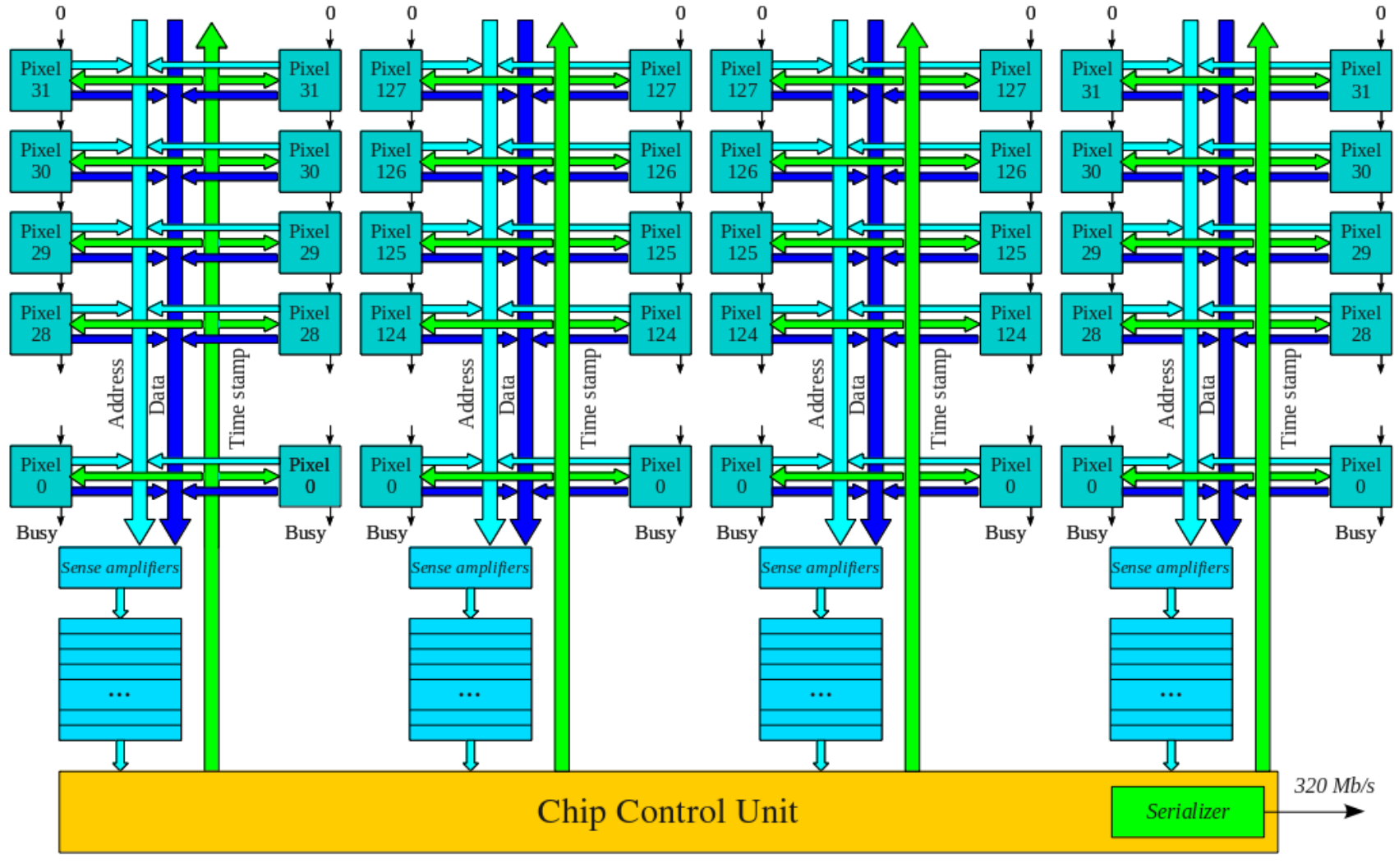

ToPiX v3

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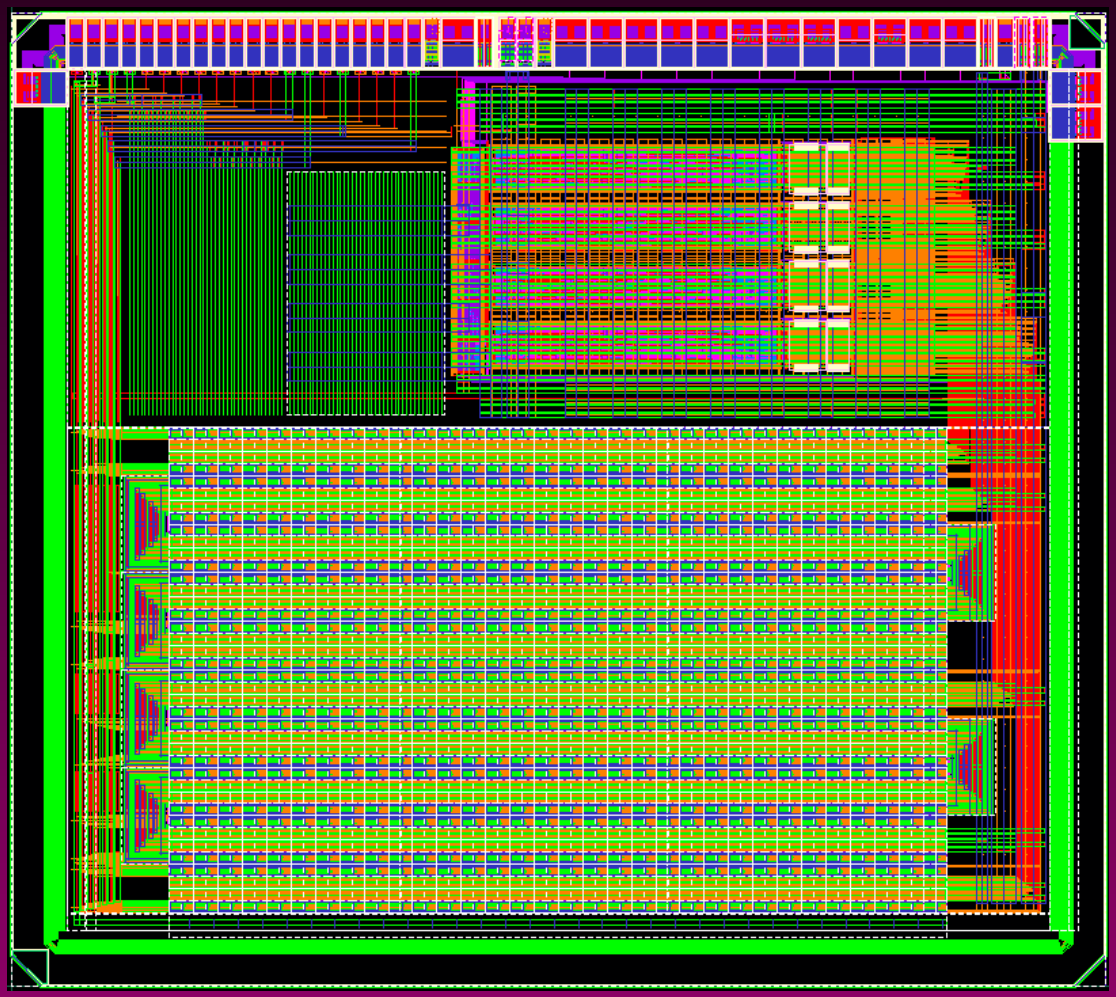
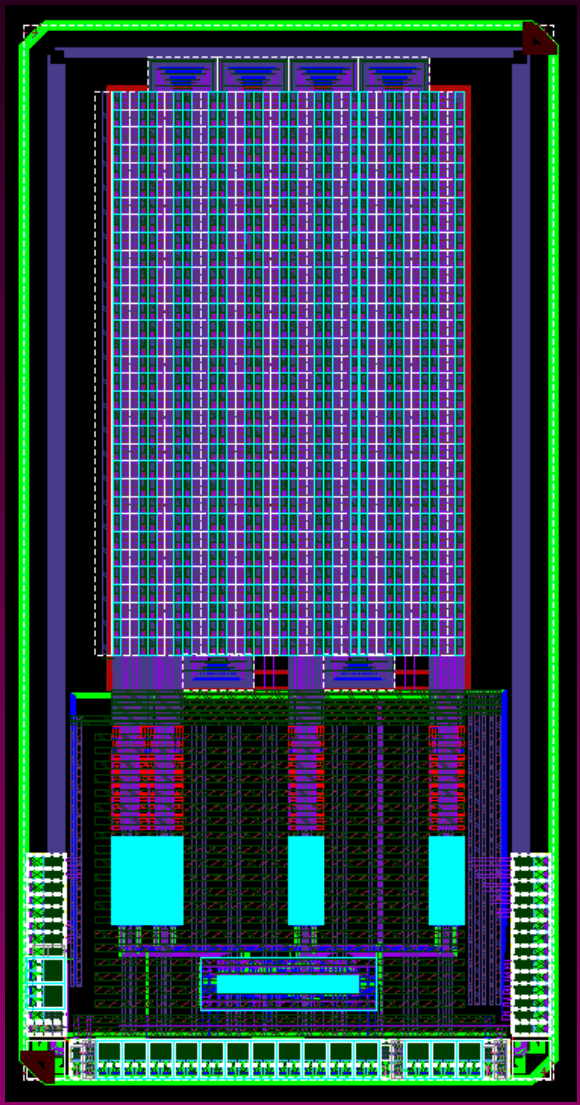


- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

ToPiX v4

Sezione di Torino



- Size : 3 mm × 6 mm
- CMOS 130 nm
- 640 pixel cells, 2×2×128 and 2×2×32 columns
- Hamming encoding and TMR pixel logic protection schemes
- Compatible with v3 sensors
- Clock frequency 160 MHz
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT-compatible SLVS I/O
- *Received on Feb 18th 2014*

Changes from v3 to v4

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Analog cell :

- Analog gain *(not ToT gain)* increase for better linearity in the sub 1 fC region
- Radiation tolerance of the clipping circuit
- Threshold control DAC linearization

Column readout @ 160 MHz

- Improved driver
- Bus capacitance reduction

System aspects :

- DDR readout
- Frame based transmission

Data format

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2	12	8	12	6
01	Chip address	FC	Not used	ECC

Frame header packet

2	14	12	12
11	Pixel address	Leading edge time	Trailing edge time

Data packet

2	16	16	6
10	# of events	CRC	ECC

Frame trailer packet

2	38
00	idle code (Hex 3A55AA55AA)

Idle packet

Other features

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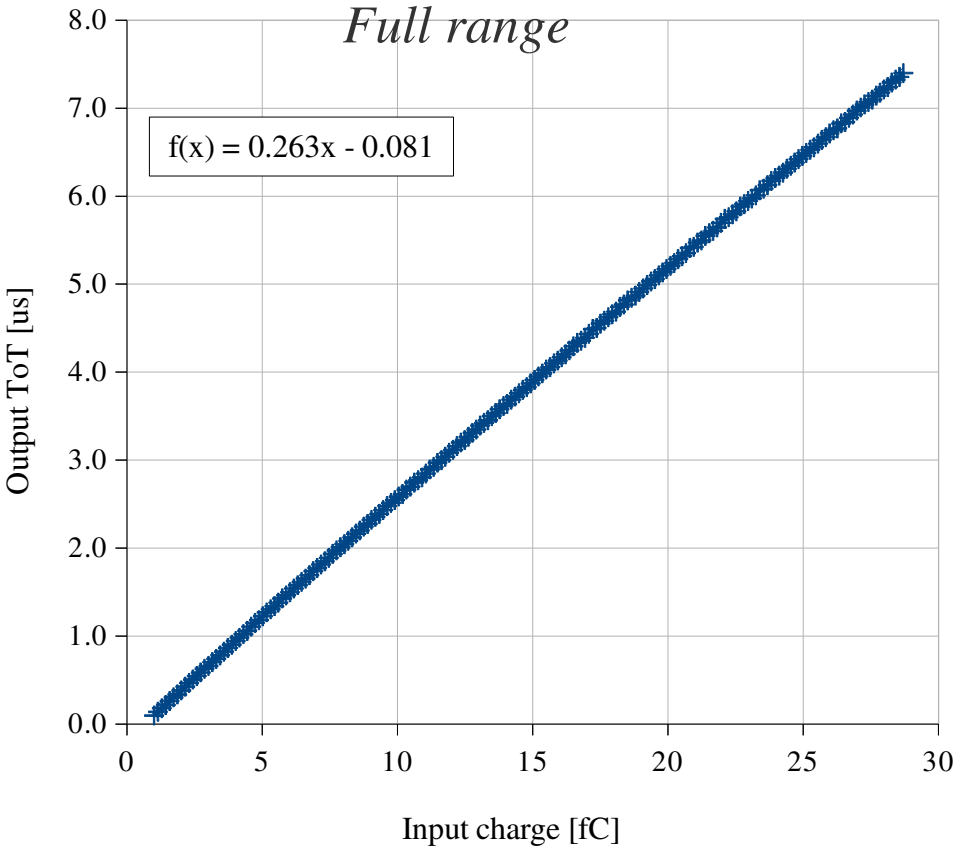
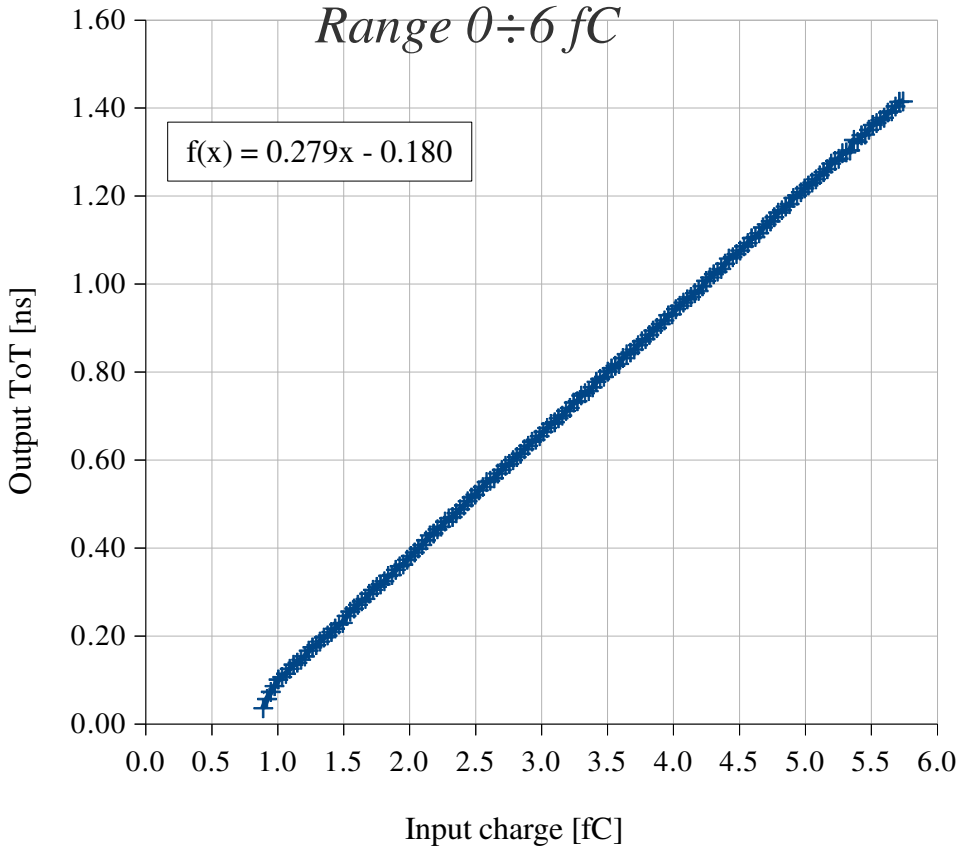
Output frequency	*160 Mb/s*	*320 Mb/s*
Time stamp counter frequency	*160 MHz*	*80 MHz*
Time stamp mode	*Binary*	*Gray*
Idle packet	*off*	*on*
Analog timeout	*off*	*on*
Detector type	*n-type*	*p-type*
SLVS current control	*0000 (max)*	*1111 (off)*
Driver pre-emphasis	*off*	*on*

ToT measurements

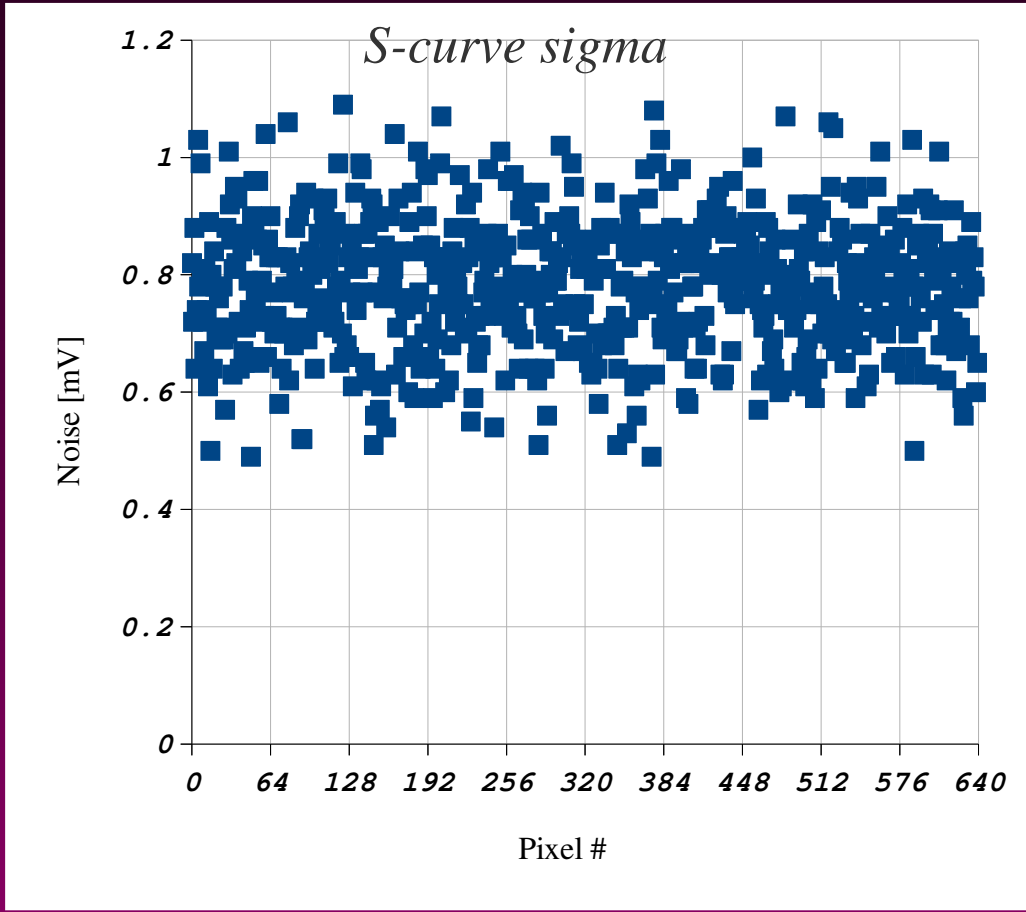
Sezione di Torino

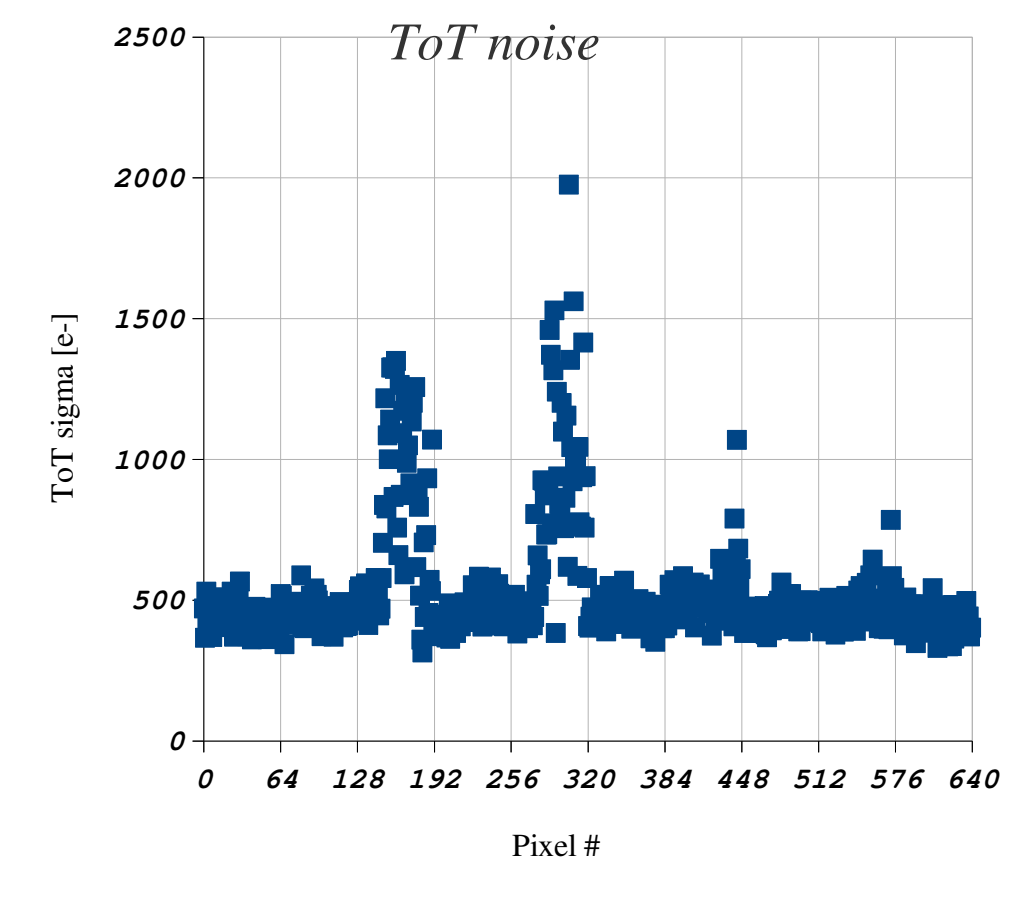




Noise measurements

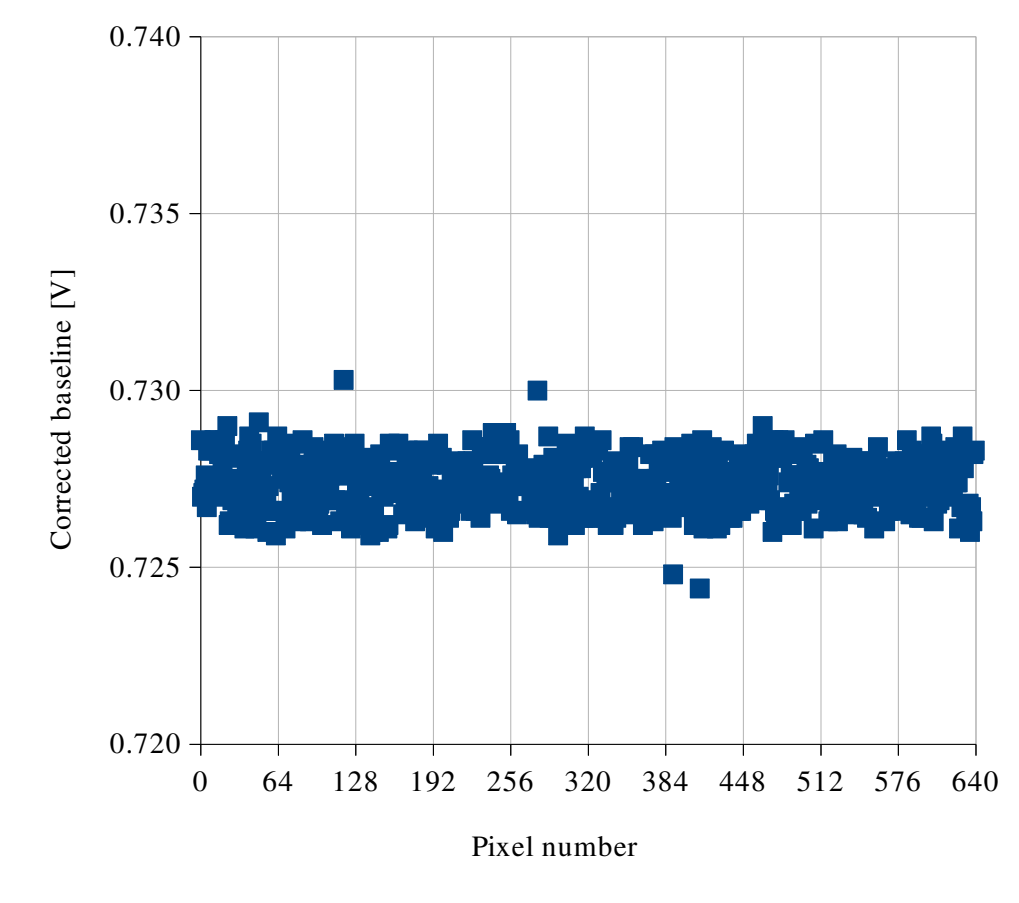
Sezione di Torino

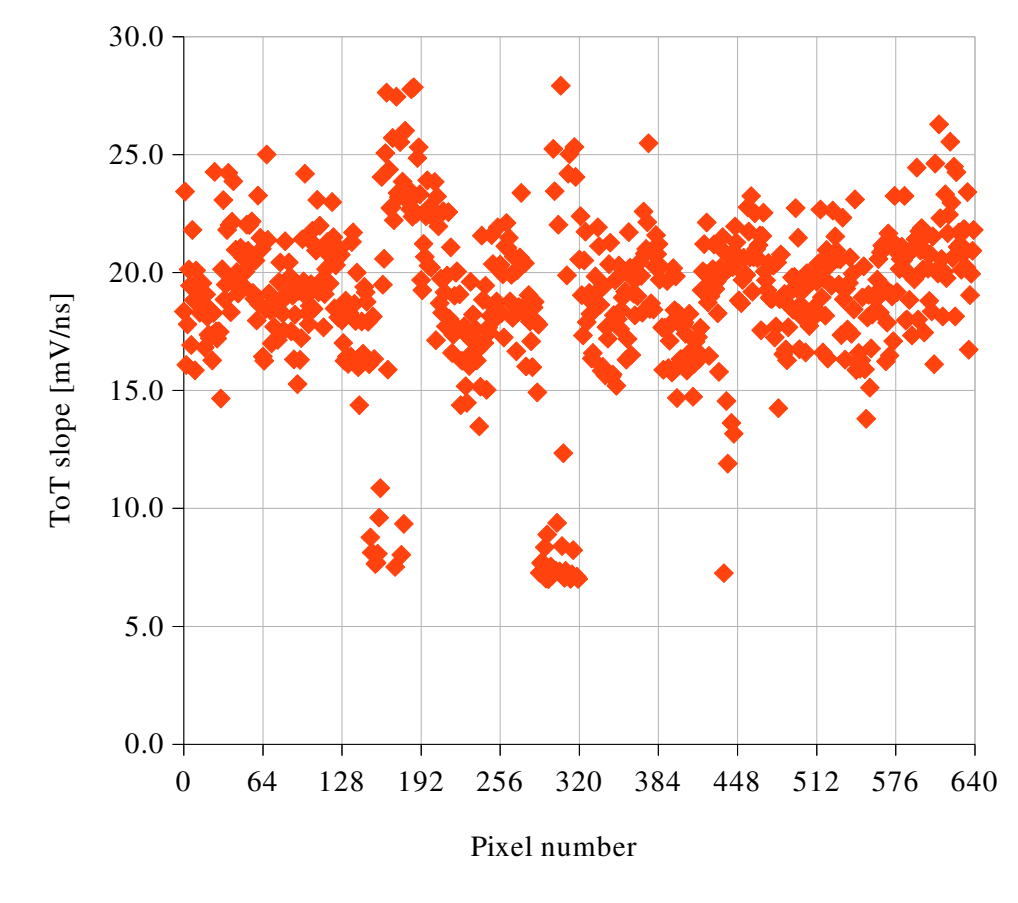




Baseline & ToT

Sezione di Torino

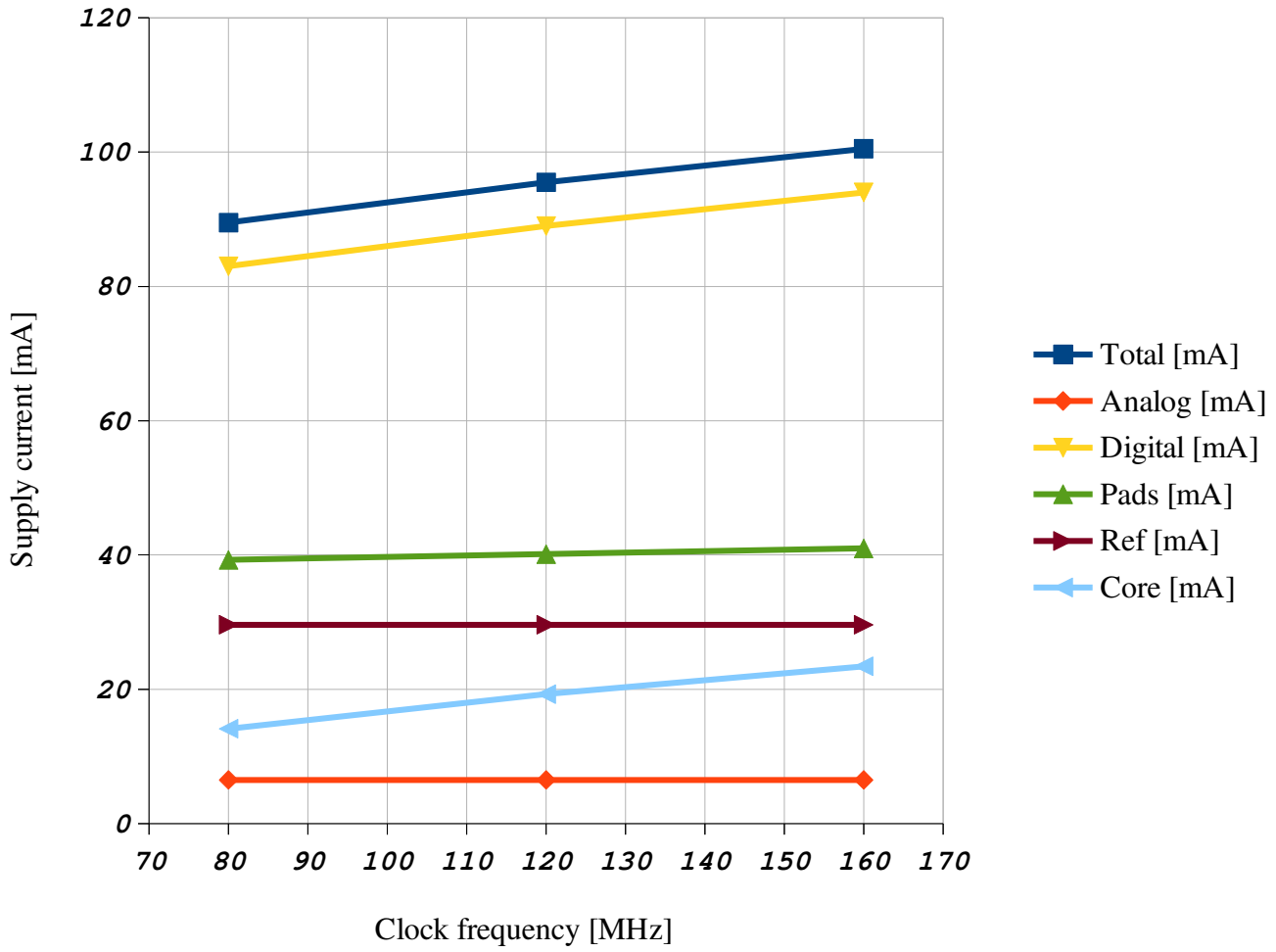




Baseline average value : 727 mV

Baseline sigma : 0.73 mV

Supply current

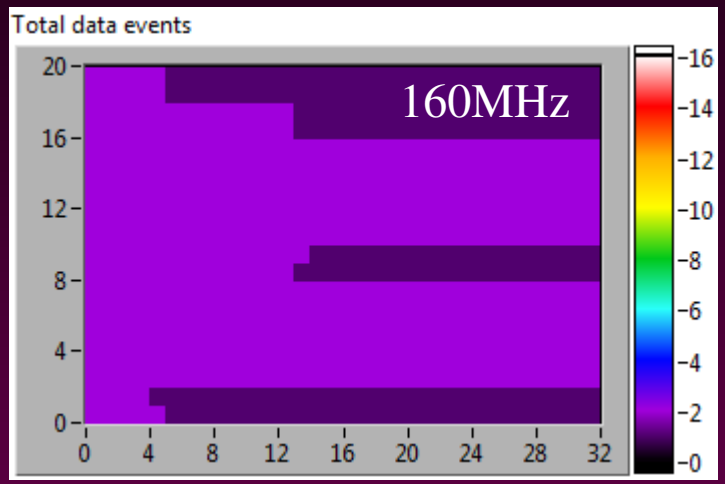


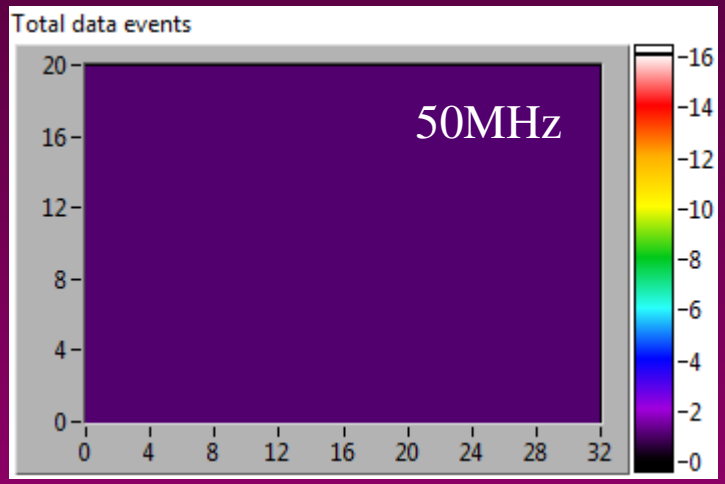
Estimated power density for the full size version :

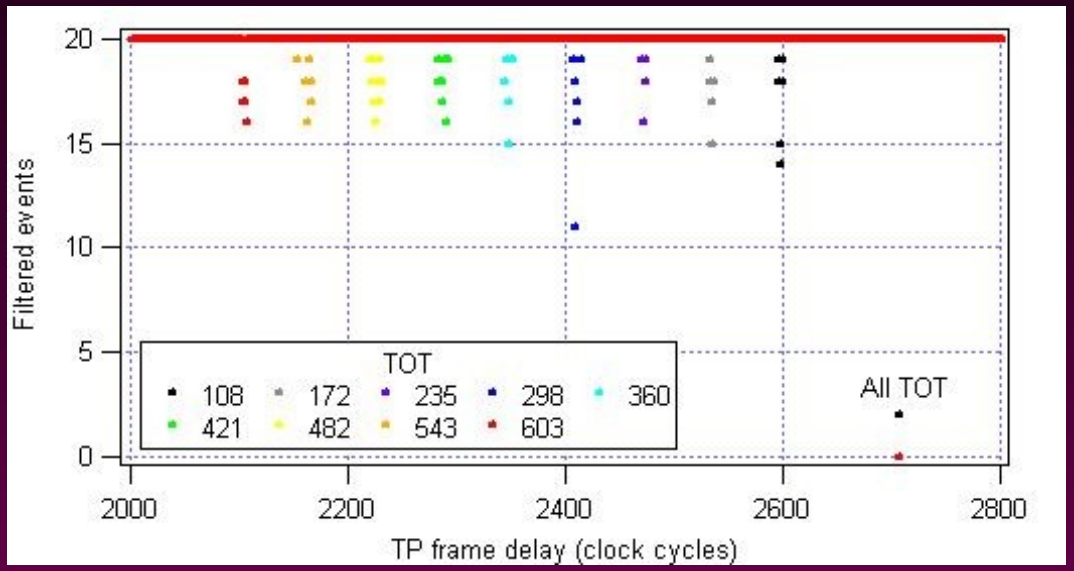
523 mW/cm^2 @ 80 MHz
666 mW/cm^2 @ 120 MHz
725 mW/cm^2 @ 160 MHz

Dummy events issue

Sezione di Torino



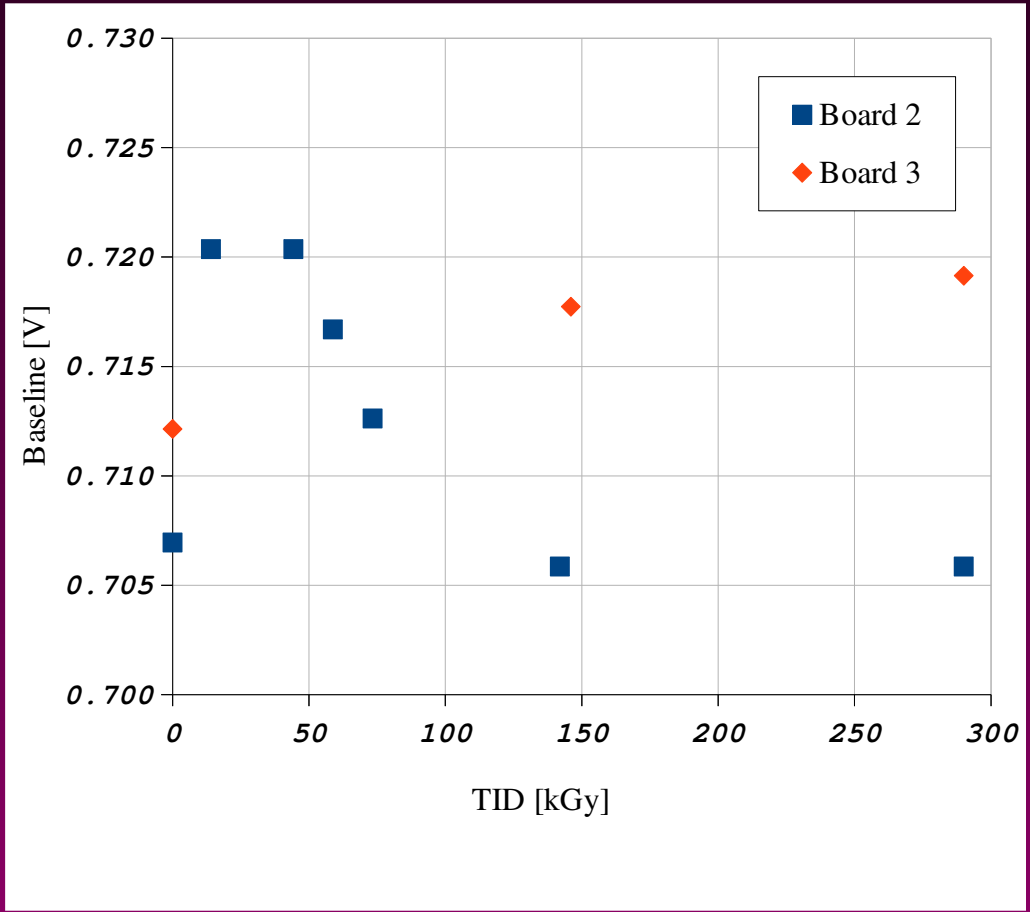


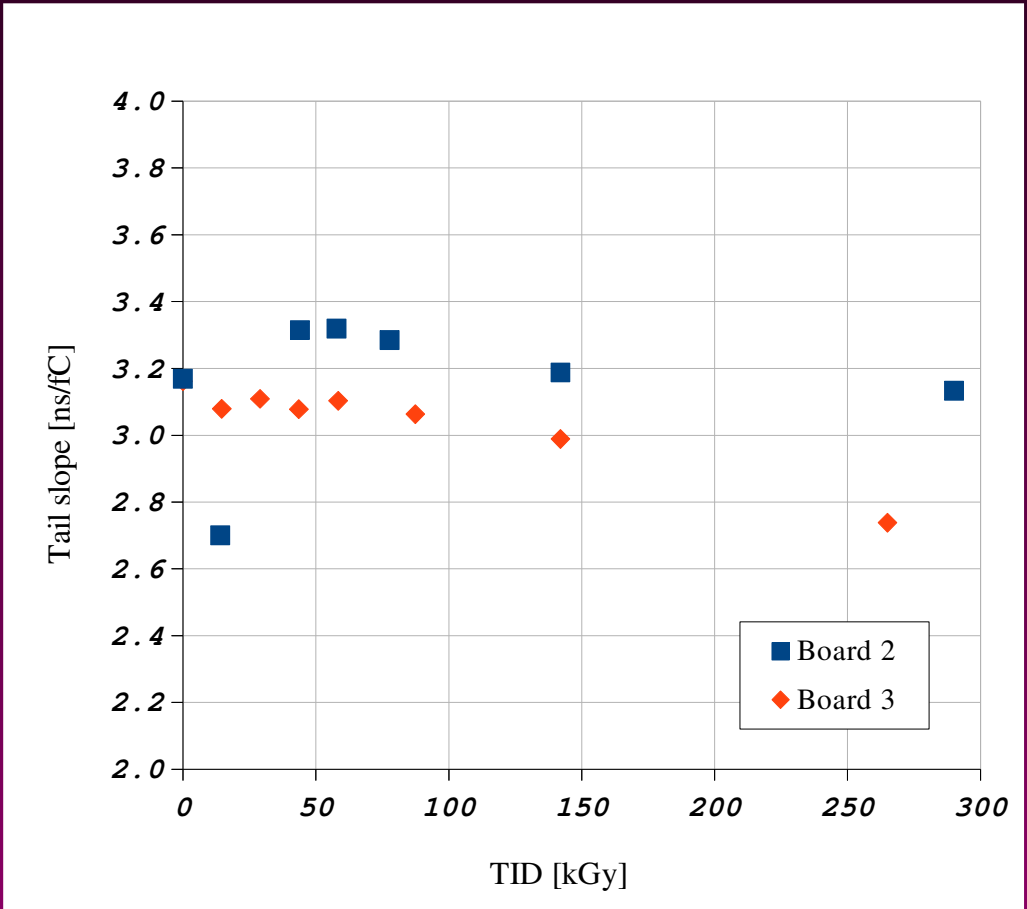


Dummy events are generated in many cases @ 160 MHz
Reason : busy propagation delay underestimated
To be corrected in the next version
Workaround : filter out events with LE or TE = FFF
Some loss in efficiency
Note : FFF in Gray is AAA in binary !

TID mesurements baseline – tail slope

Sezione di Torino

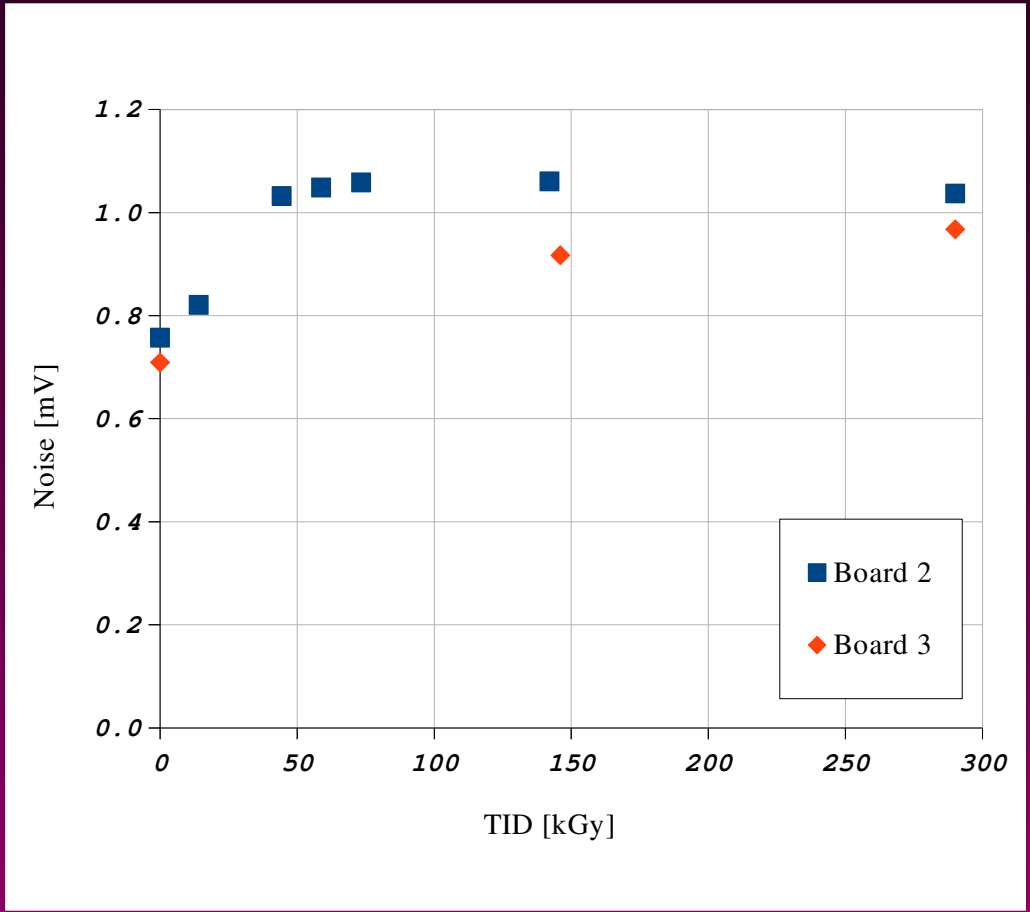




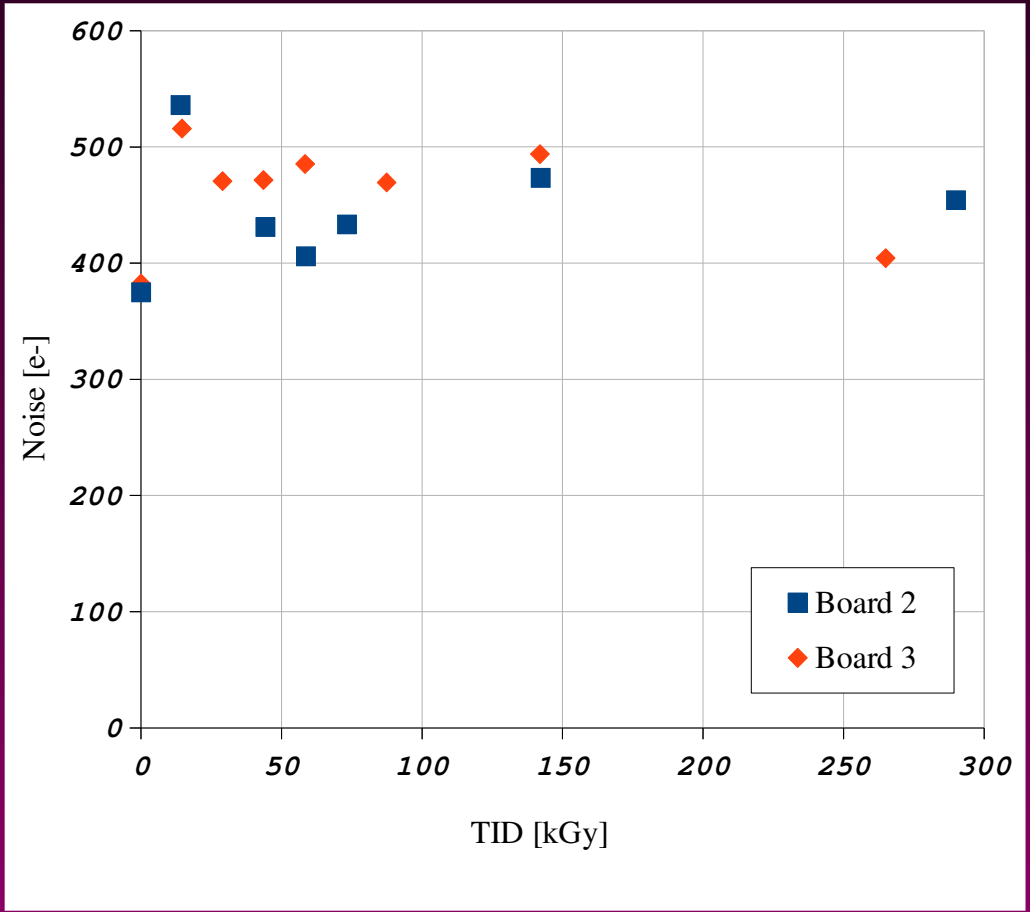
TID mesurements baseline – tail slope

Sezione di Torino

S-curve sigma

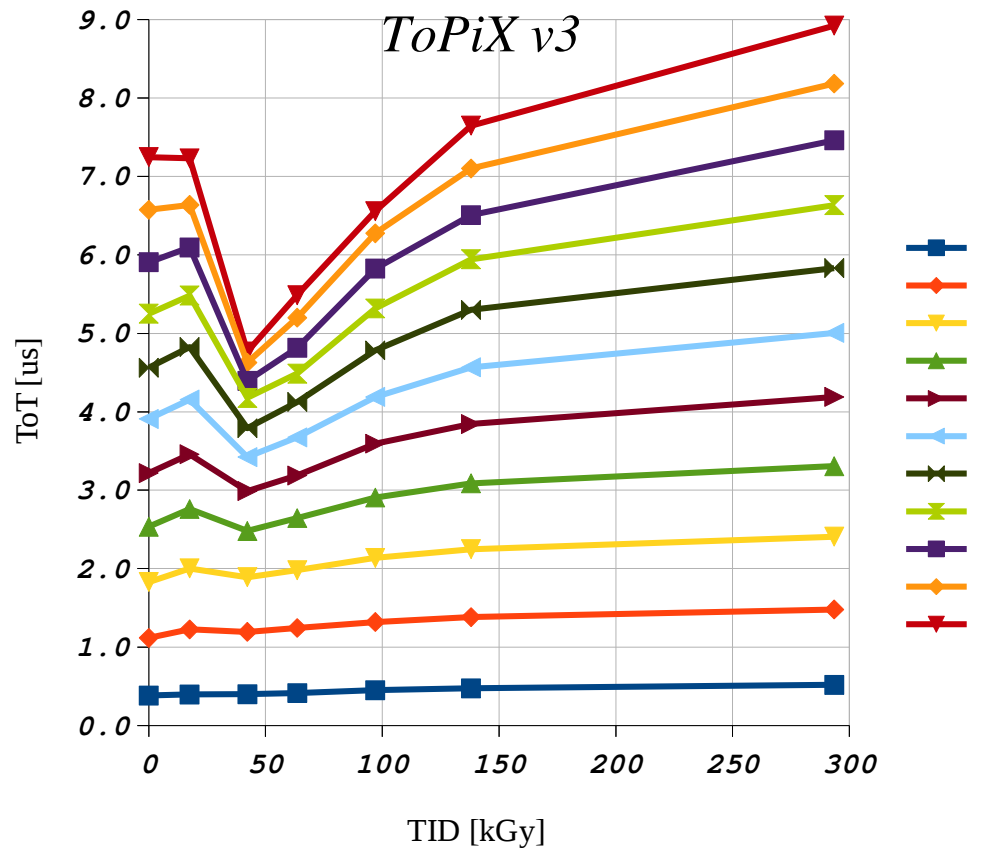


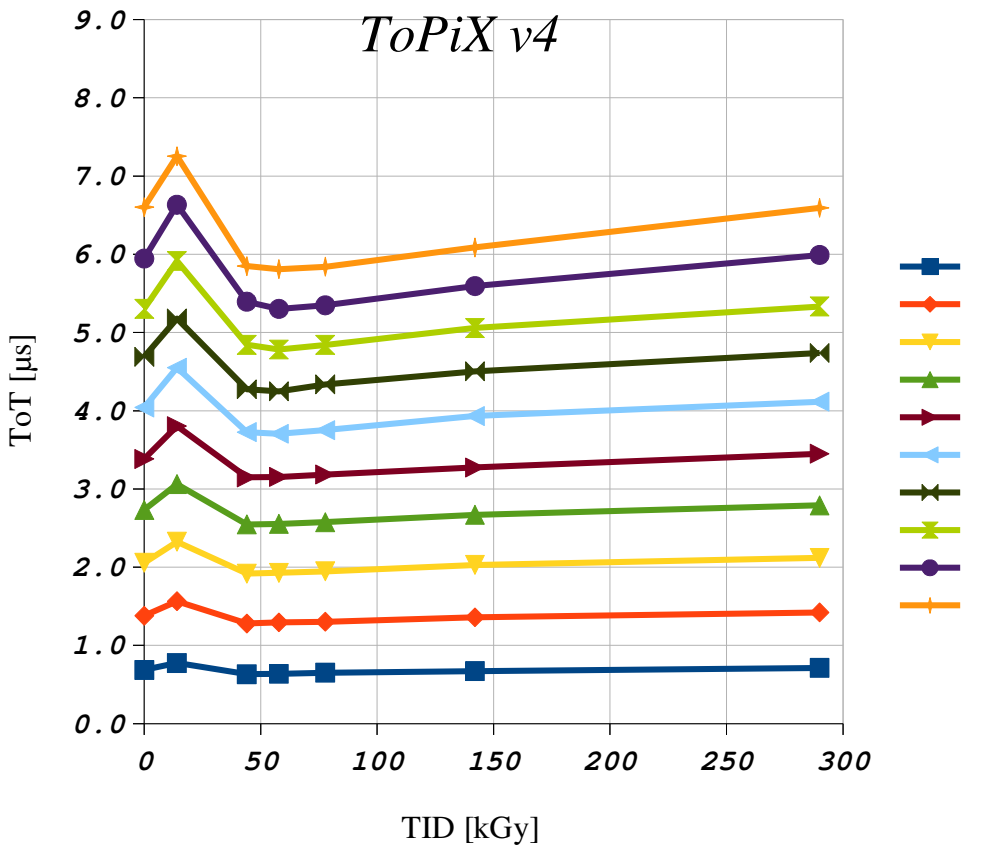
ToT noise



TID mesurements ToT

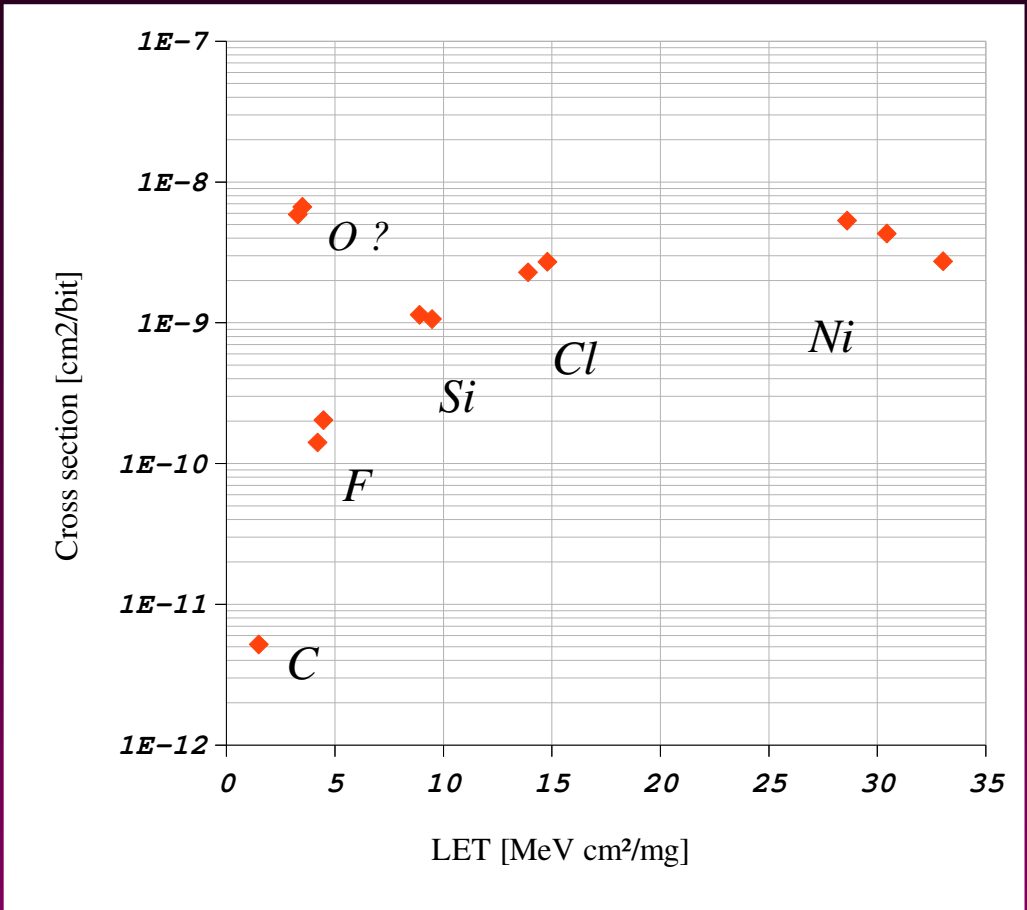
Sezione di Torino

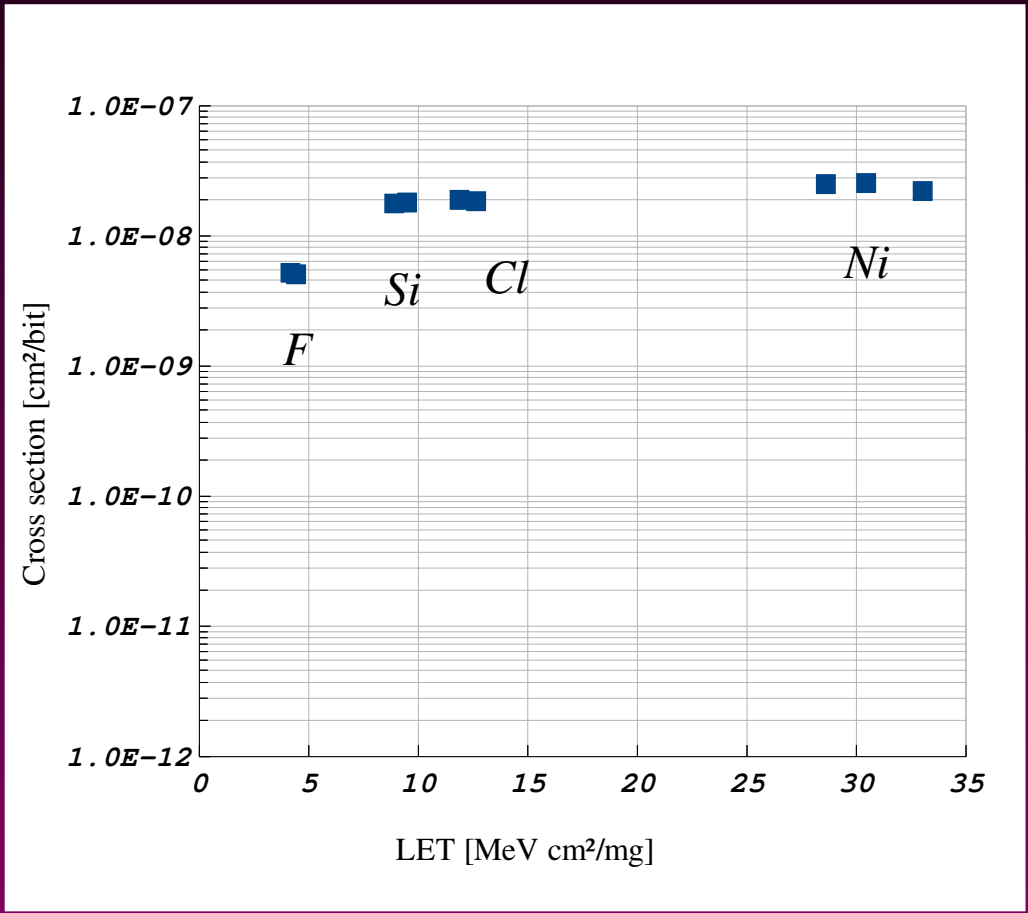




SEU test

Sezione di Torino

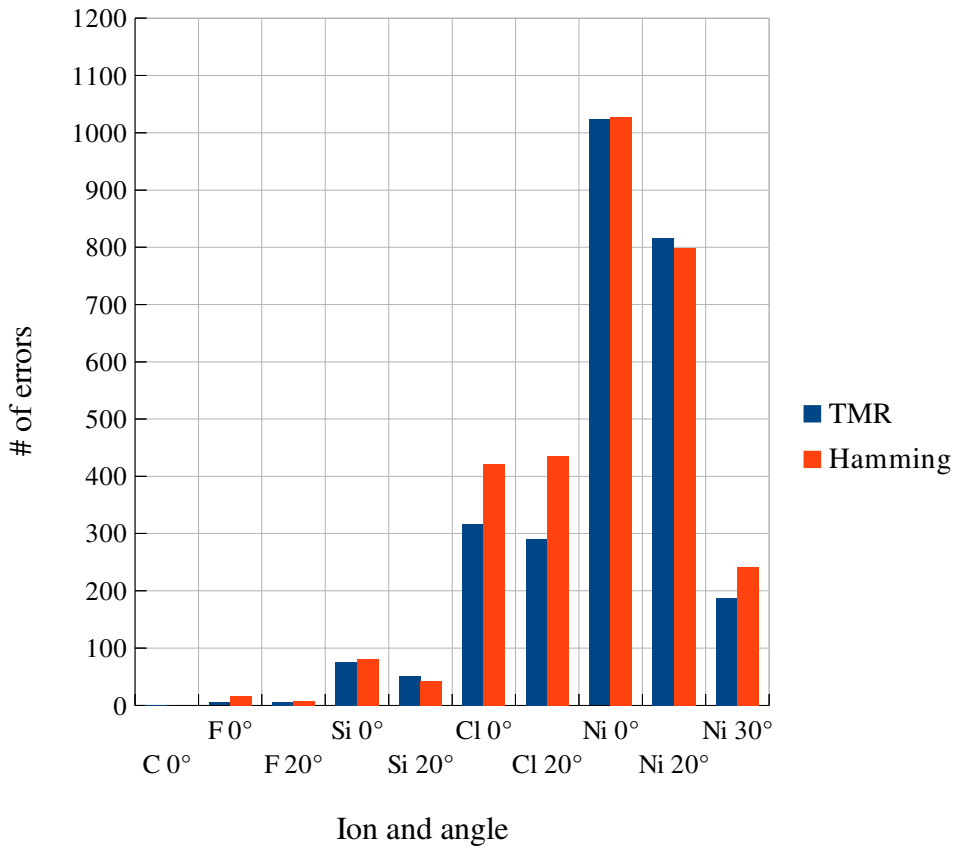


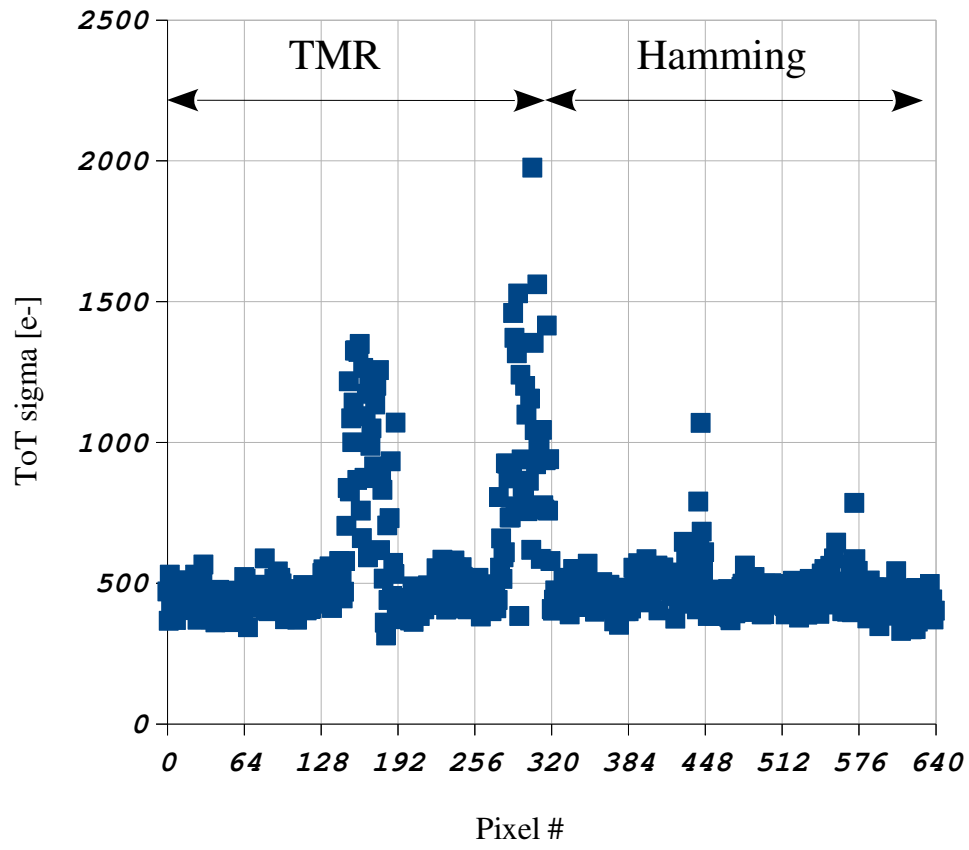


Pixel configuration registers

Hamming-corrected errors
No uncorrected errors detected

TMR vs Hamming





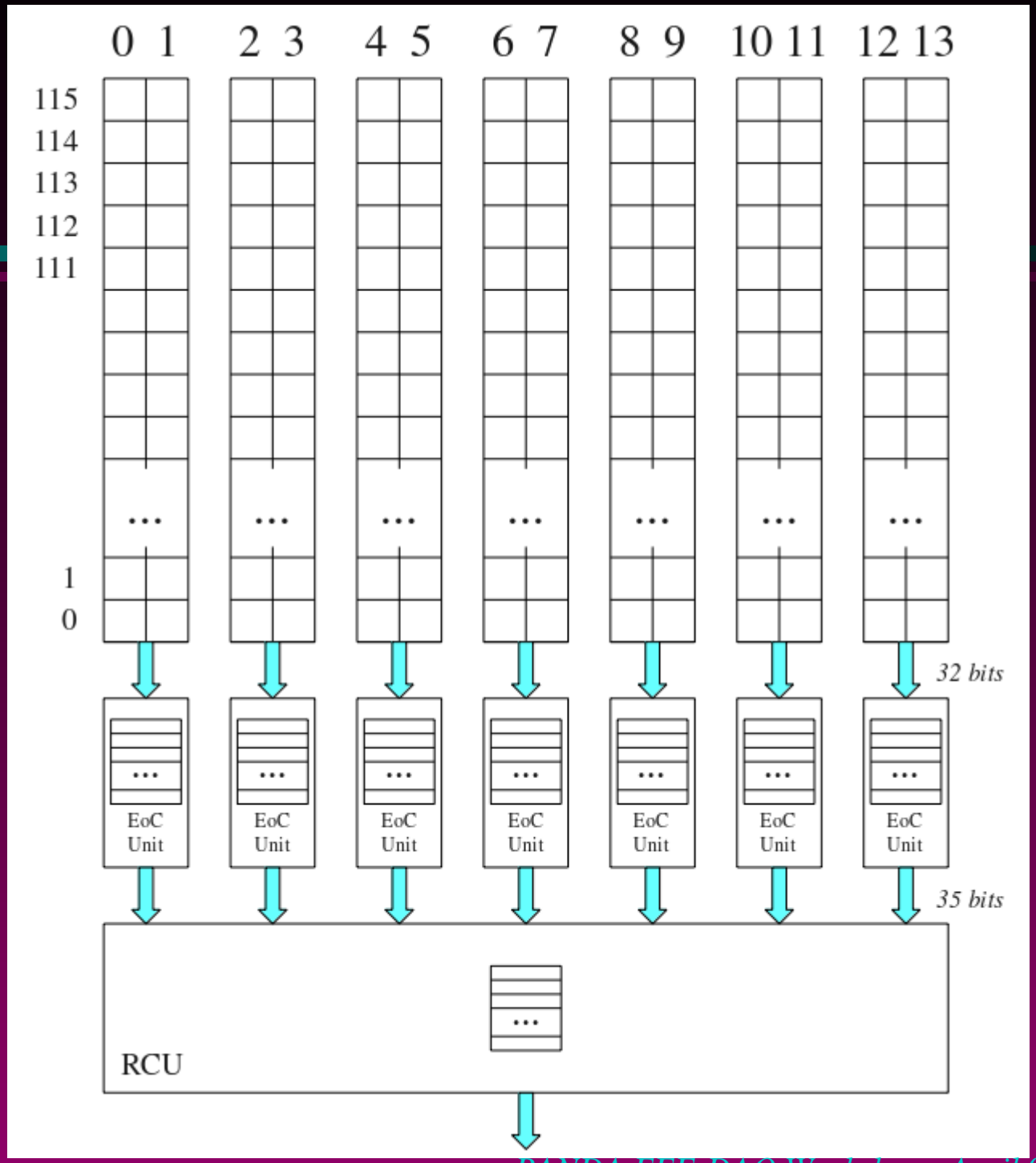
ToPiX v5

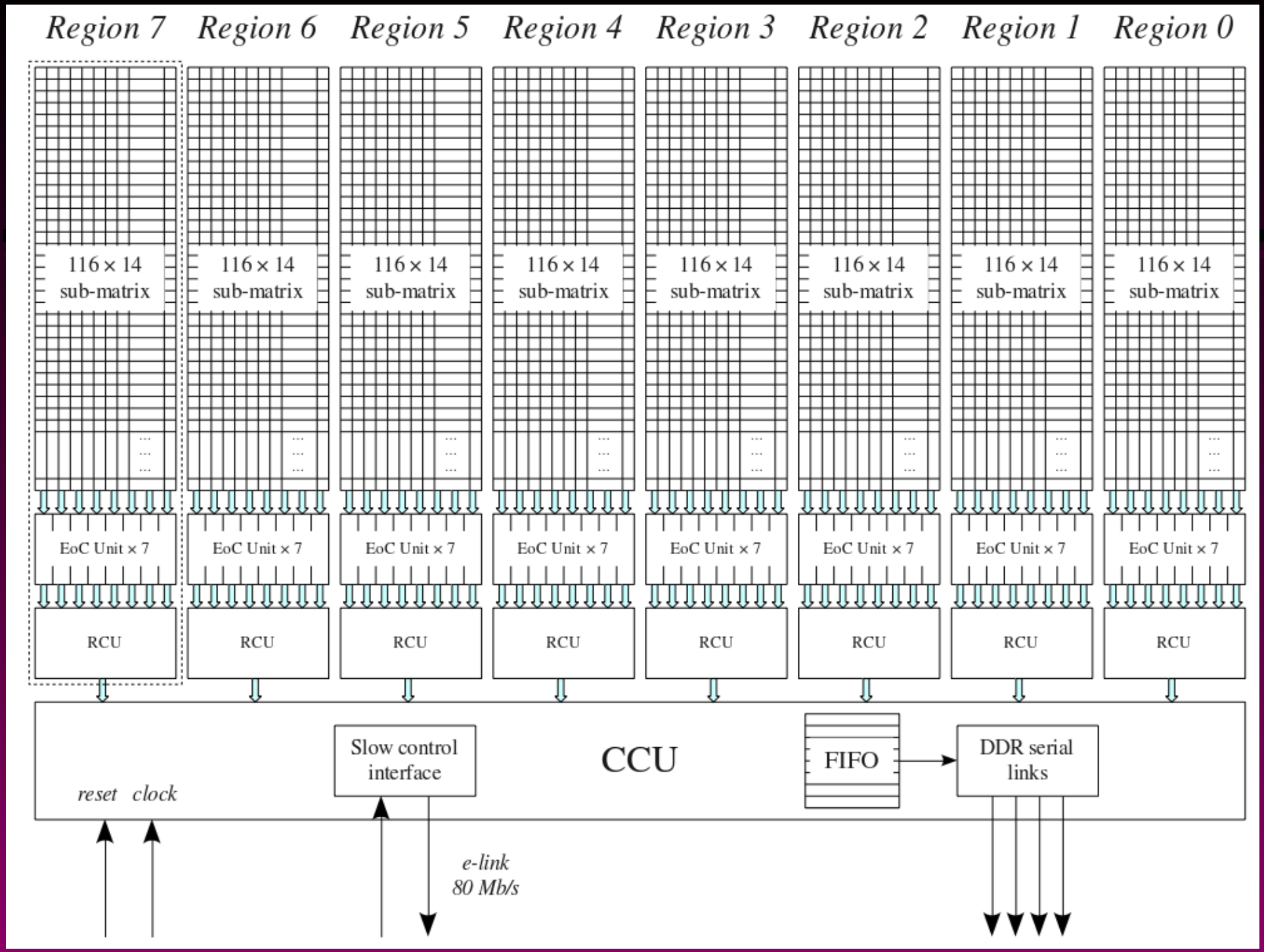
Sezione di Torino

- Full size chip design started
- Size (*preliminary*) : 11.2 mm × 14.8 mm
- Pixel matrix (*preliminary*) : 110 × 116
- Input clock : 160 MHz
- Max output bandwidth : 4 × 320 Mb/s
- Supply voltage : 1.2 V
- Columns divided in 8 regions with 7 double columns each
- Triple tier buffering (FIFO at the end of column, region control and chip control units)

REGION :

14 double columns
7 EoC Units
1 RCU




Region 7
Region 6
Region 5
Region 4
Region 3
Region 2
Region 1
Region 0
116 × 14 sub-matrix
EoC Unit × 7
RCU
CCU
Slow control interface
FIFO
DDR serial links
reset
clock
e-link 80 Mb/s

ToPiX v5 interface

Sezione di Torino

- reset *(SLVS or CMOS input – PON ?)*
- clock *(SLVS inputs, from e-link)*
- data output *(1-4 lines, SLVS outputs, 160/320 Mb/s, to e-link)*
- control input/output *(2 lines, SLVS, 80 Mb/s, from/to control e-link)*
- chip address *(12 bits, CMOS input, hardwired)*
- control input/output repeater *(t.b.d., to chain across modules)*
- *AVDD, AGND, DVDD, DGND*

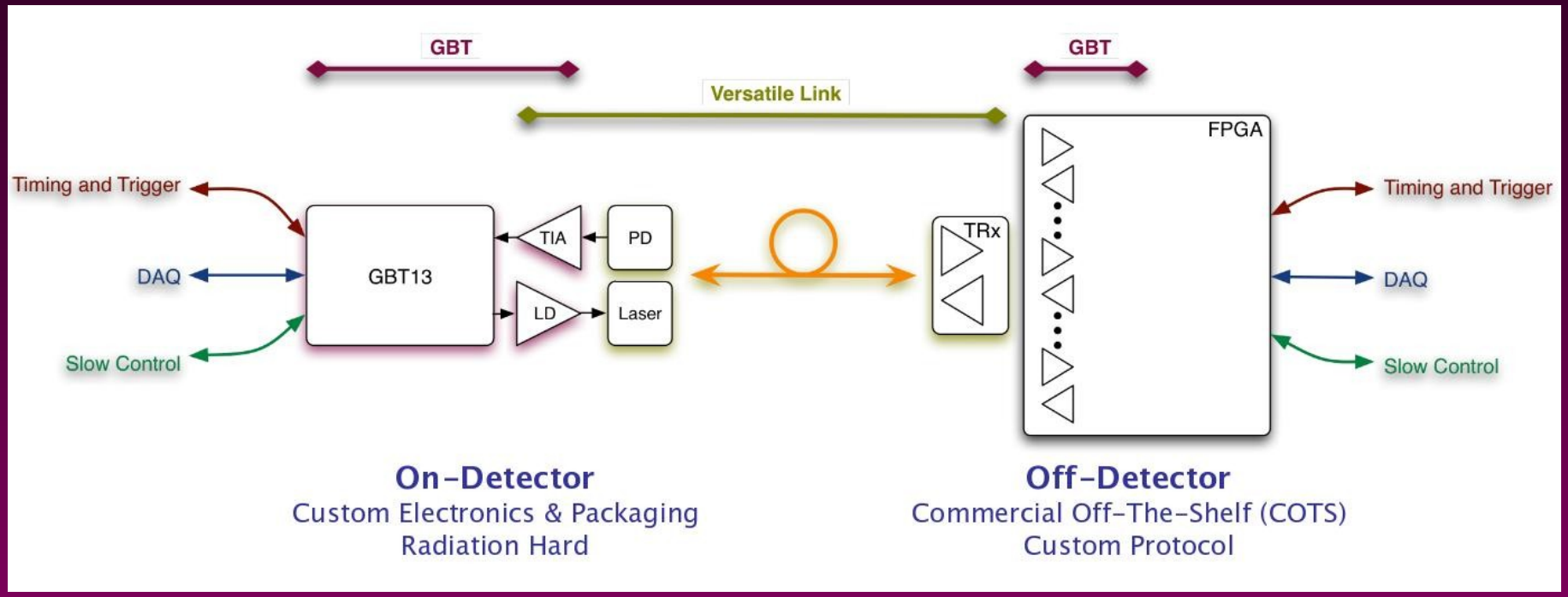
On ToPiX data rates capabilities

Sezione di Torino

	# links	Clock freq.	Event size	Rate/chip (SDR)	Rate/chip (DDR)	# pixels	Rate/px (SDR)	Rate/px (DDR)	Rate/cm^2 (SDR)	Rate/cm^2 (DDR)
		[MHz]	bits	Mev/s	Mev/s		kev/s	kev/s	Mev/s	Mev/s
ToPiX v3	1	50	32	1.43	-	640	2.23	-	22.32	-
ToPiX v4	1	50	40	1.11	2.22	640	1.74	3.47	17.36	34.72
ToPiX v4	1	160	40	3.56	7.11	640	5.56	11.11	55.56	111.11
ToPiX v5	1	160	40	4.0	8.0	12760	0.31	0.63	3.13	6.27
ToPiX v5	2	160	40	8.0	16.0	12760	0.63	1.25	6.27	12.54
ToPiX v5	3	160	40	12.0	24.0	12760	0.94	1.88	9.40	18.81
ToPiX v5	4	160	40	16.0	32.0	12760	1.25	2.51	12.54	25.08

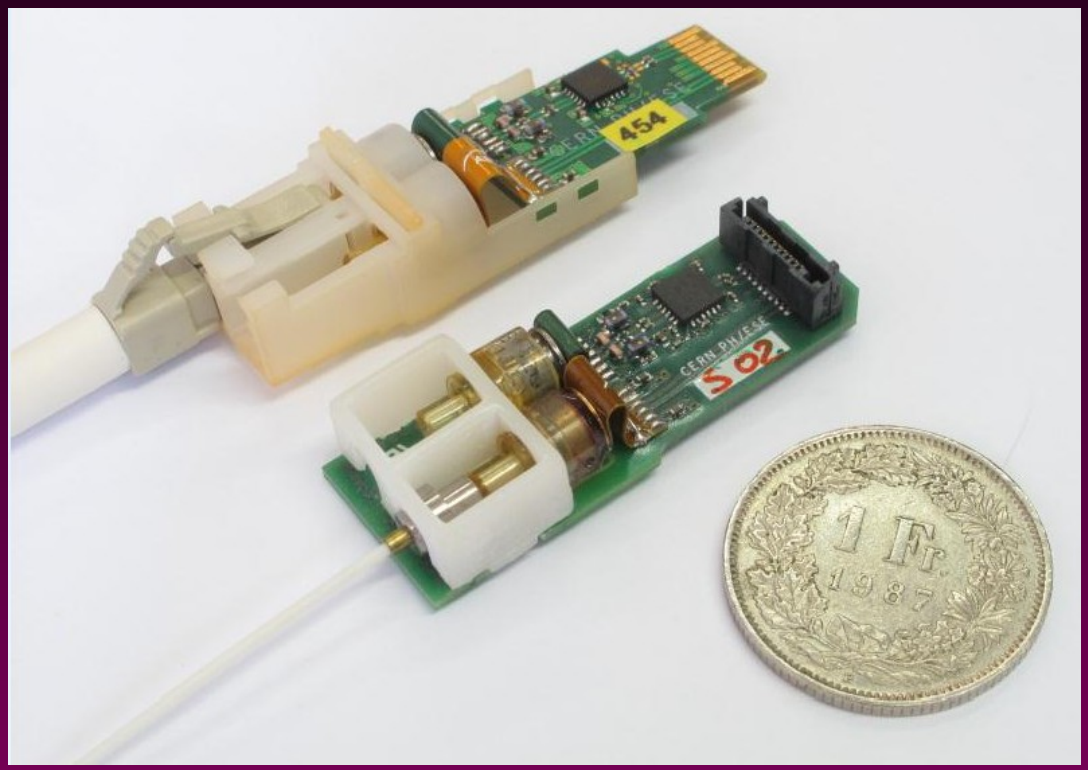
GBT

Sezione di Torino



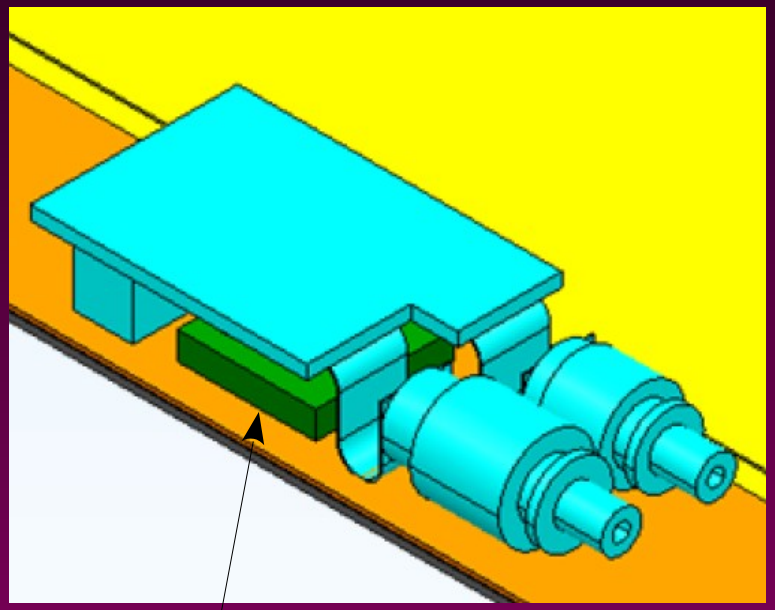
GBT components

Sezione di Torino



Versatile Transceiver
50×14×10 mm^3
45×15×8 mm^3
(F.Vasey, J.Troska, C.Soos)

Proposed arrangement for CMS tracker (C.Soos)



GBTx 10×10 mm^2
(P.Moreira et al.)

GBT status

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- GBT engineering run received from production. Tests of the first lot ongoing.
- Samples of GBTX and VTRx received in Torino
- Demo board under test @CERN.
- Started design of the MVD pixel board
- GBT-SCA code received and implemented – test ongoing, first results ok (loopback). Some limitations related to the FPGA used.

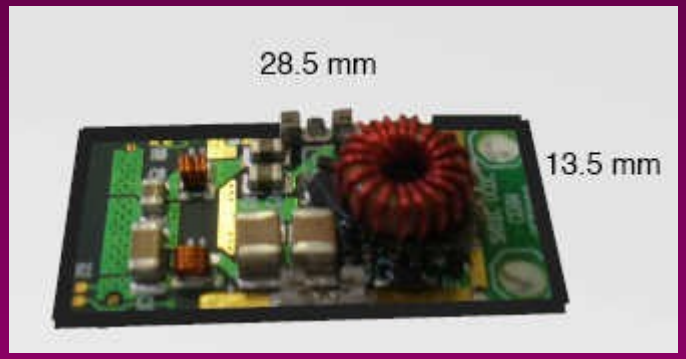
Power regulator

Sezione di Torino

- ToPiX power supply 1.2 V – I_{DC} ~ 1 A (estimated)

  → *voltage drop on cables is not negligible*

- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- Current CERN version : V_{IN} 10÷12 V, V_{OUT}=1.2÷3.3 V, I_{OUT} < 3 A
- V_{OUT}= 1.5 V, I_{OUT} < 3-4 A now avail.
- Tests with ToPiX v4 ongoing



Conclusions

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- ToPiX v4 has been received from foundry on Feb 18th 2014.
- Analog performances ok.
- Test results shows correct operation @ 160 MHz albeit column data readout is at the limit – some margin has to be added.
- TID test completed, v3 problems looks solved
- SEU tests performed, results ok (improvements in the pixel config registers are under study)
- ToPiX v5 design ongoing
- GBT chipset has completed pre-production. Samples received.
- DC-DC converters ordered.

Outlook

Sezione di Torino

- On track to have full size ToPiX ready for submission on 4th quarter 2015
- Some considerations :
  - IBM Microelectronics Division has been sold to GlobalFoundries on October 2014
  - GlobalFoundries declared it will keep the IBM processes running for at least three years (till 2017)
  - *… this does not fully guarantee that the process will not be phased out before that date*
  - ➔ If we want to have a reasonable probability to be on time, we should submit and ToPiX engineering run not later than one year from now, in order to have the production run at the end of 2016

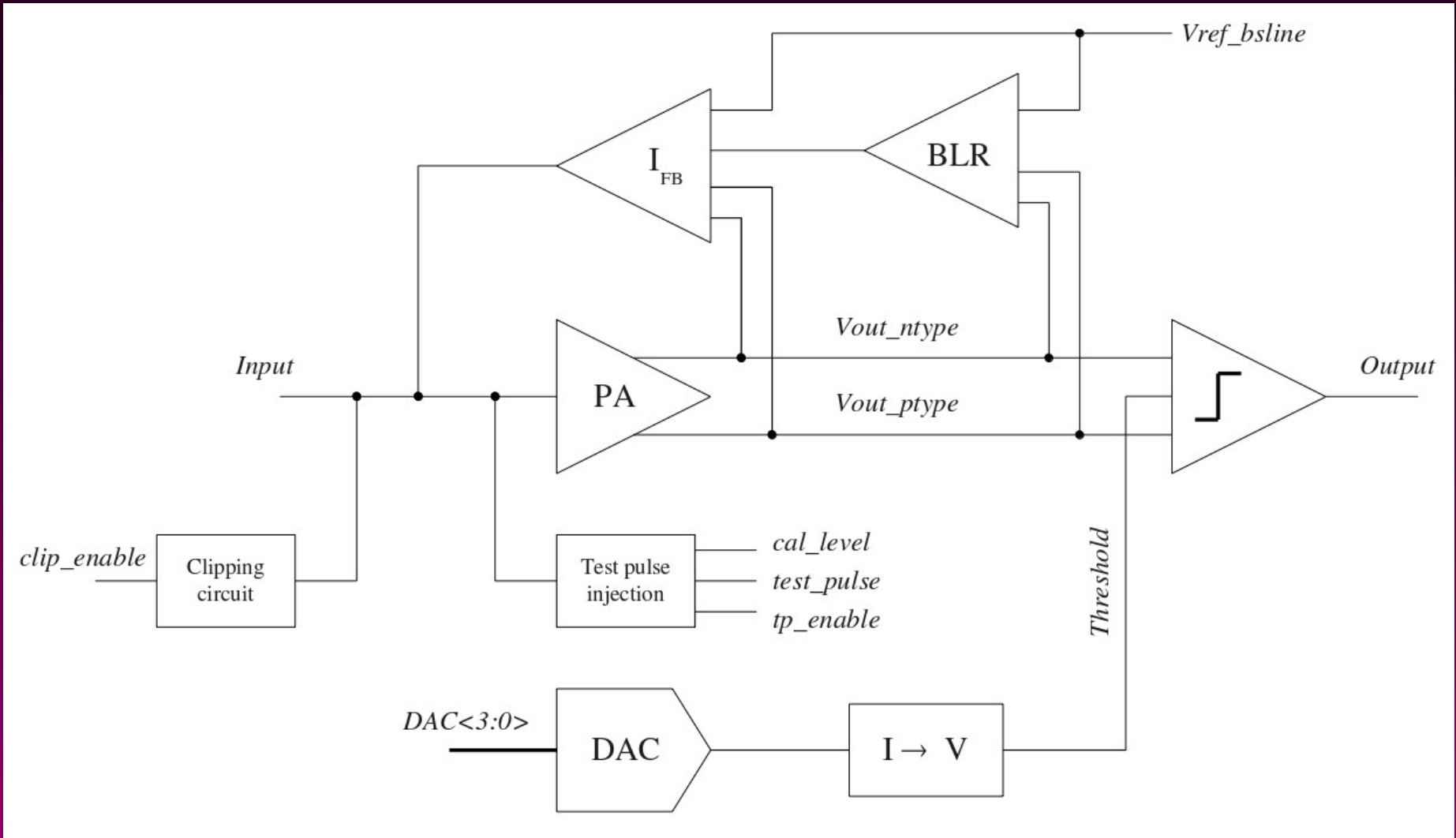
PANDA FEE_DAQT Meeting

Sezione di Torino

Backup slides

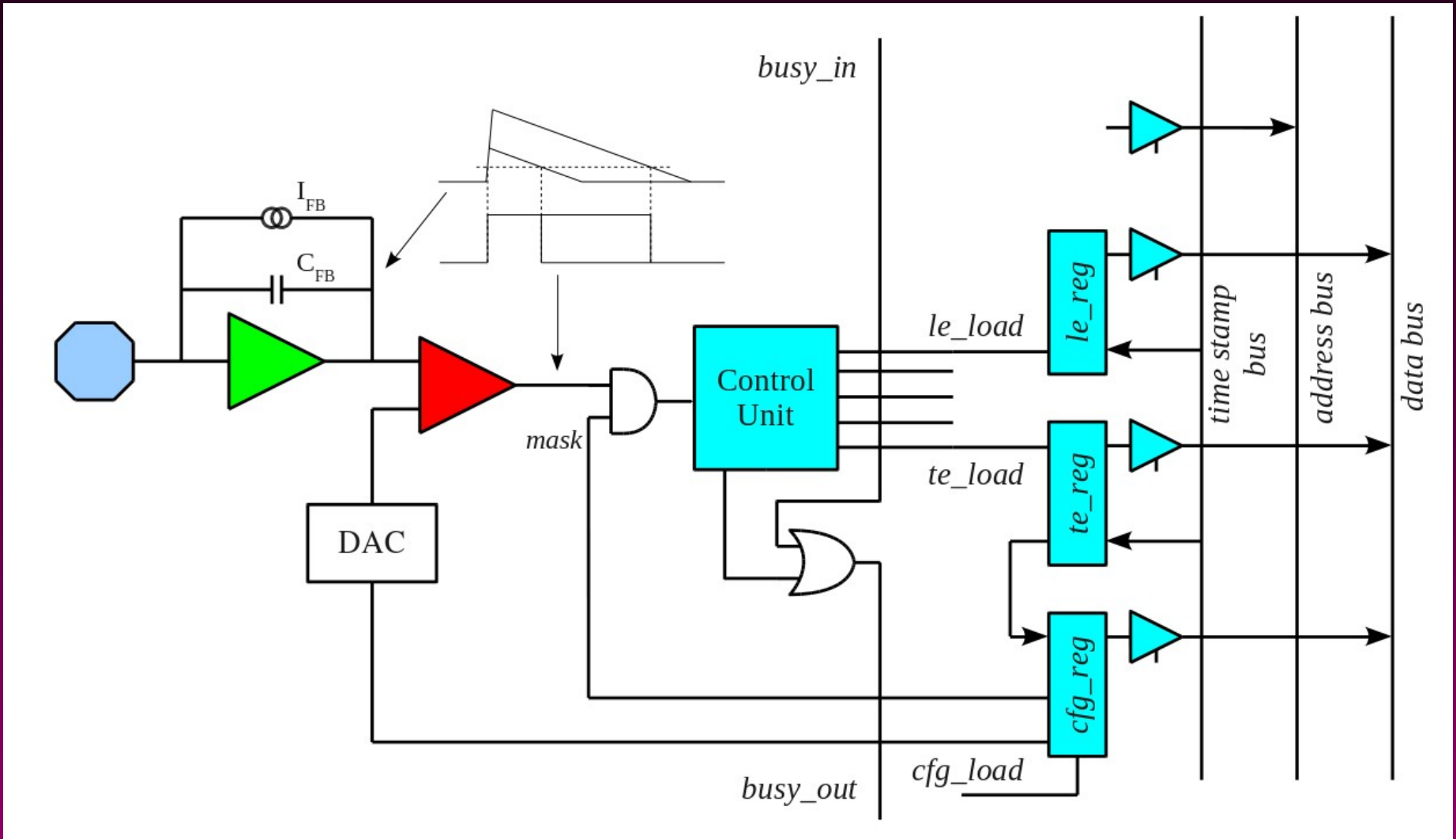
F/E schematic

Sezione di Torino

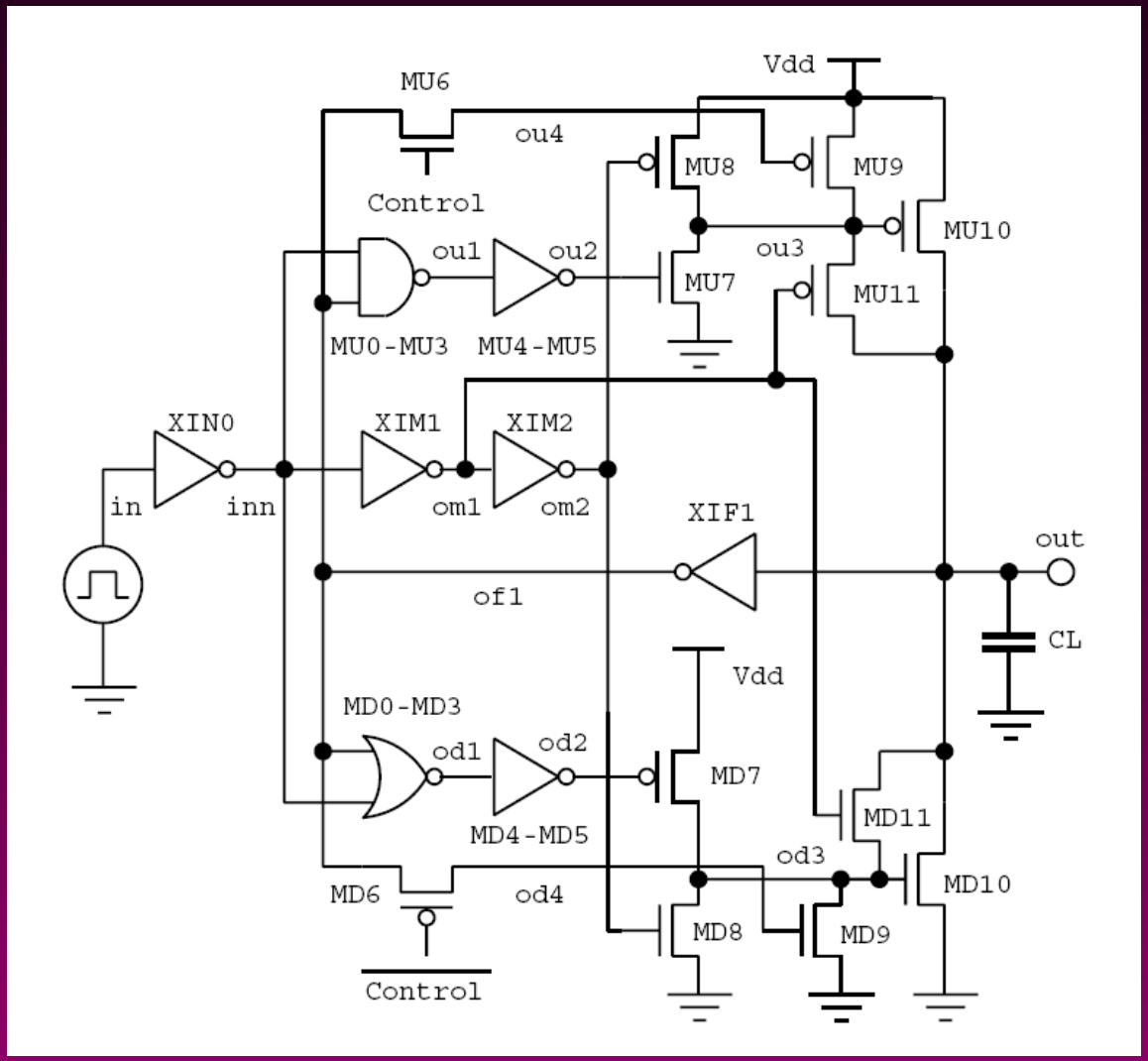


Pixel cell schematic

Sezione di Torino



Line driver



Bus capacitance : 49.9 fF/cell
Bus resistance : 9.3 Ω/cell

Provides both reduced voltage swing and pre-emphasis or full voltage swing

J.C.Garcia, J.A.Montiel, S.Nooshabadi
Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects
ISCAS 2007