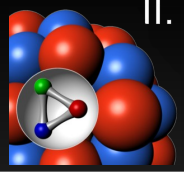

II. Physikalisches Institut

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Status of the Prototype Trigger-Less Data Acquisition

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in behalf of the $\overline{\text{P}}$ANDA Collaboration

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This work was supported in part by BMBF (05P12RGFPF), HGS-HIRe for FAIR and the LOEWE-Zentrum HIC for FAIR

Bundesministerium für Bildung und Forschung

HGS-HIRe for FAIR
Helmholtz Graduate School for Hadron and Ion Research

HIC for FAIR
Helmholtz International Center

Prototype Trigger-less Data Acquisition (PTDAQ)

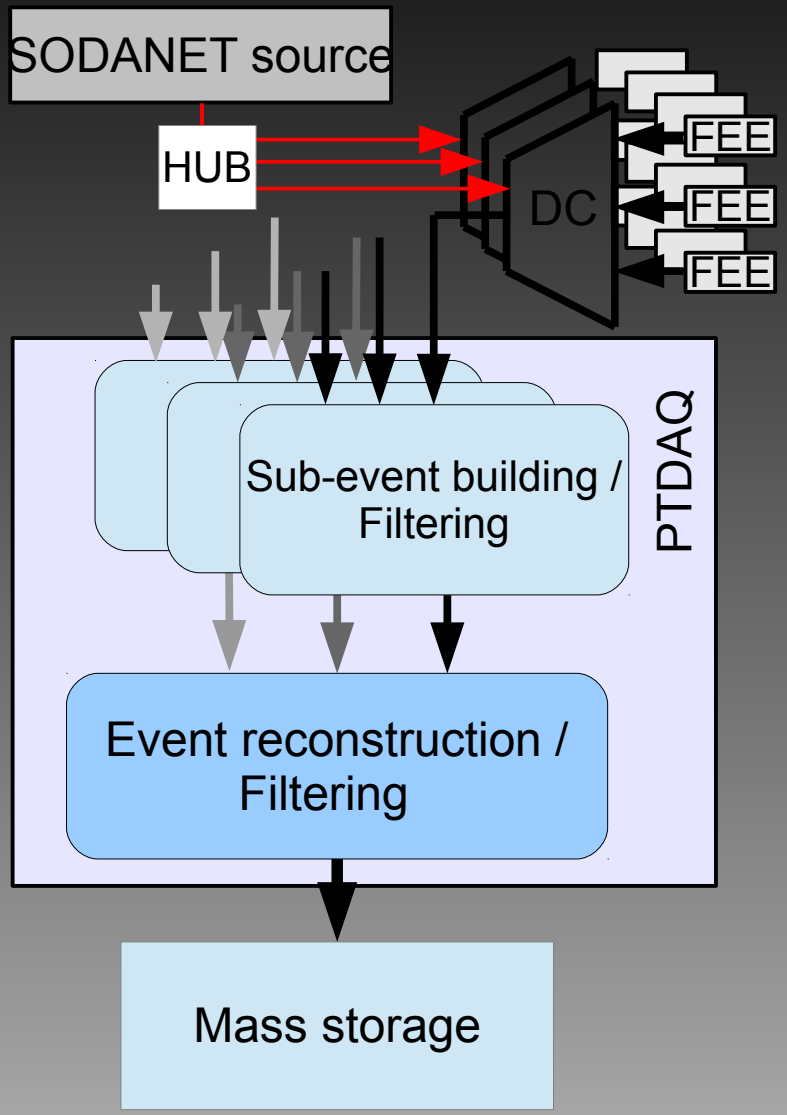
Used for testing:

- Synchronization of data acquisition (SODANET)
- Sub detector prototypes
- Reconstruction algorithms
  - Yutie Liang
    - FPGA Helix Tracking Algorithm for $\overline{\text{P}}$ANDA
- Current hardware

Differences to the $\overline{\text{P}}$ANDA DAQ:

- No connection between sub-event building boards via backplane
- Smaller interaction / data rate

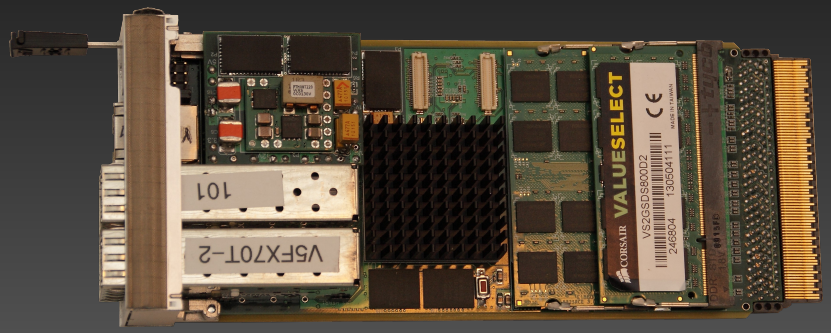
Prototype Trigger-less Data Acquisition (PTDAQ)

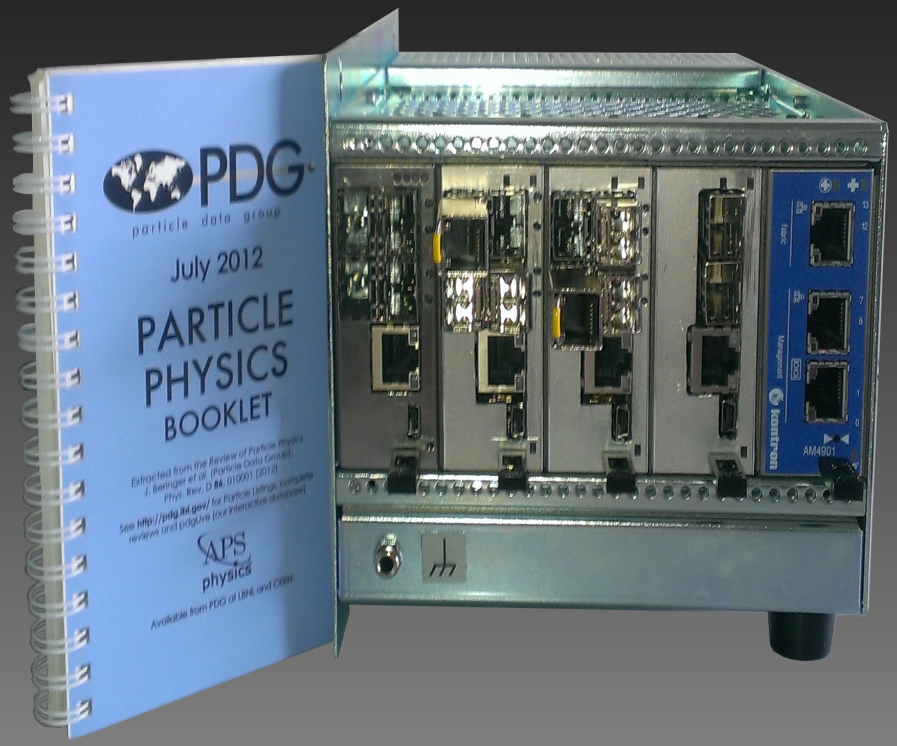


Functionality:

- Digitalized data front end electronic synchronized at data concentrator
- Sub-event building and first filter algorithm
- Event reconstruction and second stage of filter algorithm

Hardware Components





xFP board:

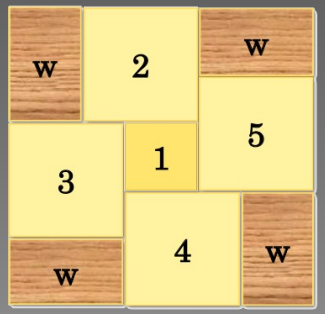
- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
  - 6.25 Gbit optical
- 1 Gb Ethernet

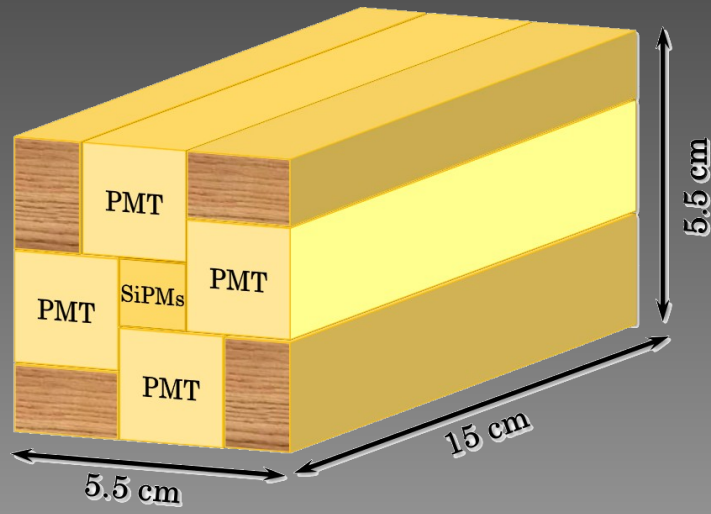
Micro TCA shelf:

- Up to 4 xFP
- Up to 9 data concentrators

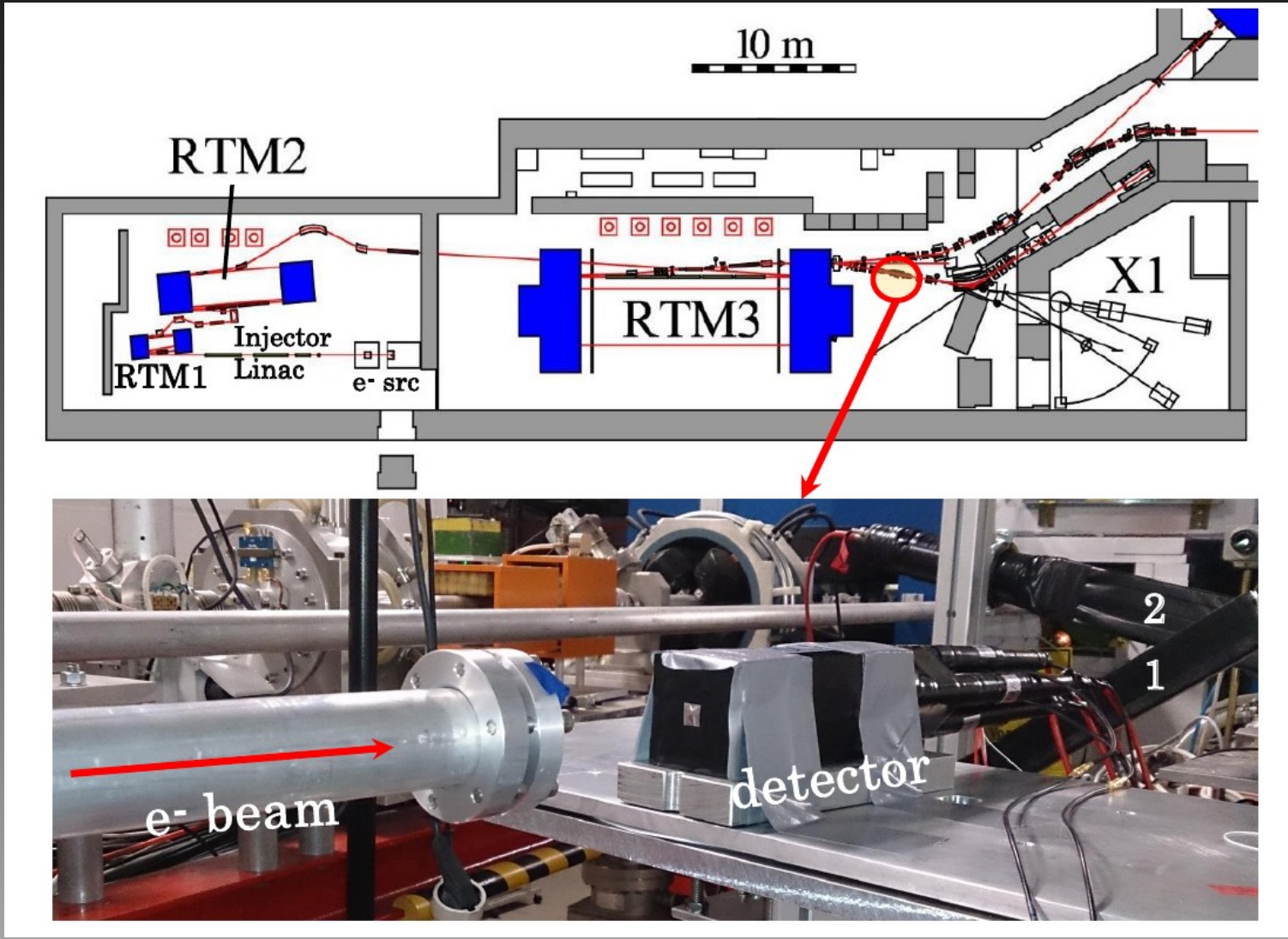
MAMI Test Setup

- Beam parameter:
  - 210 MeV electrons
  - 0.003 - 2 MHz event rate
- Detector:
  - 1 mini PWO crystal
  - 2 HAMAMATSU SI-PM
  - 4 $\overline{P}$ANDA crystals

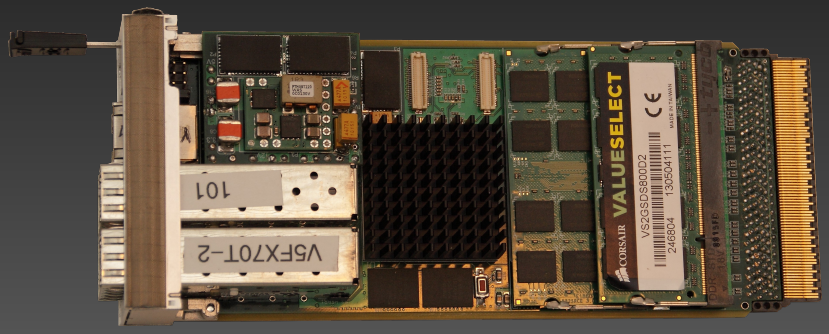




MAMI Test Location



Used Hardware



Sampling ADC (Uppsalla)

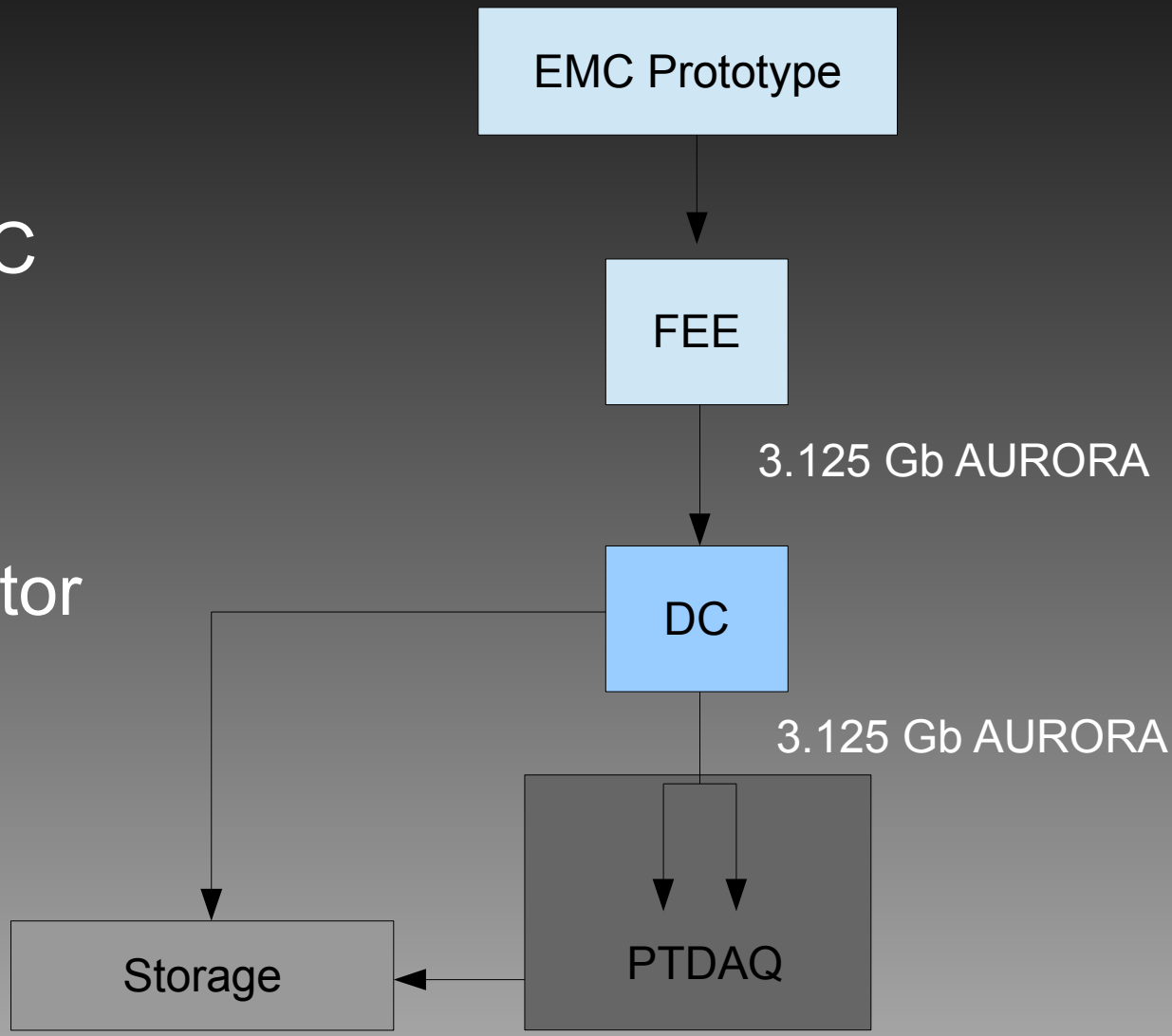
- Version 2011
- 16-ch, 14-bit
- 125 MSPS
- Virtex-5LX50

xFP board:

- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
  - 6.25 Gbit optical
- 1 Gb Ethernet

MAMI Test Setup

- DAQ chain
  - 1 Sampling ADC
  - Pile-up mode
- 1 xFP version 2
  - Data concentrator
- 1 xFP version 3
  - Burst-builder

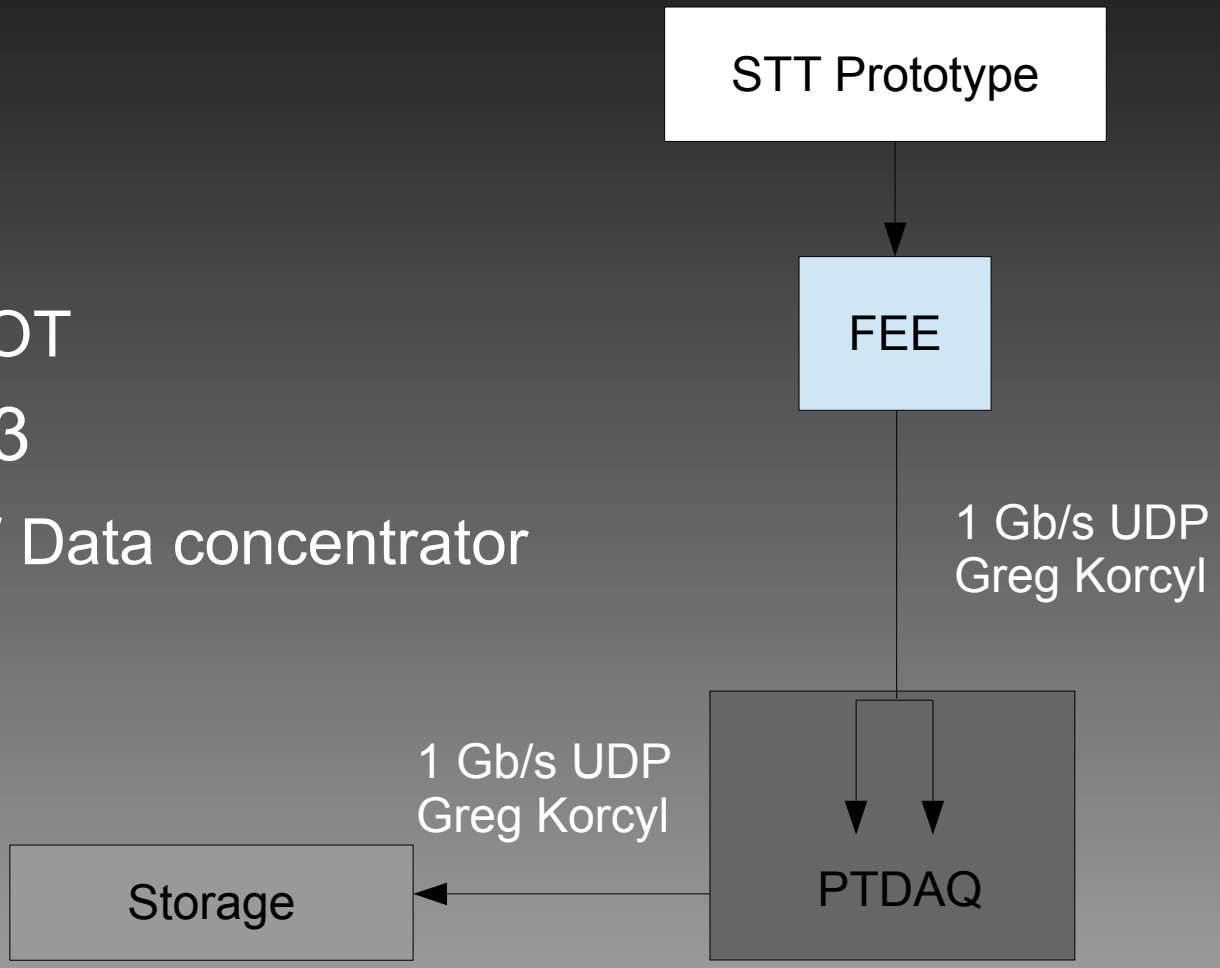


MAMI Test Results

- Stable Connection between DC and xFP
  - 2-Input burst building successful
  - For ~ 15 * 10^6 Stable events
    - Event size ~ 700 Byte
  - Data rate of ~1 Gbit/s

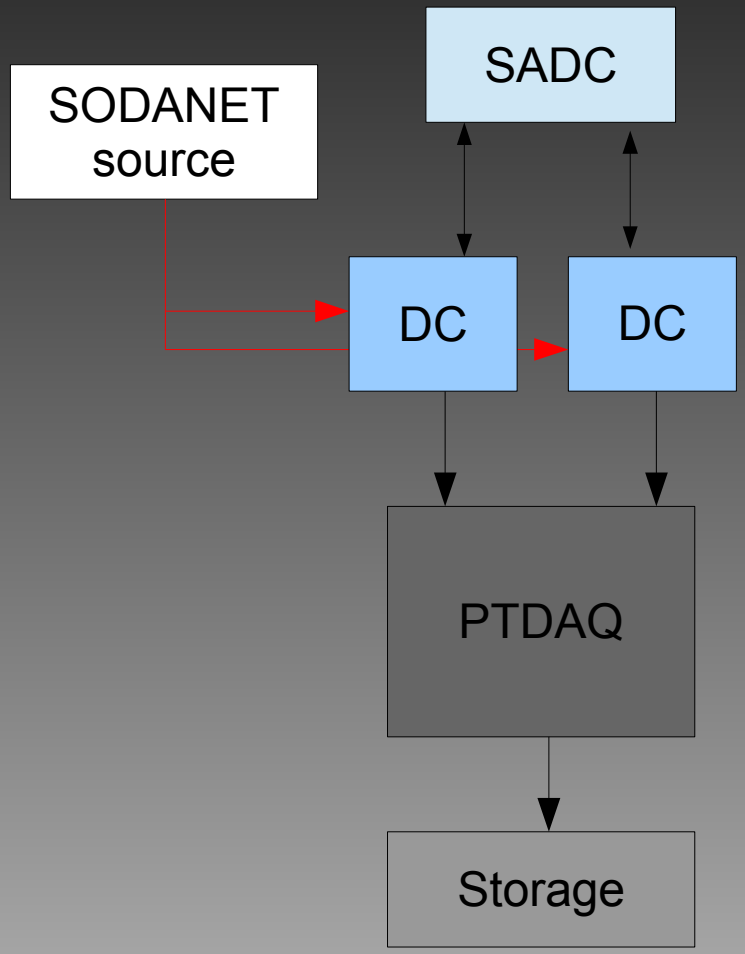
Jülich Connection Test

- DAQ chain:
  - 1 TRBv3
    - FEE board /TOT
  - 1 xFP version 3
    - Burst-builder / Data concentrator

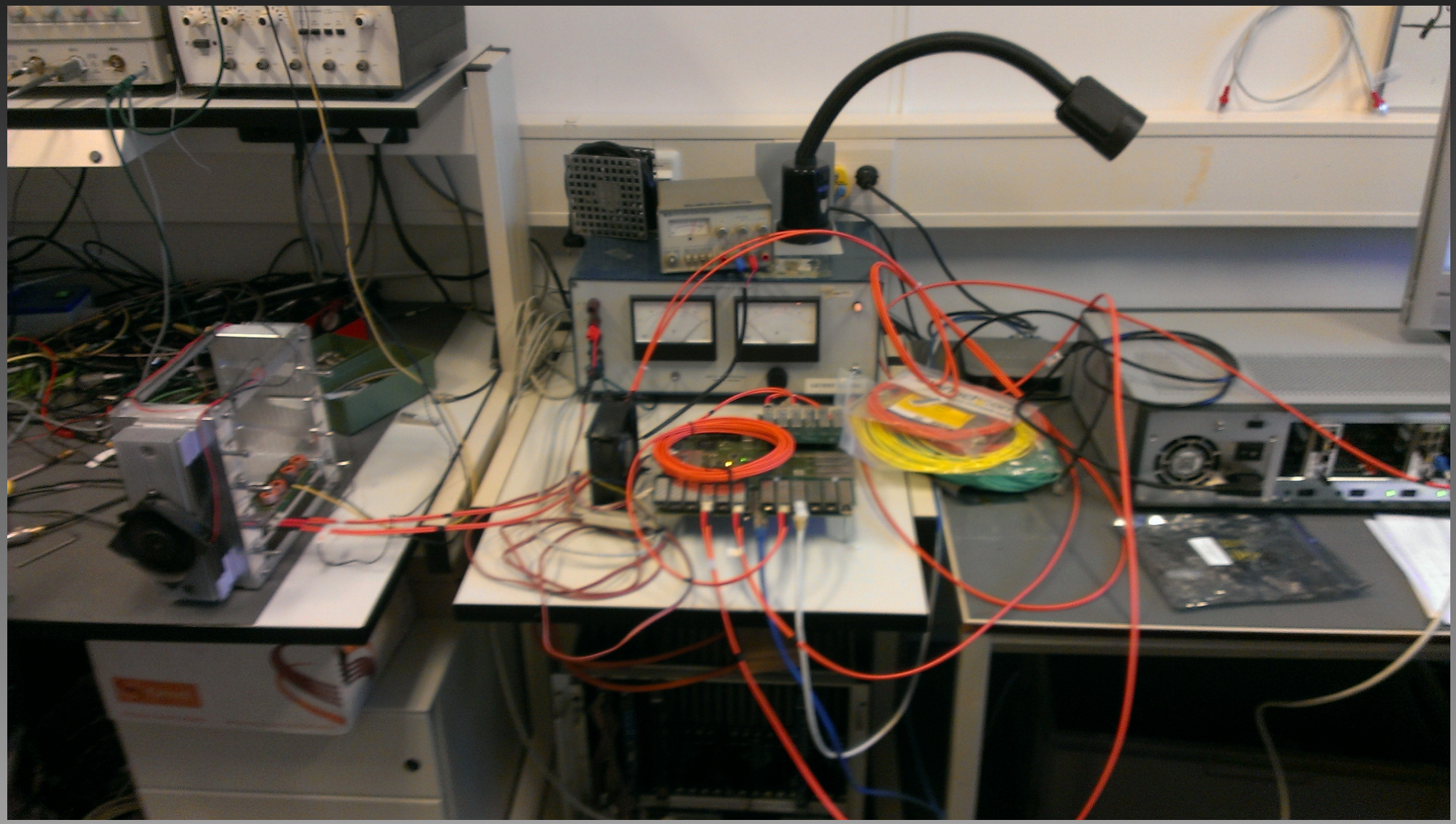


Groningen SODANEt Connection Test

- DAQ chain
  - 1 Sampling ADC (Uppsala)
  - Feature extraction mode
- 1 TRBv3
  - 2 Data concentrator
  - 1 SODAnet source
- 1 xFP version 3
  - Burst-builder



Groningen SODAnet Connection Test



Groningen SODAnet Connection Test

Sampling ADC (Uppsalla)

- Version 2012
- 32-ch, 14-bit
- 80 MSPS
- Virtex-6

Results

Stable Connection between TRBv3 and xFP using SODANET

- Stable Connection without burst building
  - Several 100 * 10^6 events
  - Data rates between
    - 0.5 to 10 MB/s
- 2-Input burst building successful
- 1 * 10^6 Stable events
  - Event size ~ 60 Byte
- Data rate of ~ 0.5 Mbit/s

Summary & Outlook

- Tested freely streaming data
  - In beam environment
  - different types of DC
- Tested SODANET Connection

Summary & Outlook

- Permanent readout setup @ Gießen
  - Proto 60
  - SADC
  - SODANET
  - DC
  - PTDAQ
- Participating in different in beam measurements
- Testing reconstructing algorithm
- Increasing the setup of the PTDAQ

Backup

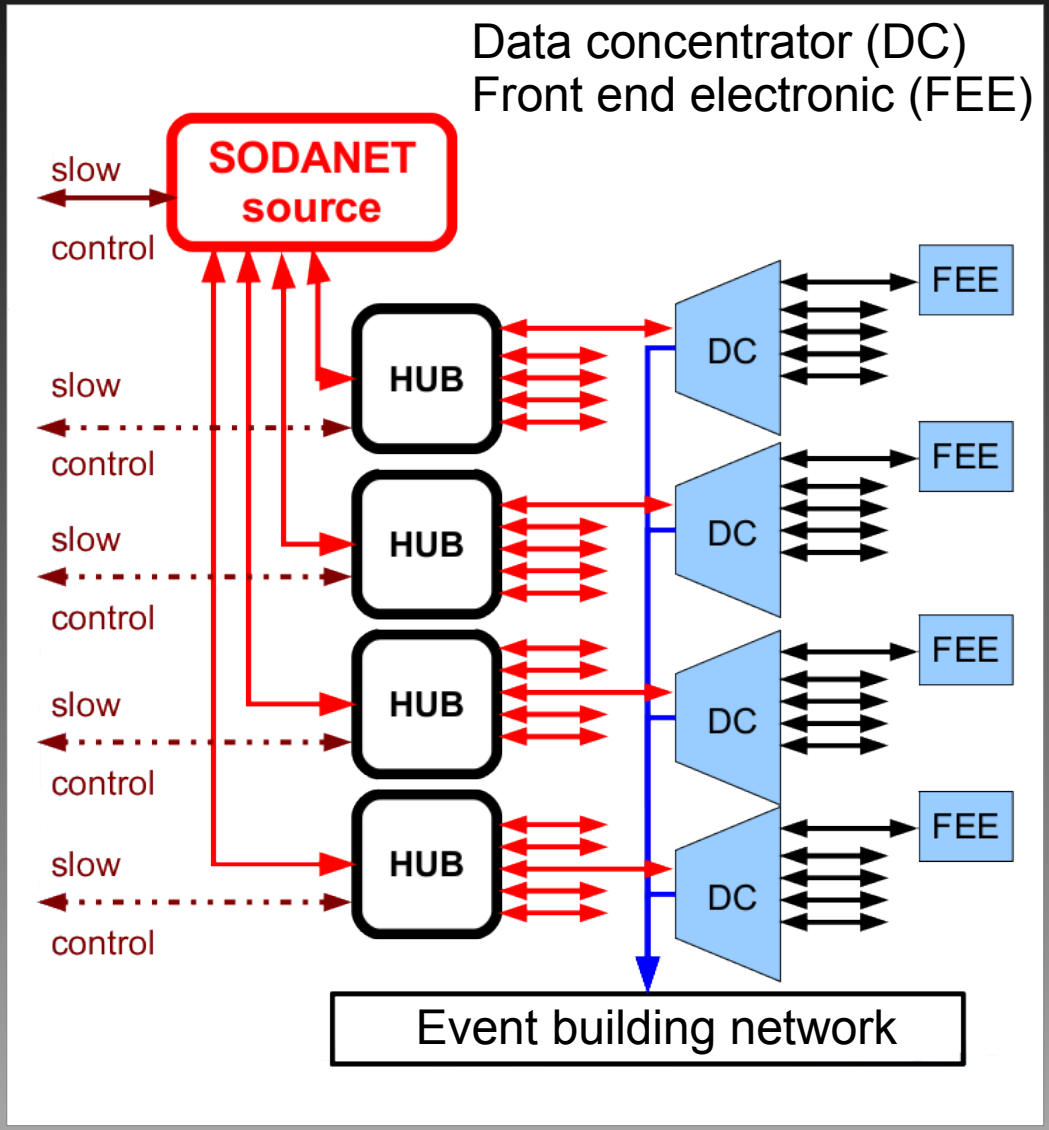
Synchronization of Data Acquisition

Functionality:

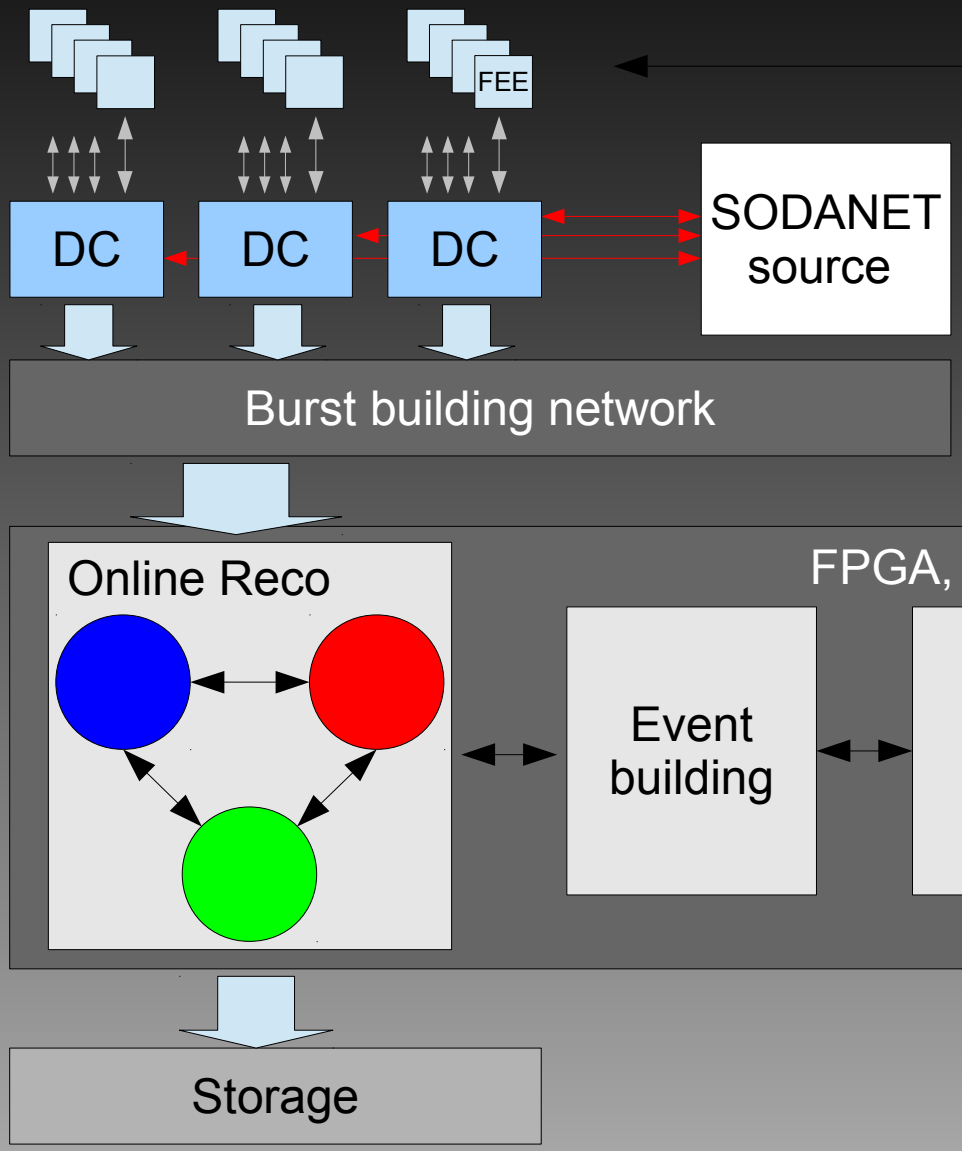
- Distribution of clock
  - Time stamp
- Distribution of synchronization commands
  - Start, stop, calibration
- Signal distributed over optical fiber
- Measurement of a signal propagation time
- Distribution of detector configuration data
- Slow control

SODANET link:

- Bidirectional
  - Source → data concentrator:
    - Synchronization
    - Front end electronic configuration
  - Data concentrator → source:
    - Slow control, used for time calibration



The PANDA DAQ



Autonomous FEE
Freely streaming data

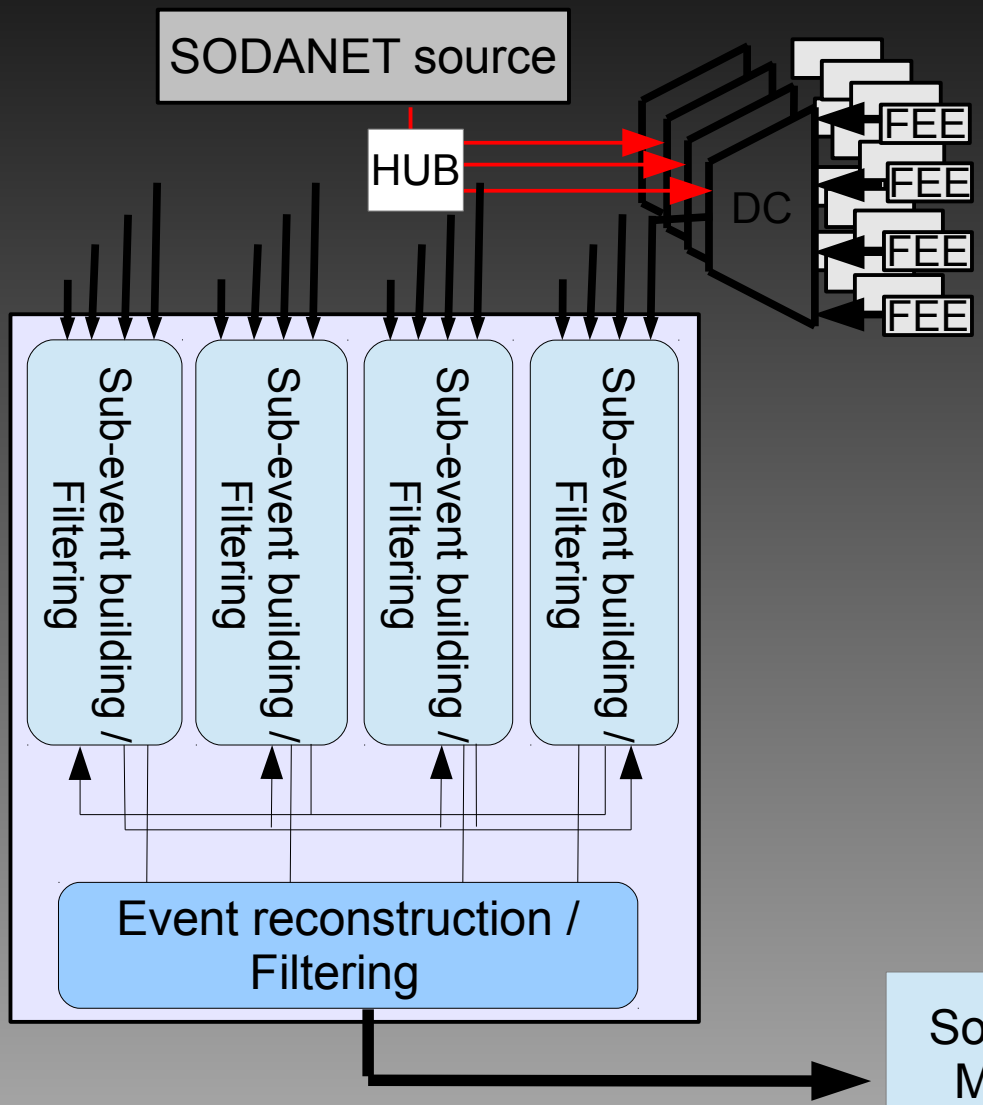
Synchronization
Feature extraction

Burs building
Partly reconstruction

Full reconstruction
- Tracking
- PID
- Neutral reconstruction

Event building
Event filtering (based on physics)

Data concentrator (DC)
Front end electronic (FEE)



- VHDL code can be used without many changes
- Increased number of inputs per sub-detector
- Increase the possible data rate
- High performance event reconstruction
- High level event filtering
  - Software trigger on a sever farm or GPUs

The PANDA DAQ

- Freely streaming data :“Trigger - less”
- No hardware triggers
- Event filtering
- Autonomous FEE, sampling ADCs with local feature extraction
- Time-stamping (SODA)
- Data fragments can be correlated for event building
- Caveat: the high-rate capability implies overlapping events !!!
- average time between two events can be smaller than typical detector timescales
- This “pile-up” has to be treated and disentangled
- Real-time event selection in this environment is very challenging and requires a lot of studies

Status &Outlook

Status:

- One board setup
  - Connection for of up to 4 DCs
  - Tested with simulated DCs

Outlook

- Tests with different types of DCs
- Test different kinds of detectors with beam
- Upgrade to ATCA based Compute Node DAQ using carrier boards and xTCA compliant boards