# Some new thoughts for future CN development and PANDA DAQT structure

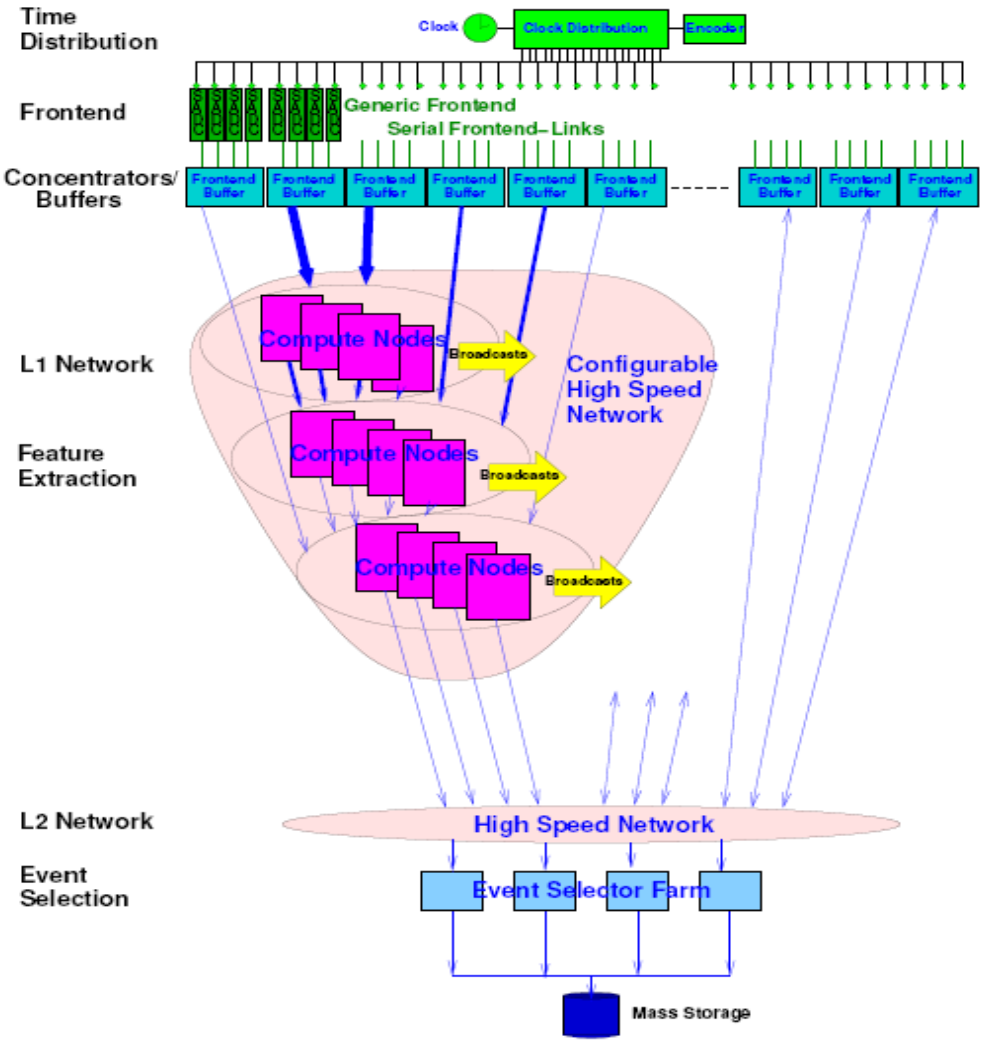
Zhen-An LIU
TrigLab IHEP Beijing
For PANDA DAQT Workshop
GSI Germany
Apr. 9-10 2015

# Outline

- Brief Review on CN Development
- Discussion
- Some new thoughts
- Summary

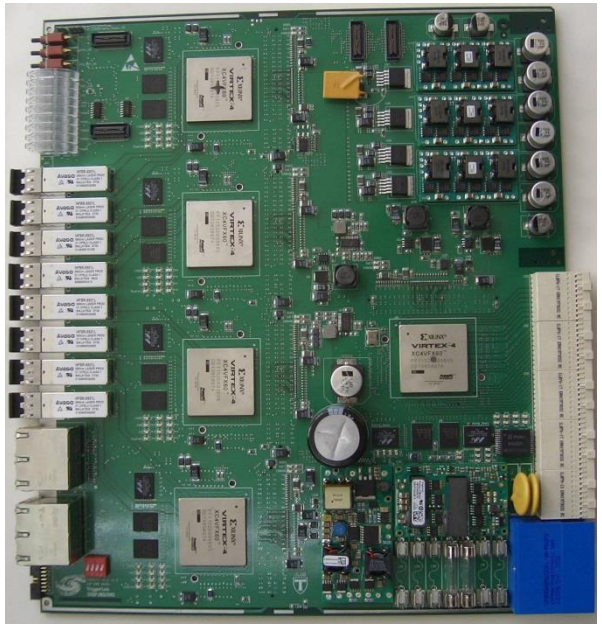
# Brief Review on CN Development

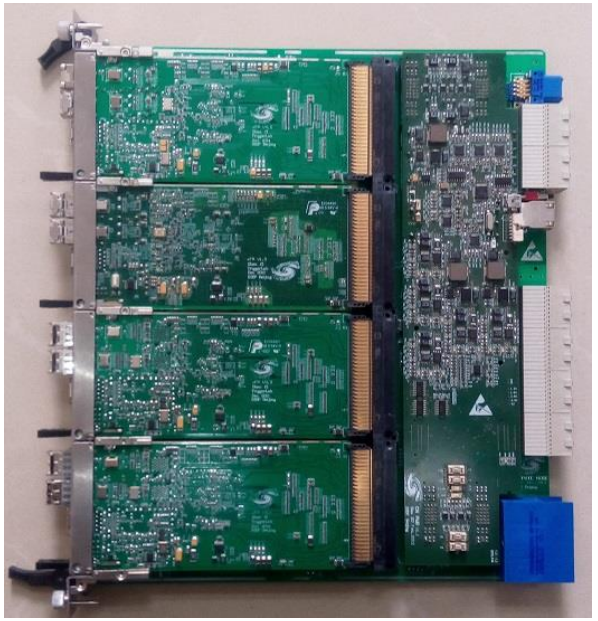
- Structure of PAND/ overall system
  - Compute Node(CN
    - Key modude
    - For Trigger and
    - DAQ
  - ATCA compliant



# Brief Review on CN Development

- CN Development summary
  - 3 main versions has been developed
    - V1, fixed transvers
    - V2, Transcivers Pluggable, SFP
    - V3, Processor Pluggers also
  - Some of them has been used in PANDA collaborators





# Discussion

- Should the latest version be OK for use?
  - Xilinx V4 FPGA is rather old
- Some further necessary modification?
  - ATCA to MTCA?
- Wolfgang and me we have some discussions on this

# Some ideas

- Long term further development in case the project schedule is allowed?
  - V4 on the Carrier Board should be replaced by V5 or K5?
  - V5 should be replaced also by V5 or K5?
  - More channels for xFP with 12 ch MiniPOD transceivers?
- Move from ATCA to MTCA?
  - Double width AMC card as CN processor?
  - Patch Panel for interconnections

# Summary

- 3 versions of CN have been development for PANDA DAQT.
- Further verification with real software will be helpful
- Some further idea raised for discussion in the collaboration.