GBT-FPGA implementation

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GBT

- What is GBT?
  - GBT is a radiation-tolerant chip designed by CERN
  - It provides a 4.8 Gbps link with different encoding options, which makes it possible to use one kind of a link for different purposes

GBT-FPGA overview

- GBT-FPGA is implementation of GBT designed for Xilinx & Altera FPGAs
- The VHDL implementation abstracts all architectural differences between FPGAs:
  - clocking architecture
  - transceiver capabilities
  - small differences still remain (e.g. number of channel per transceiver)

GBT-FPGA banks

- "Bank" is a module that covers one transceiver:
  - provides multiple links (4 per bank in Xilinx, 3 in Altera FPGAs)
  - includes all support logic – PLLs, alignment, buffers etc.
  - user can instantiate many banks via configuration file, maximum number is device-dependent

GBT link

- "Link" is a single channel in a bank
- Each link can have different configuration:
  - data encoding & frame format
  - standard or latency-optimised

GBT-FPGA Link TX & RX paths

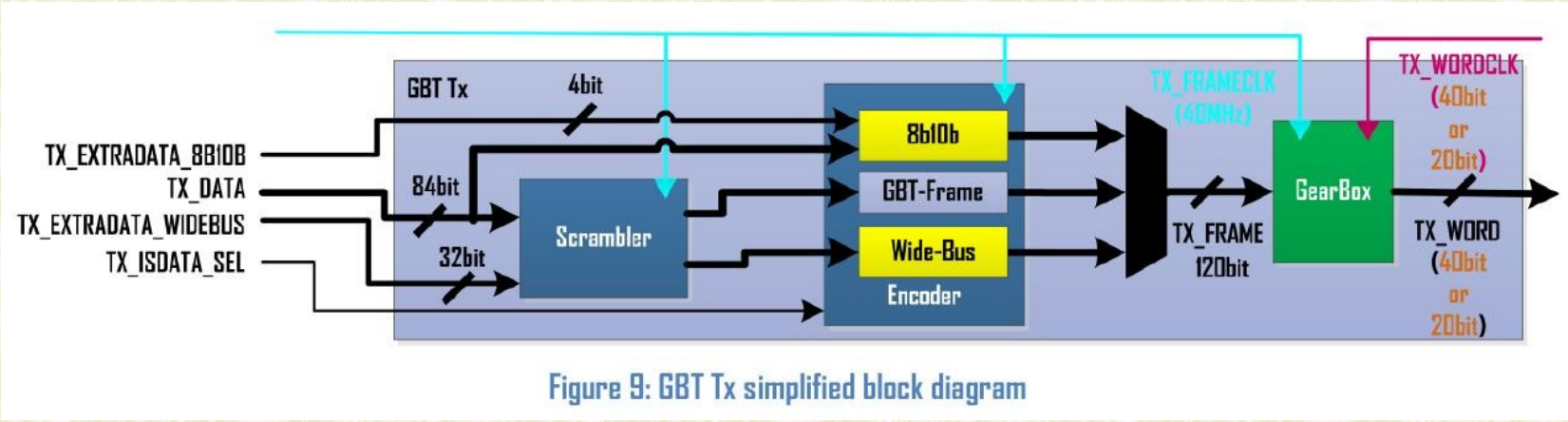


Figure 9: GBT Tx simplified block diagram

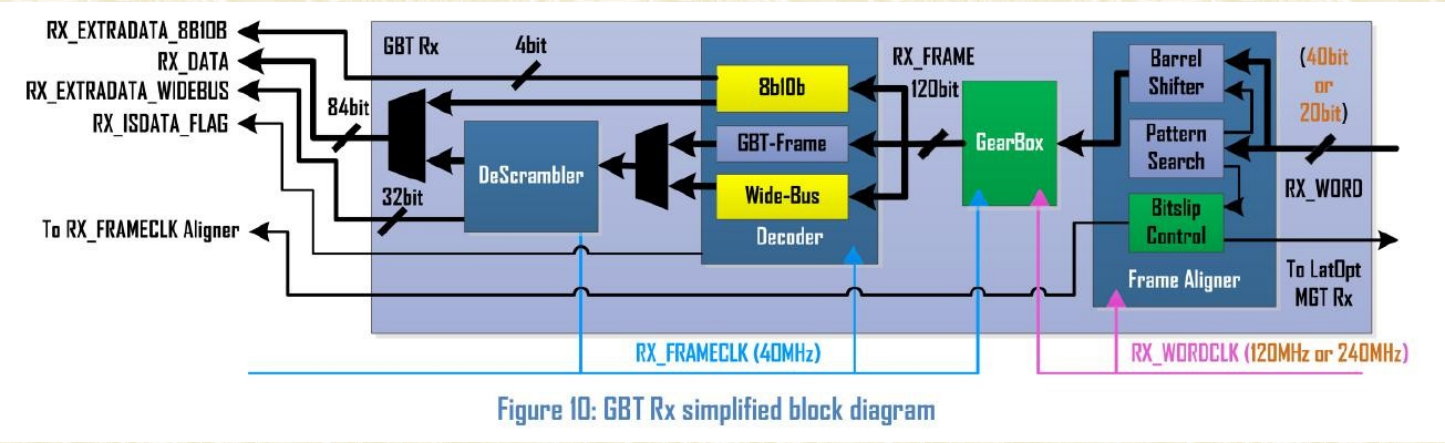


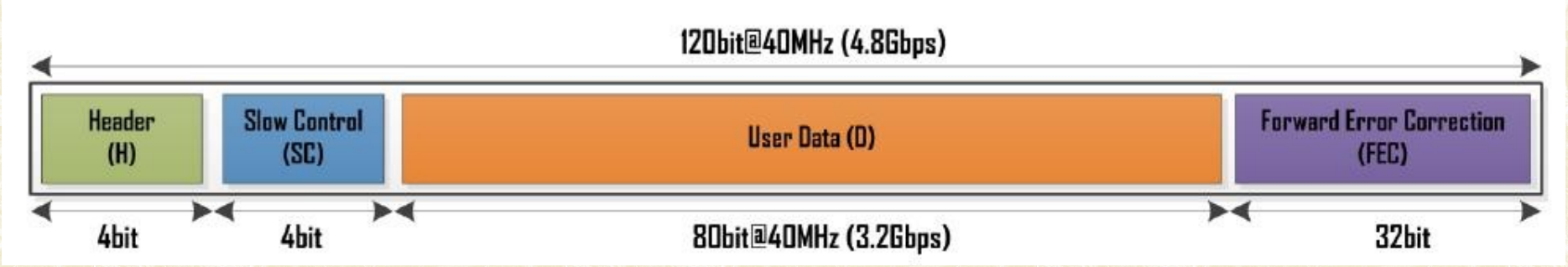
Figure 10: GBT Rx simplified block diagram

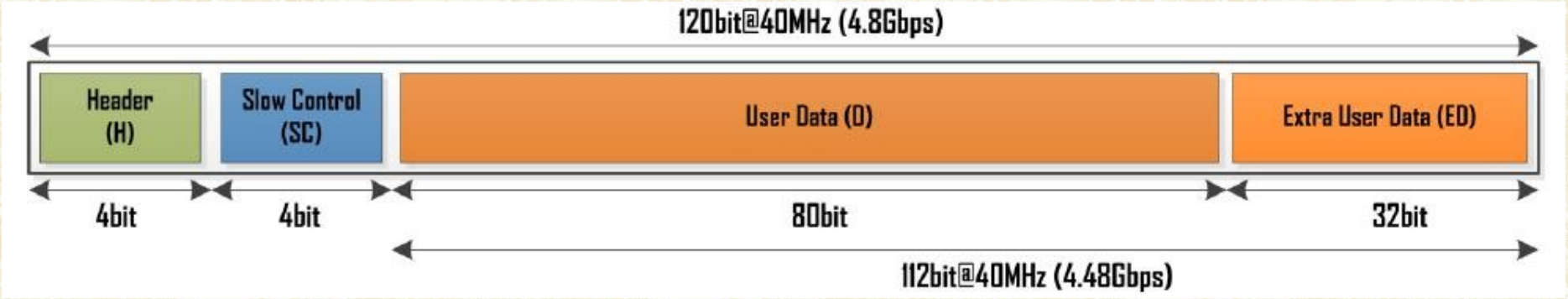
(figures taken from GBT-FPGA User Manual)

GBT-FPGA encodings

- Encoding selection dictates frame format & data throughput
- FPGA implementation supports two encodings:
  - GBT-Frame: 3.2 Gbps, Forward Error Correction, downlink & uplink
  - Wide-bus: 4.48 Gbps, no FEC, uplink only

GBT-FPGA encodings





(figures taken from GBT-FPGA User Manual)

Latency modes

- Each link can be configured in "standard" or latency optimised mode
- Standard mode uses FIFOs for clock domain crossing, which allows for asynchronous clocking
- Latency-optimised mode provides deterministic latency, but puts more constraints on clocking infrastructer. Either both sides need to have common clock source, or one side has to use RX recovered clock
- Ability to work with recovered clock allows distribution of system clock within downlink data stream

IP cores, VHDL code

- The GBT-FPGA design is very well written and doesn't depend on proprietary IP cores too much
- Vendor-dependent IP-cores include BRAM components & debugging facilities
- SVN code includes example projects for selected boards (e.g. KC705 Kintex 7 development board)

Porting the code to Vivado & AFCK

- Original project worked only with Xilinx ISE, project was ported to Vivado
- All changes were sent upstream to Sophie Baron from CERN
- Project was also ported to AFCK

Thank you for your attention!