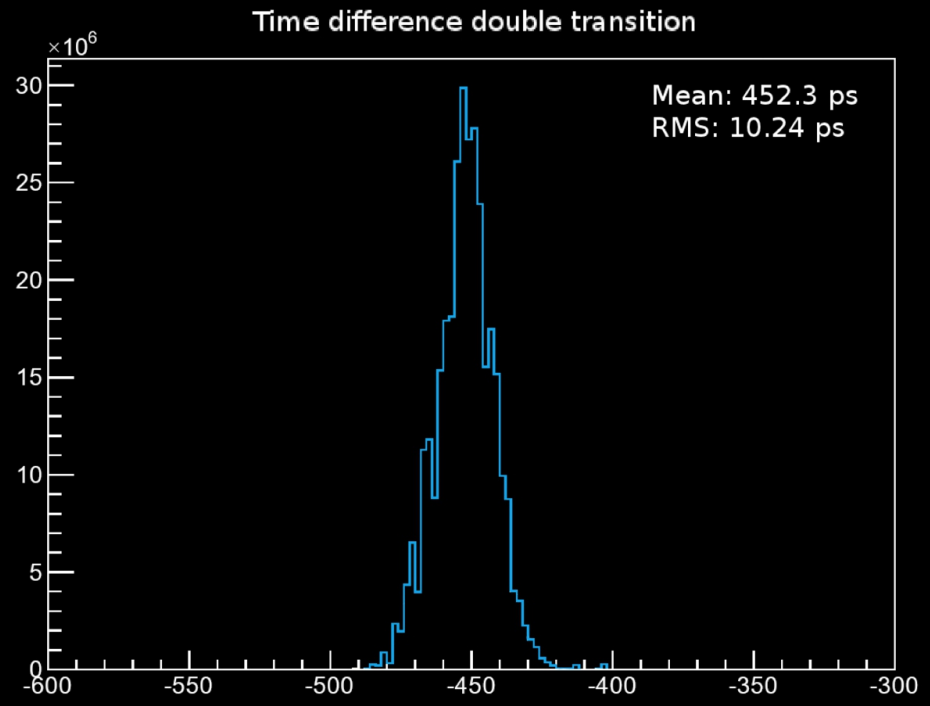
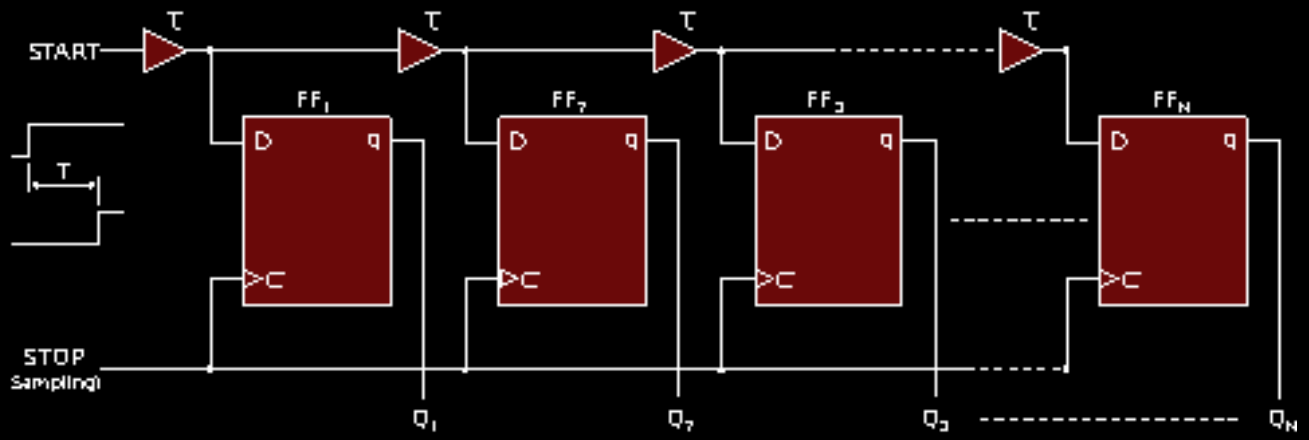
A low-accuracy TDC?

TDC Performance

- even without calibration not worse than 50 ps
- some systems need less performance:
  - MDC: 500ps
  - STT: 300ps
  - RICH: 100ps

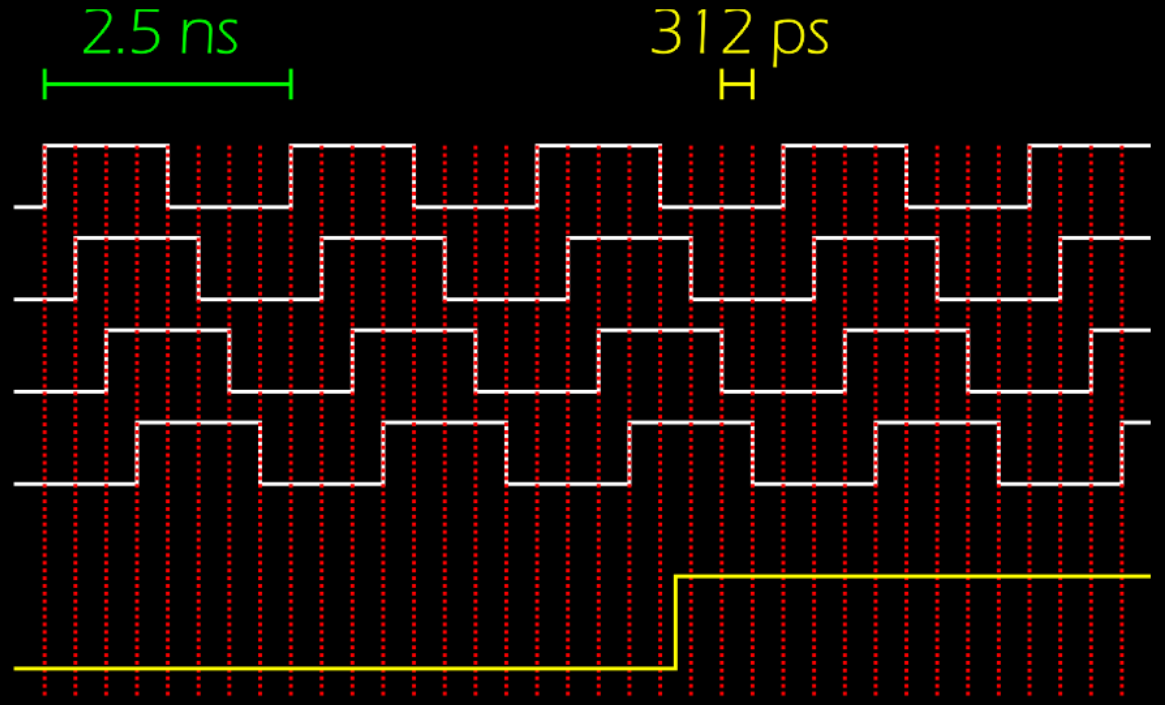




Low-cost FPGA TDC

- Sampling with phase shifted clocks
  - e.g. 400 MHz
  - sampling with rising/falling edge
  - 4 clocks shifted by 90°

  → 312 ps binning
- many channels, only limited by I/O (110/220 on Trb3sc)
- technique proven by many people



First Tests

- Using a MachXO2 FPGA
  - matching PLL structure (same as ECP 5, better than ECP3)
  - but slow fabric & large clock skew
  - at 266 MHz internal RC oscillator (500ps mean bins)
  - only basic floorplanning
- measured bin sizes
  - 590, 200, 1010, 310, 410, 180, 580, 700 (ps)
  - not perfect, but there is place for improvement...

To Do

- Research & Development needed
  - advanced VHDL programmer who wants to dive into non-standard FPGA usage & dig through tools and documentation on internal architecture