FPGA-TDC
Status and Plans

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Joint CBM / Panda DAQ Developments
"Kick-off" Meeting
19-20 February 2015, GSI

Jagiellonian University in Kraków

GSI

Johannes Gutenberg Universität Mainz

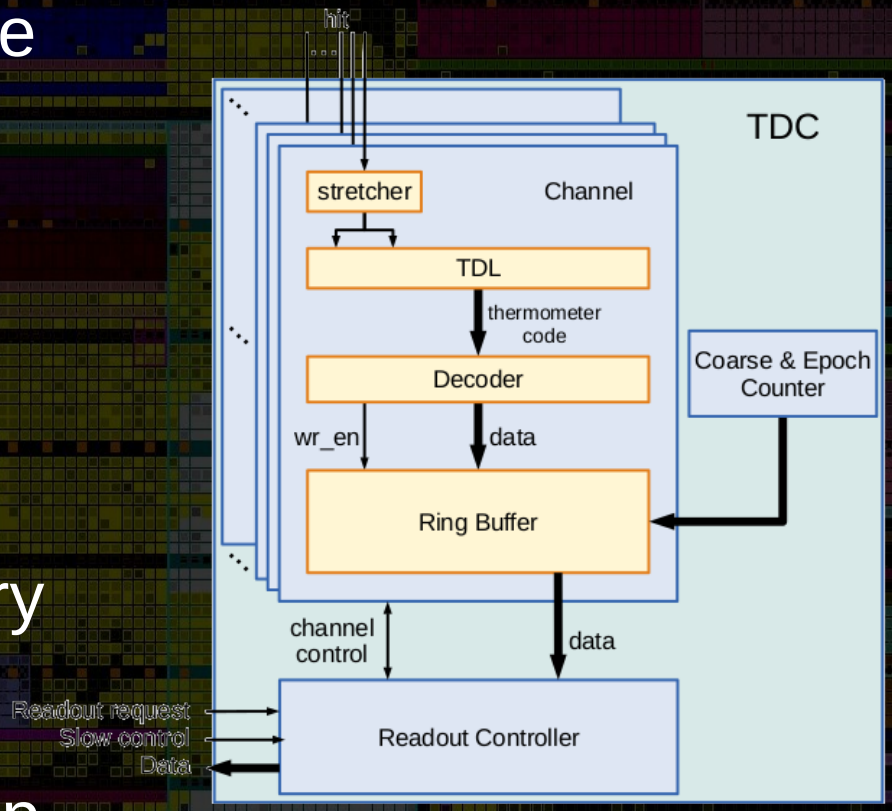
Goethe Universität Frankfurt am Main

- Outline

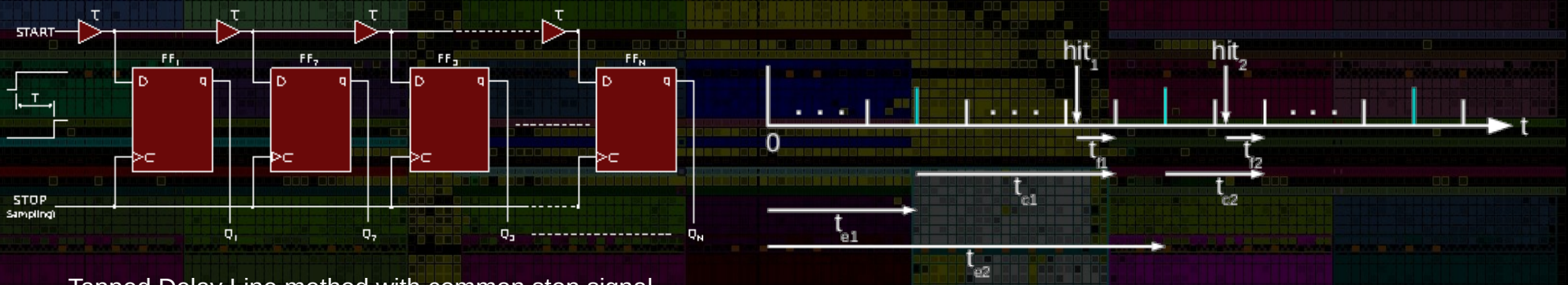
- TDC status – Single/Double Edge Measurements
- Applications
- Future Plans

- Conclusion & Outlook

- Tapped Delay Line for fine time interpolator
- Coarse & Epoch counters for long measurement range
- Stretcher for short pulses & double edge
- Decoder: thermocode → binary
- Ring buffer
- Calibration hits from an on-chip oscillator

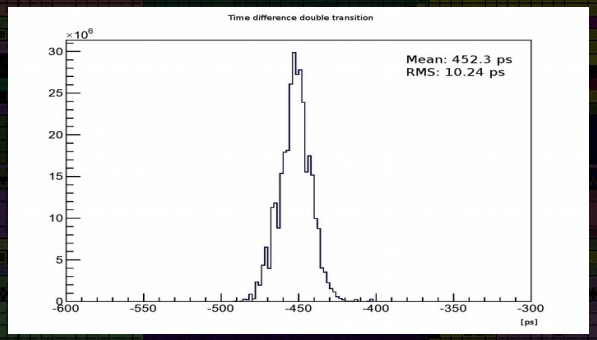


Simplified architecture of the TDC

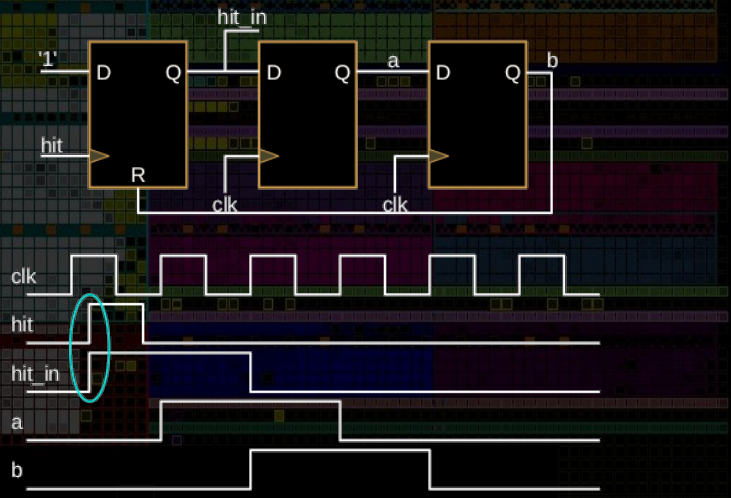


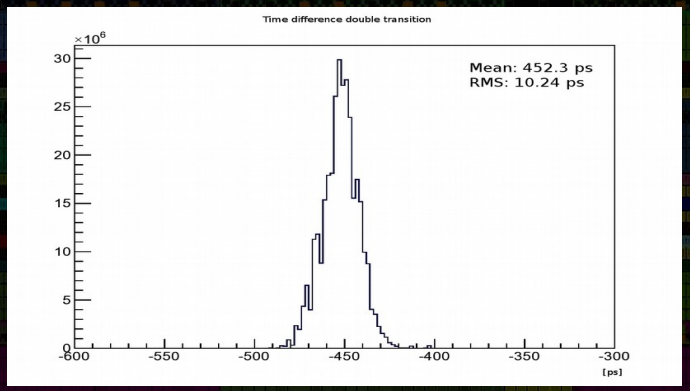
Tapped Delay Line method with common stop signal

- $\Delta t = (t_{e2} + t_{c2} - t_{f2}) - (t_{e1} + t_{c1} - t_{f1})$
- RMS measured on two channel: ~10 ps
- Stretcher for short pulses (~500 ps)



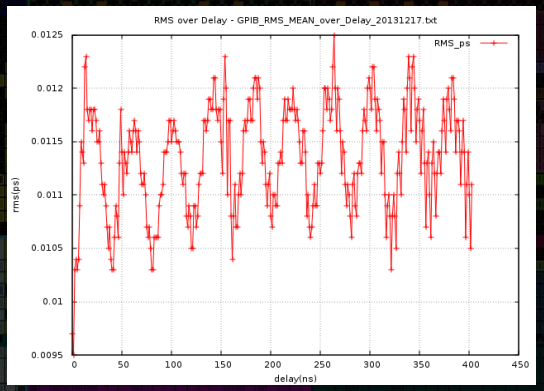
Time precision test



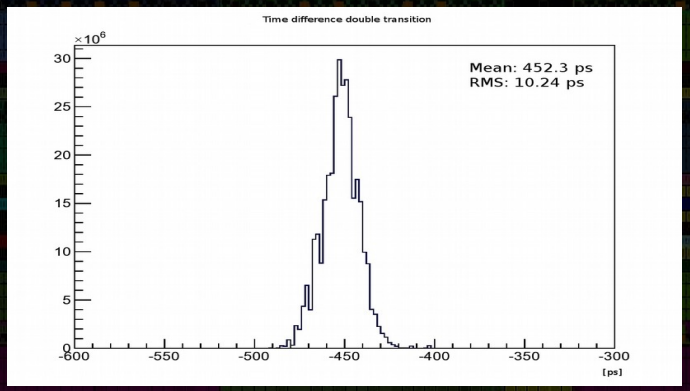


Time precision - ToF

Single edge measurement
RMS ~10 ps
ΔRMS < 3 ps



Precision vs mean



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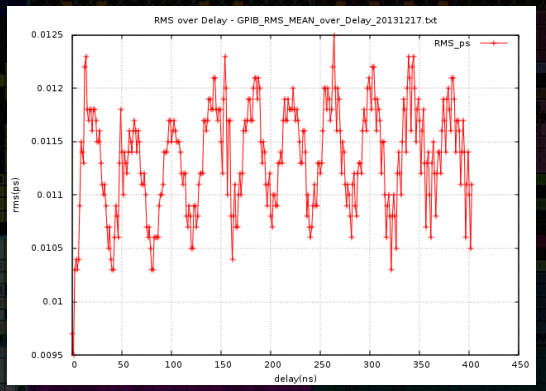
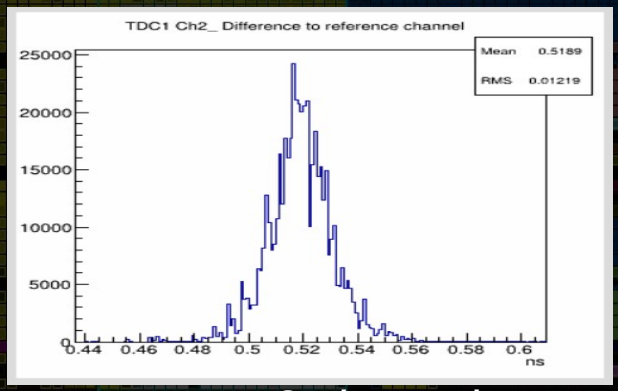
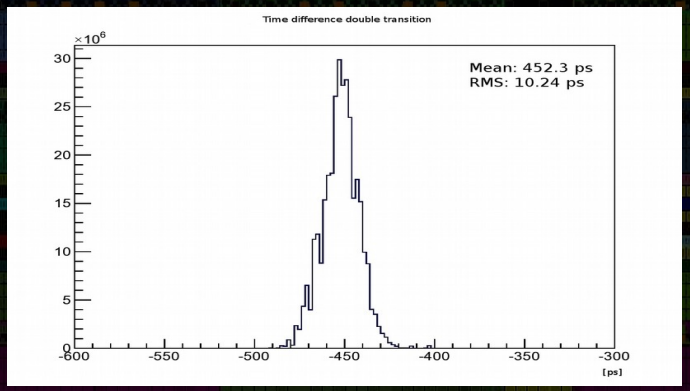


Precision vs mean

ToT measurement on 2 channels
Short pulse measurement



ToT on 2 channels



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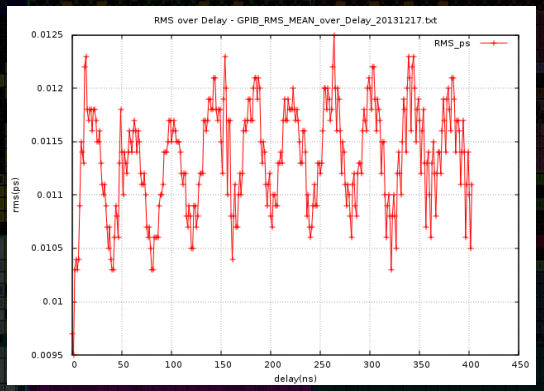

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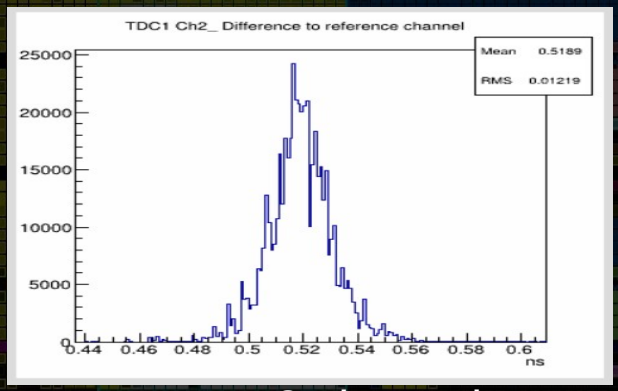

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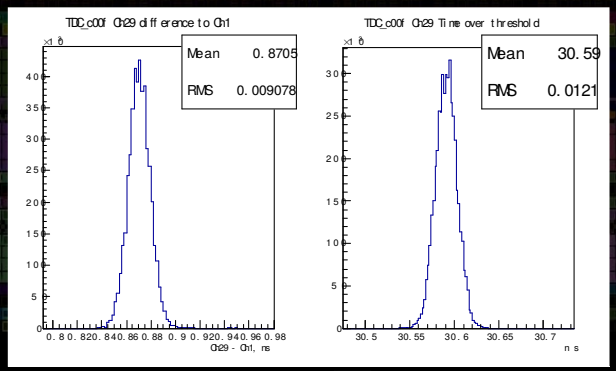
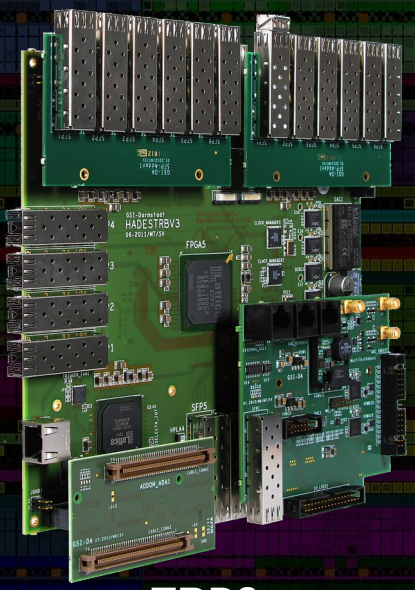


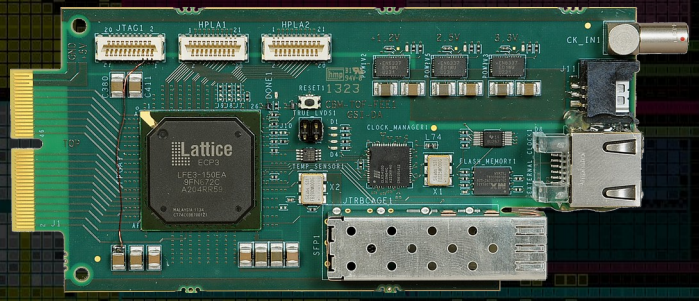
ToT on a single channel

ToT measurement on a single channel



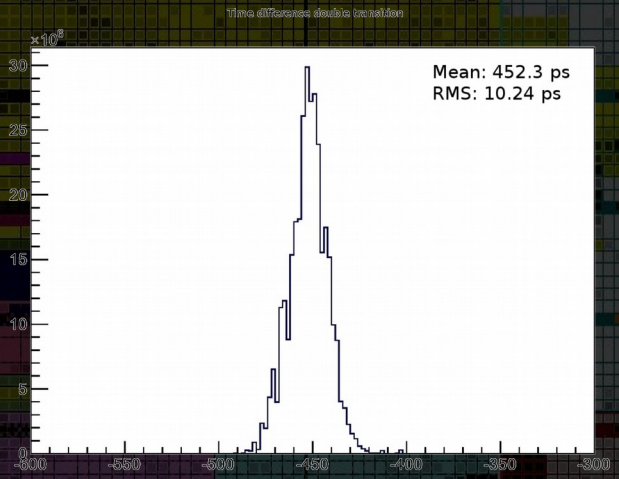
TRB3

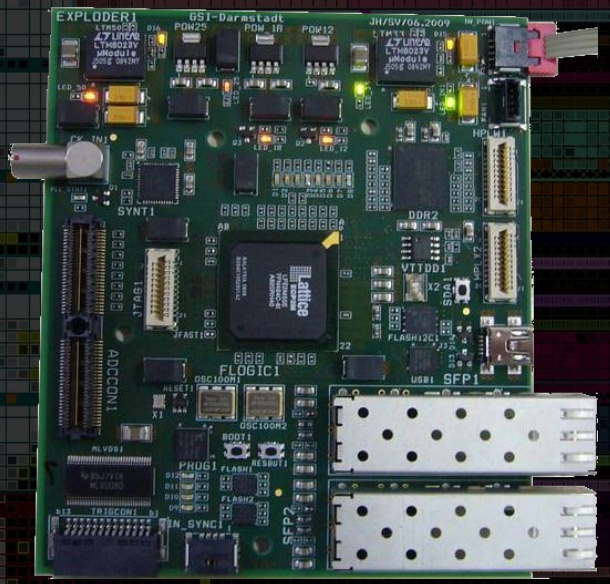
- TDC design is tested with 2 different Lattice FPGA families on 6 different boards with 2 different readout protocols
- Similar results are obtained from all of the devices
- No curve fittings or cuts are applied to the results
- The TDC can be adapted for ToF, ToT or Charge measurements



CbmTof & CbmRich

Febex3 & Tamex3

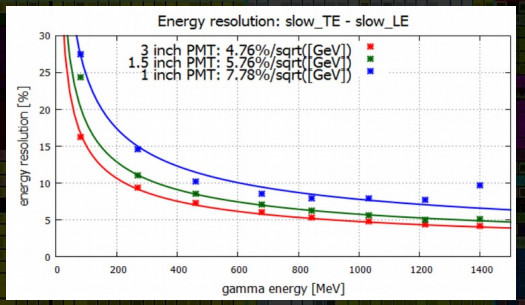


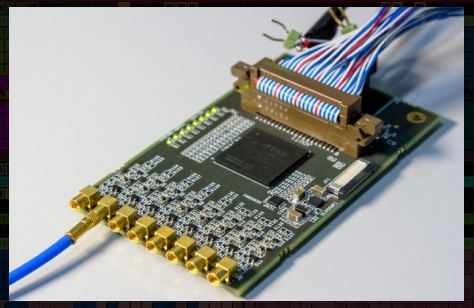


Febex2

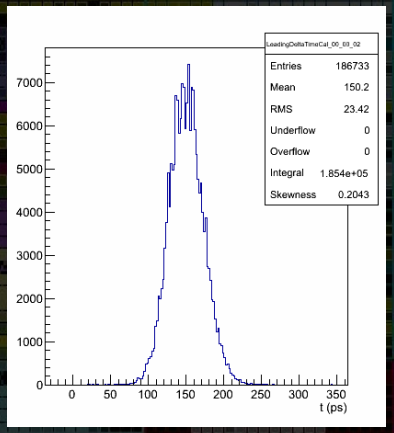
Tested with ...

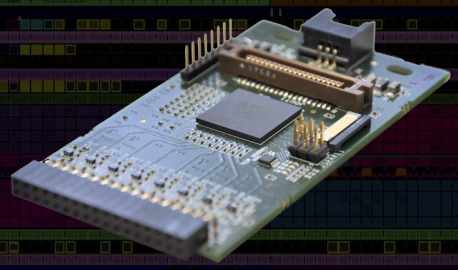
- PaDiWa Amps for charge measurements
- Tested in lab with pulser and in gamma beam in Mainz (MAMI)
- Charge precision in lab: 0.5% (no walk correction)





- PaDiWa FEE
- Pulser test: ~23 ps
- Single phototelectron laser test with MCP: ~70ps





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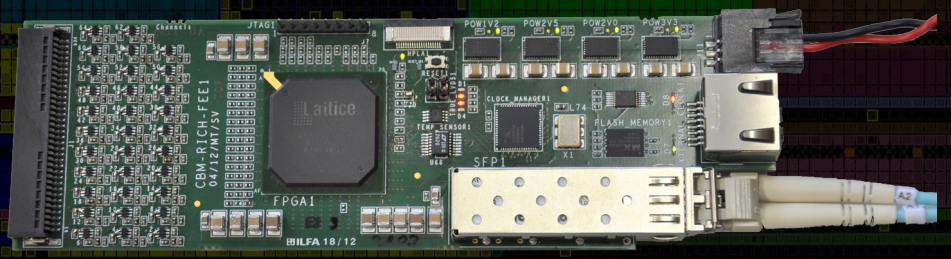
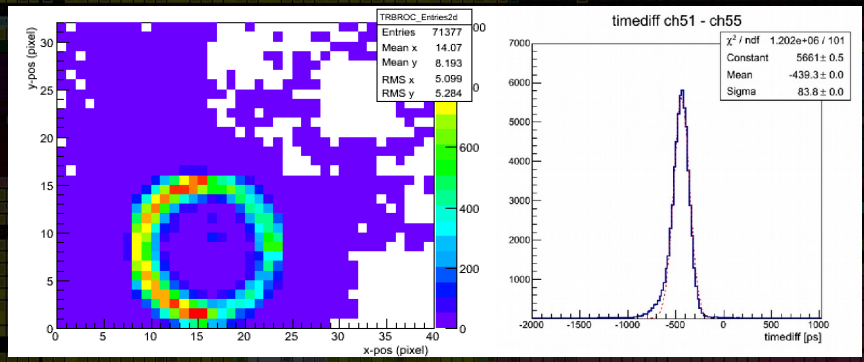
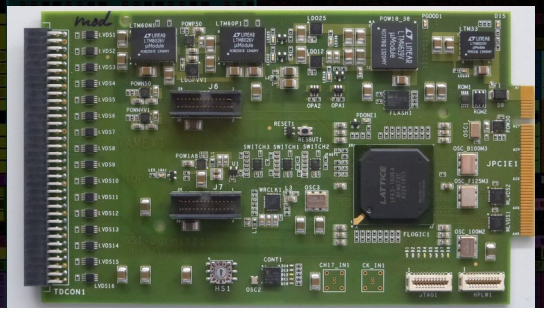
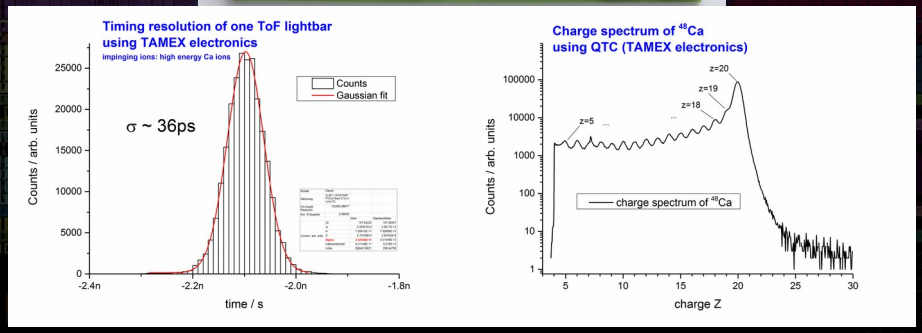


- CBM-RICH in October 2012
- FEE + 65 Ch TDC
- 83ps RMS due to FEE design error





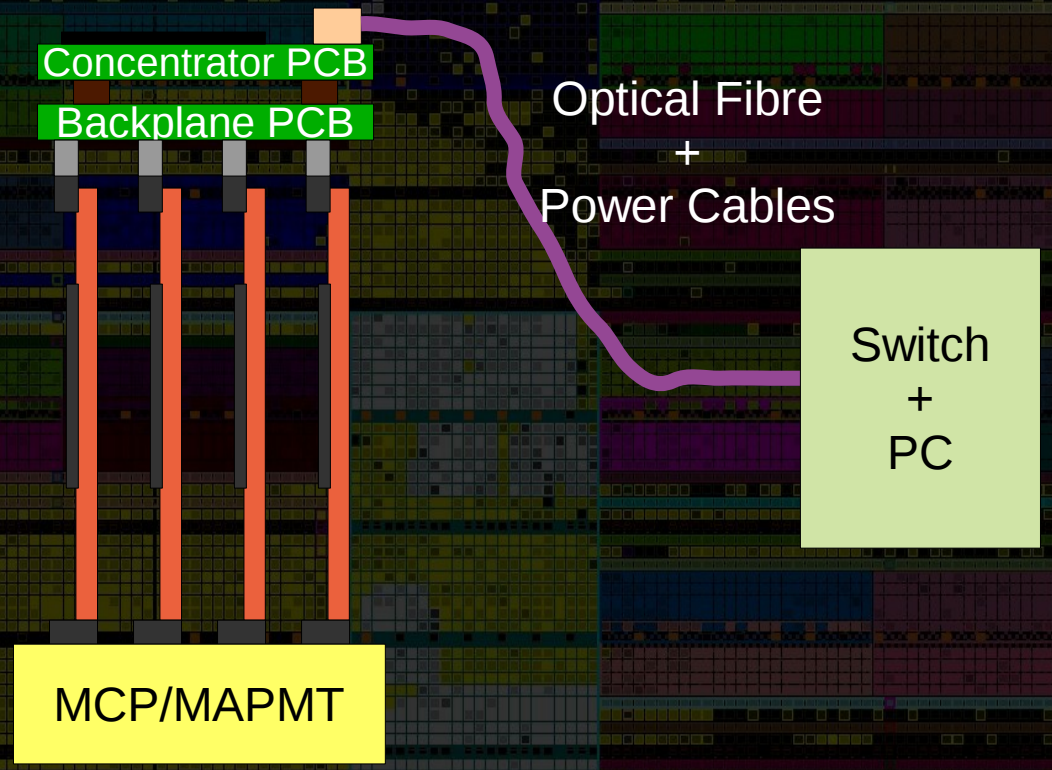
- TAMEX in September 2014
- Time (10ps) & Charge (0,9%) measurements
- Full detector precision 36ps

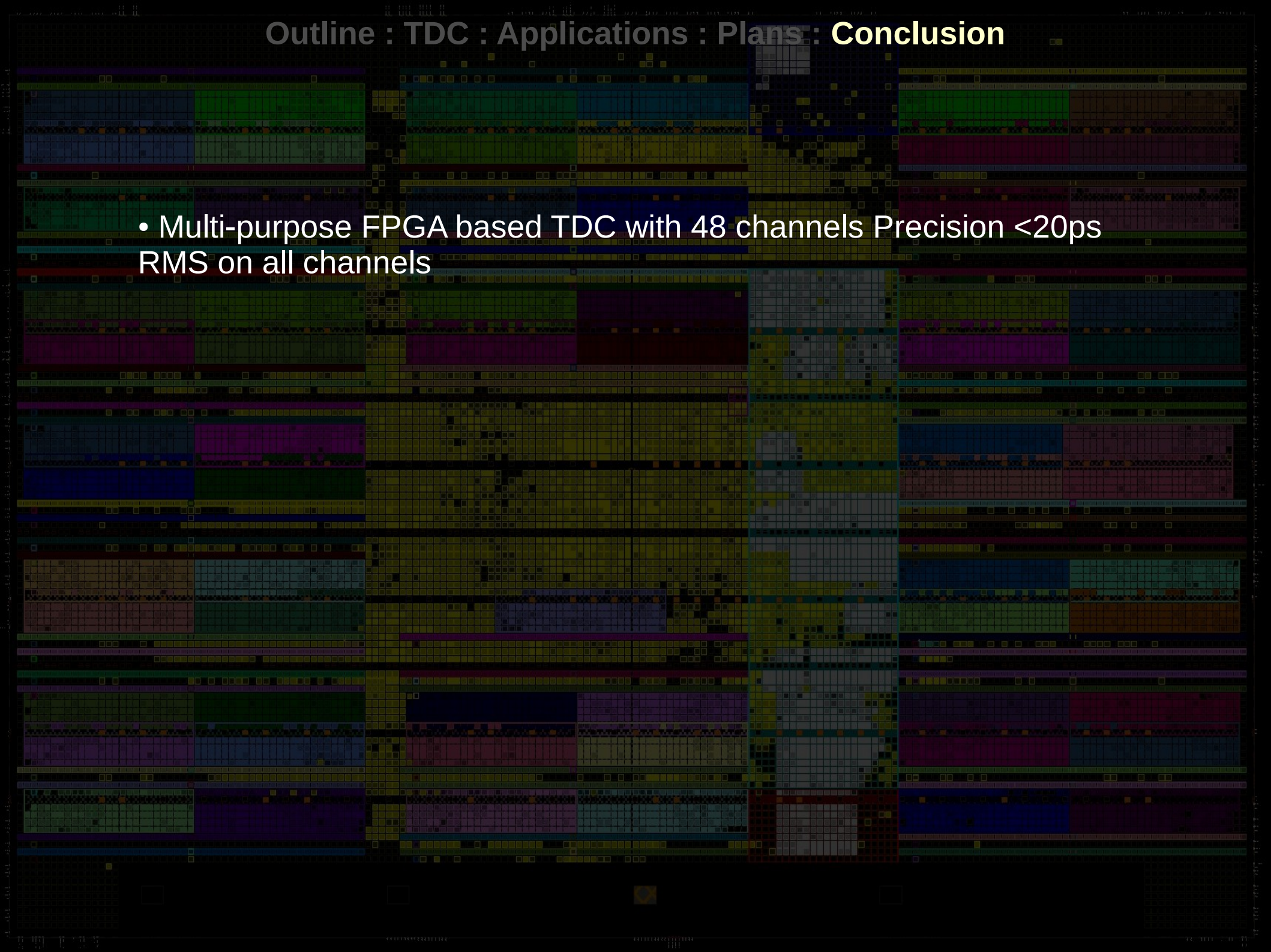


The plans are …

- to finalise the tests of the double edge measurement in a single channel
- to increase the number of channels per FPGA (back) to 64
- to increase the TDC clock frequency to 240MHz (or better 360MHz) for a synchronous system – PANDA & CBM
- to implement TDC in the next generation Lattice FPGA ECP5 for the DIRICH board

- DIRC-RICH → DIRICH: Joint development of Panda-DIRC, CBM-RICH and HADES-RICH
- Padiwa + TDC
- Higher Integration needed to put TDC also on Padiwa
- We have to keep form factor → ECP3-150 too big
- New Lattice-FPGA available: ECP5-85F
  - 32 channels ToT, ~10ps precision TDC
  - Very good price: ~40€
  - 4 channels <3.2Gbps, 1.1V, 80mW static power
  - 17x17mm^2 for 381caBGA (same size as MachXO2)
  - All features needed





- Multi-purpose FPGA based TDC with 48 channels Precision <20ps RMS on all channels

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- TDC on DIRICH

TRB3 Community

Developers

Cahit Uğur	TDC
Jan Michel	TrbNet & DAQ
Grzegorz Korcyl	GbE
Manuel Penshuck	CTS
Michael Traxler	Organisation & Hardware
Ludwig Meier	Slow Control Software
Jörn Adamczewski-Musch	DAQ & Analysis
Sergey Linev	DAQ & Analysis
Matthias Hoek	Unpacking & Analysis

Active Users

Marek Pałka
Christian Pauly
Adrian Zink
Andreas Neiser

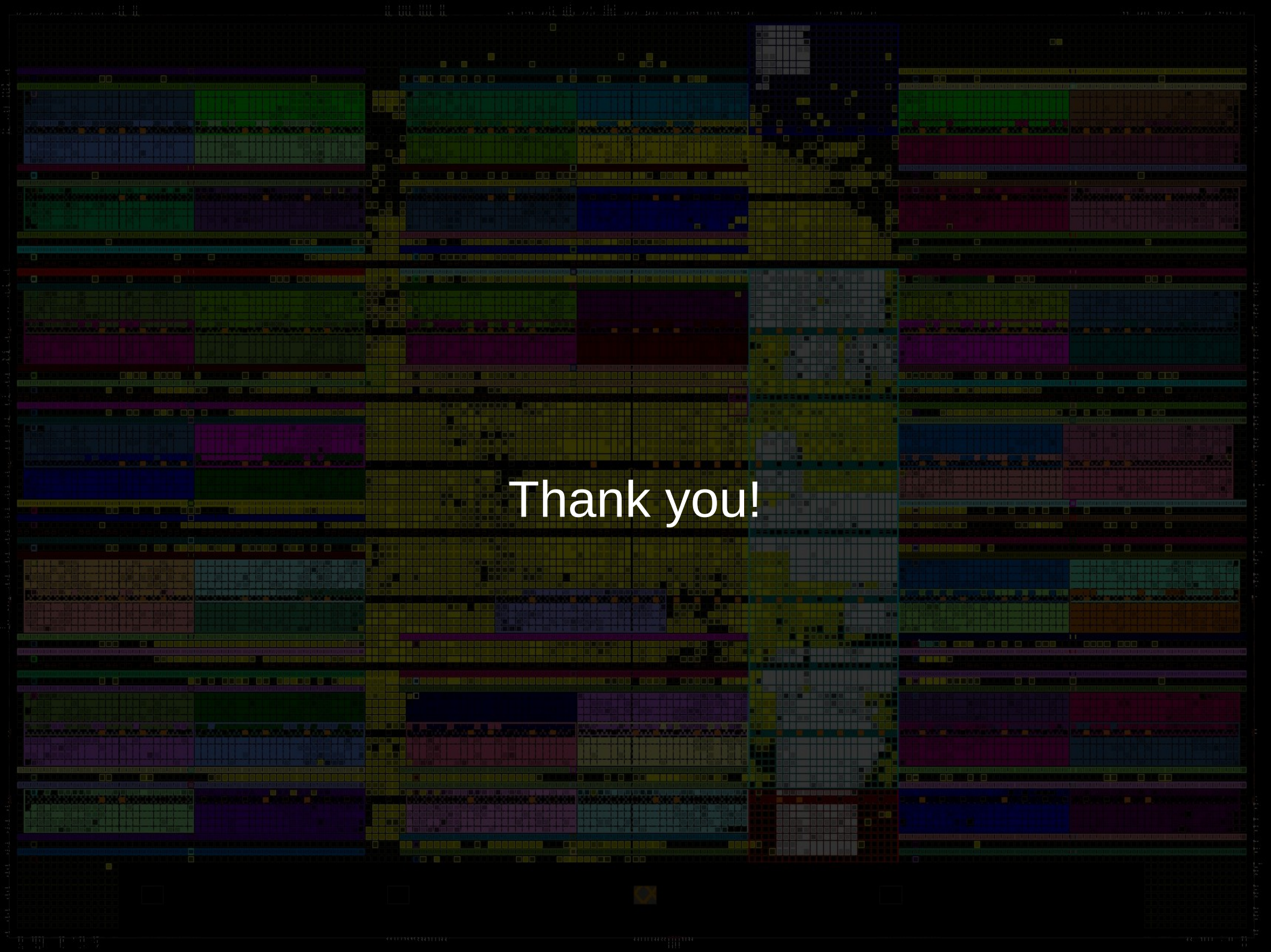
PANDA DIRC Groups in Mainz & GSI
CBM RICH & CBM ToF

Detector Groups

PANDA Barrel DIRC
PANDA Disk DIRC
PANDA ToF
CBM Forward Calorimeter
CBM – RICH
CBM – ToF
HADES MDC FEE
HADES Calorimeter
Mainz A2 Collaboration
Mainz Neutron Detector

Coimbra PET Scanner
ATLAS

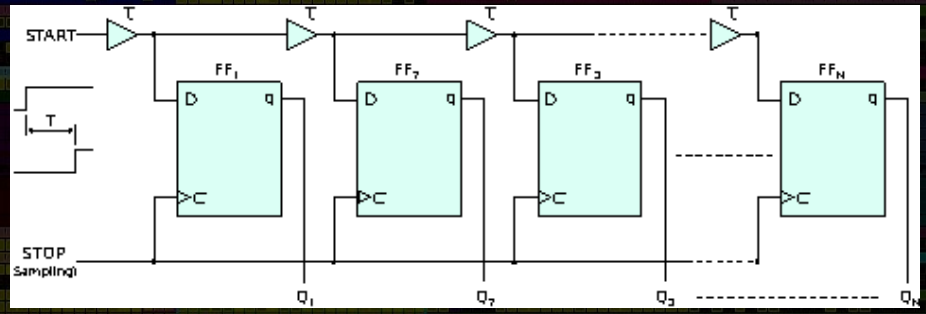
and many more to come...


Thank you!

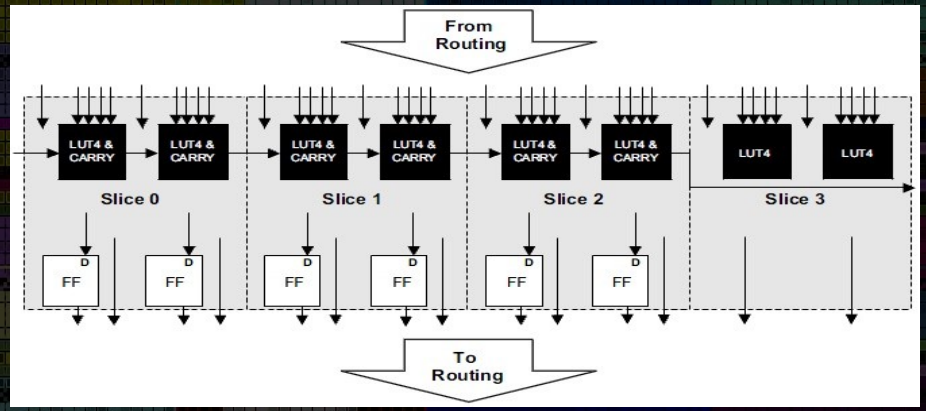
Backup Slides

Tapped Delay Line Method

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line



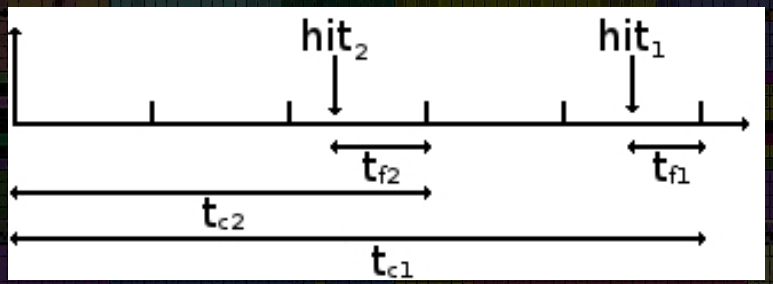
Tapped Delay Line Method



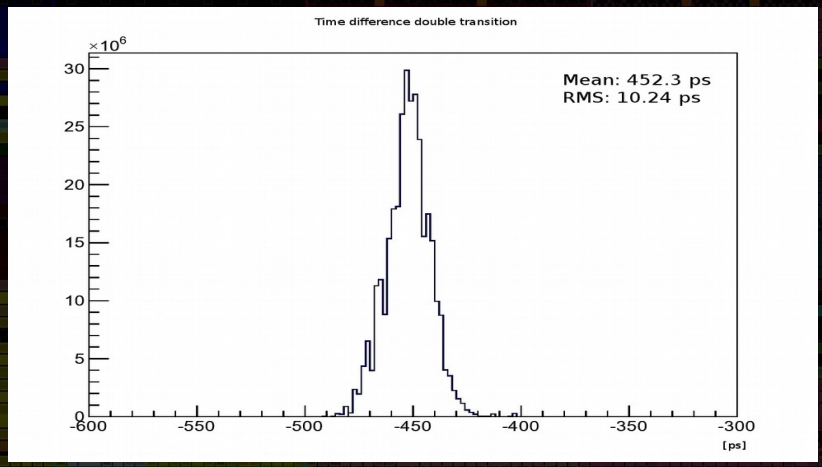
PFU Diagram

Laboratory Test Results

- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps against the same clock
- Precision: 10.34 ps / √2 = 7.3 ps RMS



Time difference between two measurements



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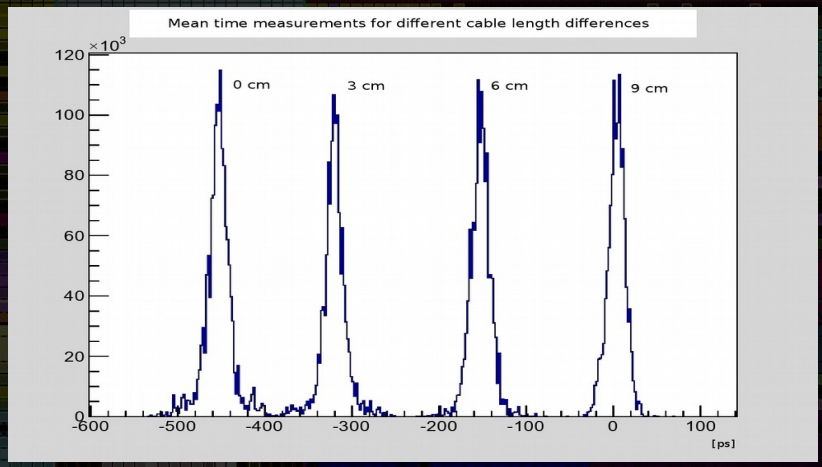
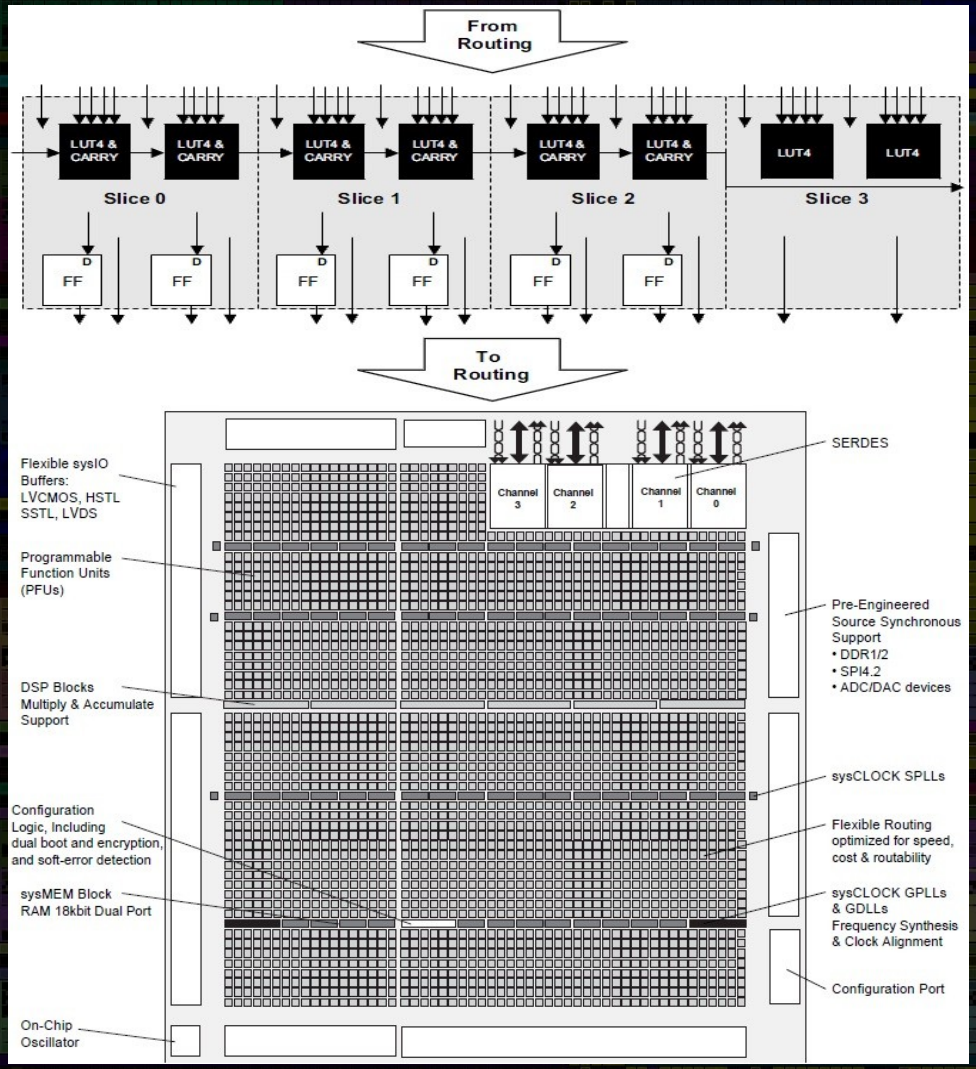
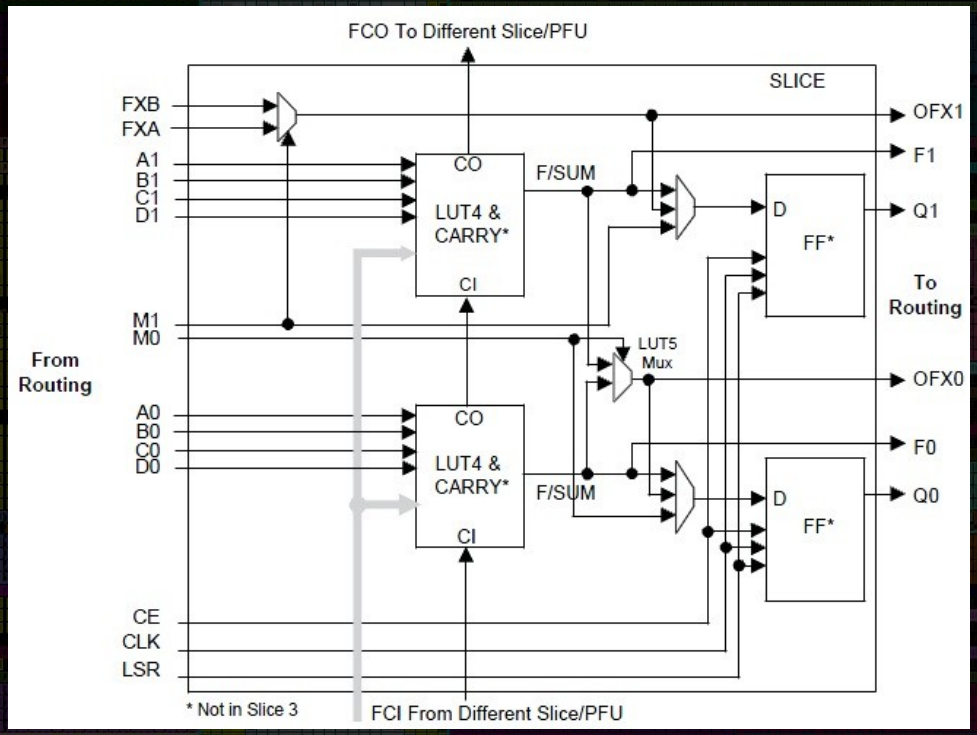


Mean measurement test

Architecture of TDC

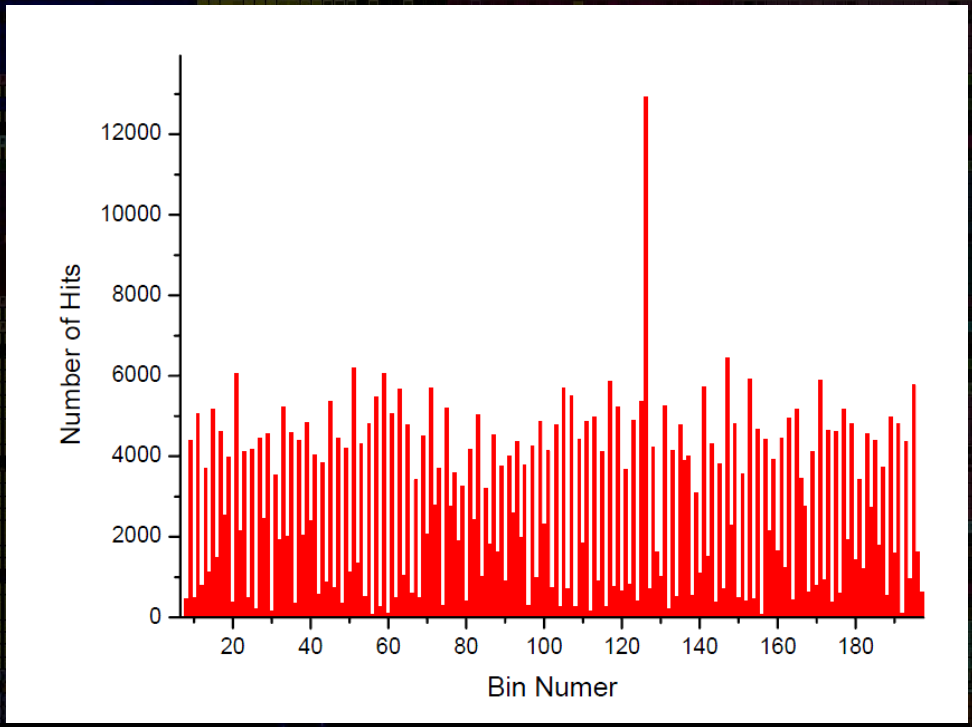




Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floor-plan

Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture



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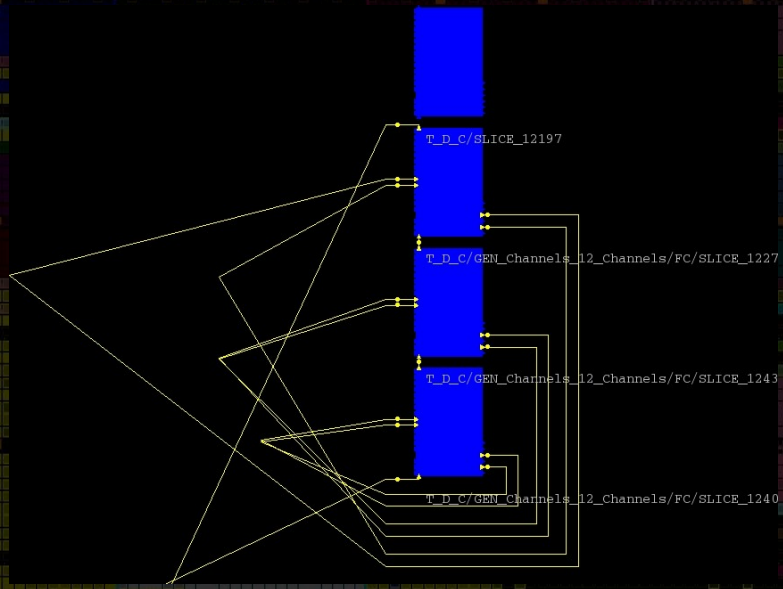

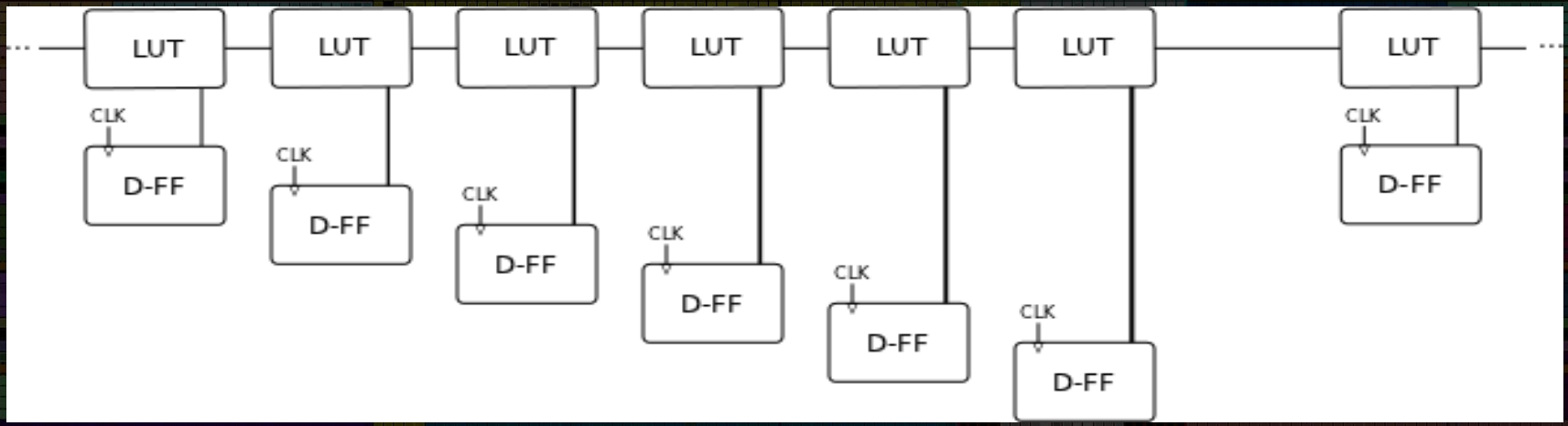

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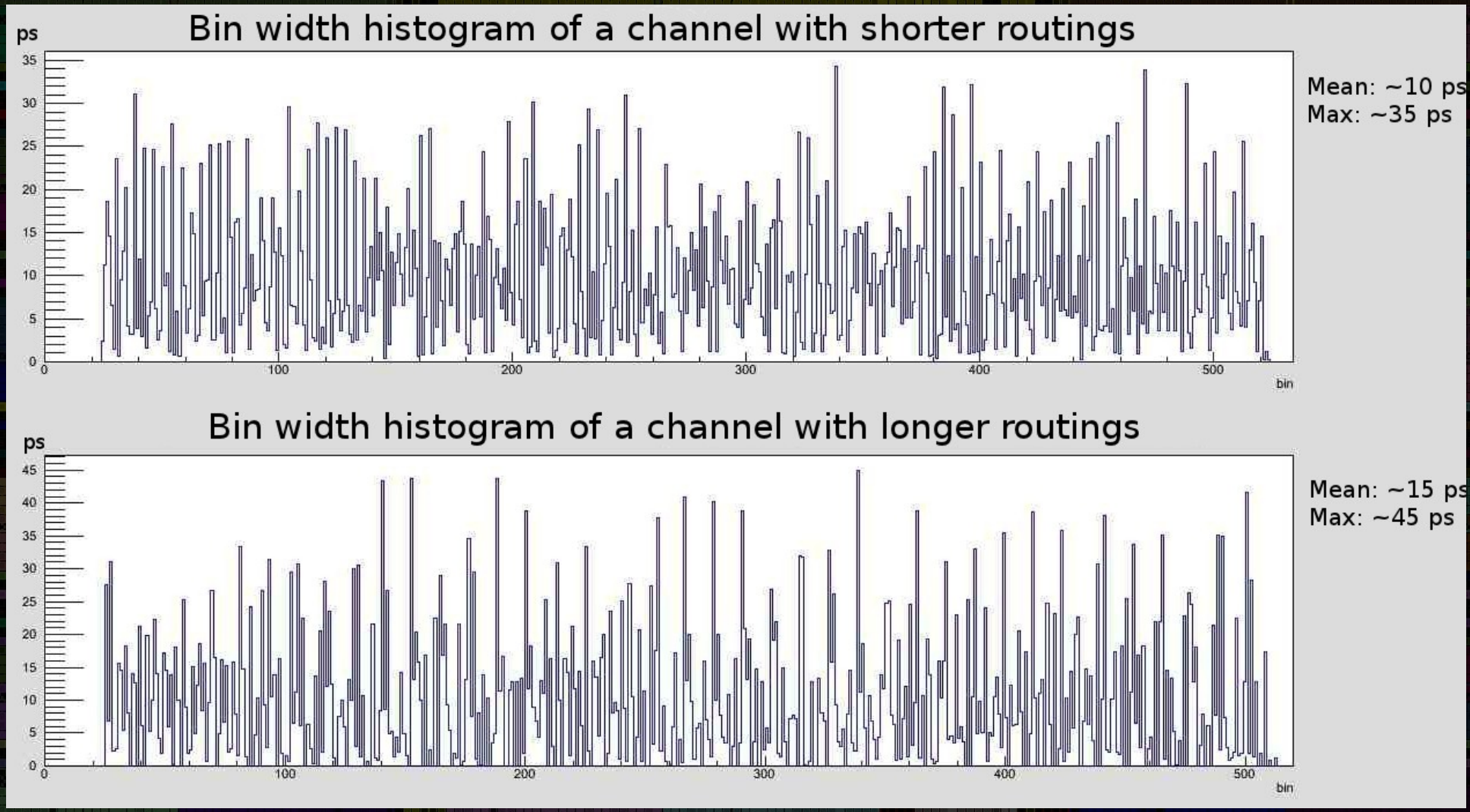

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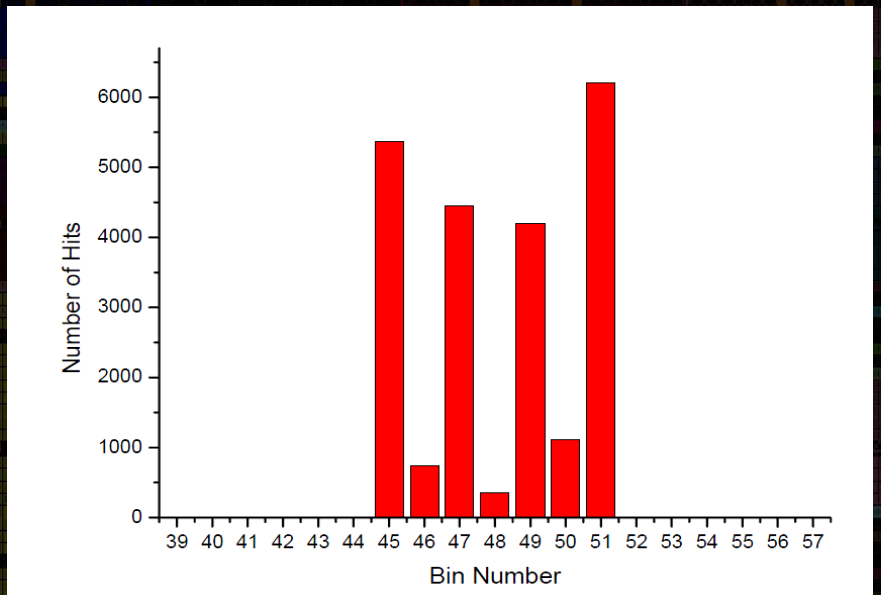
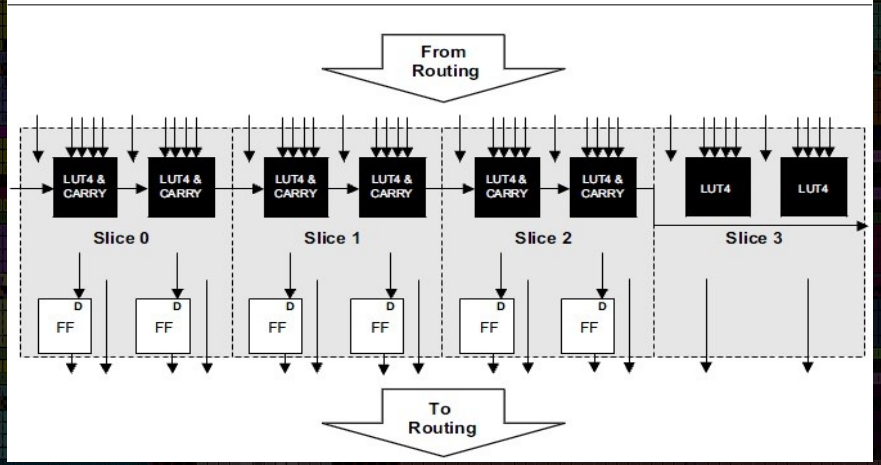
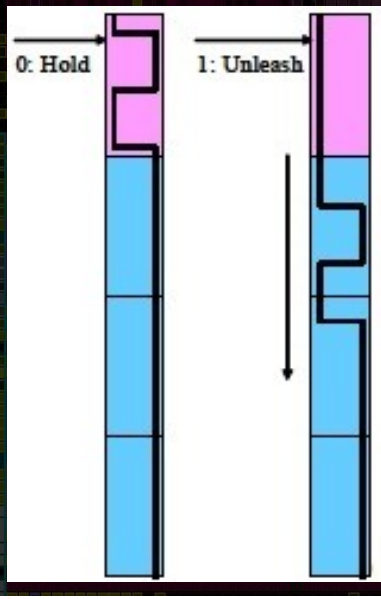
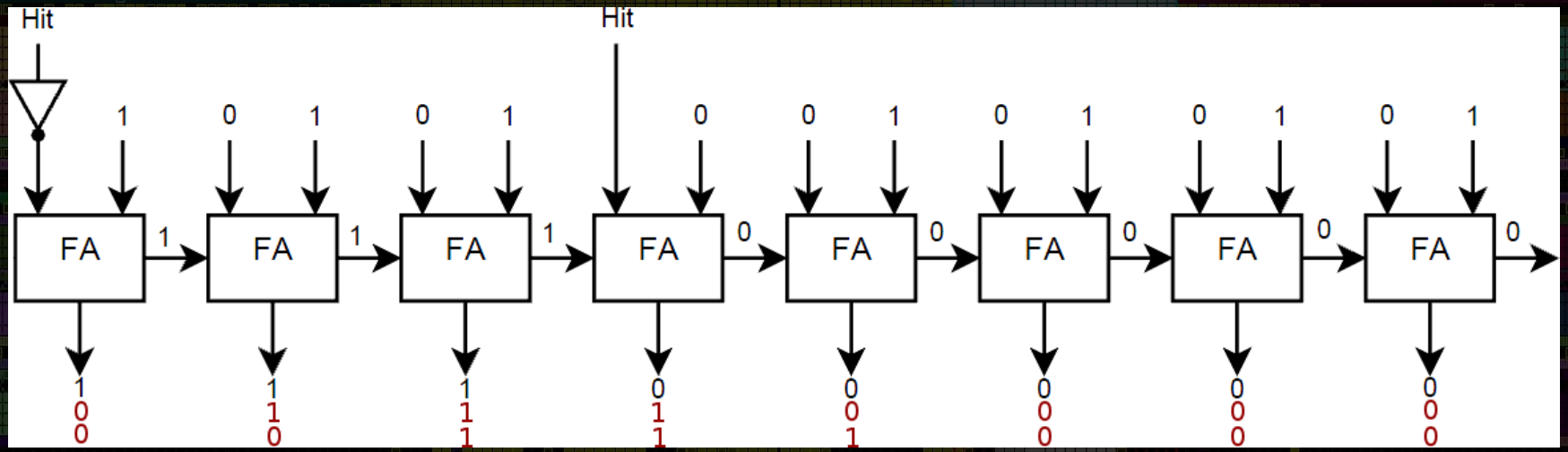




Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced





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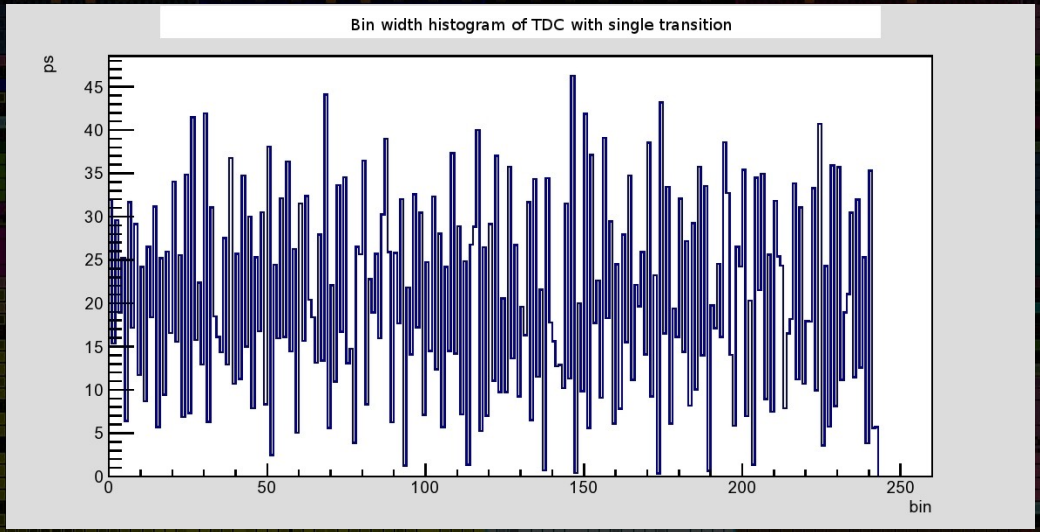
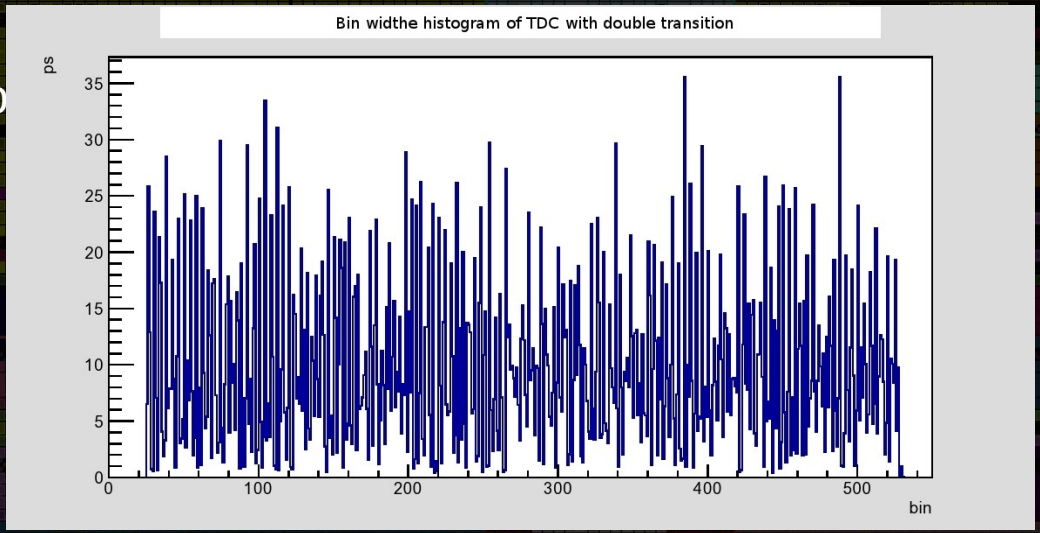


Bins: ~240
Mean: ~20 ps
Max: ~45 ps

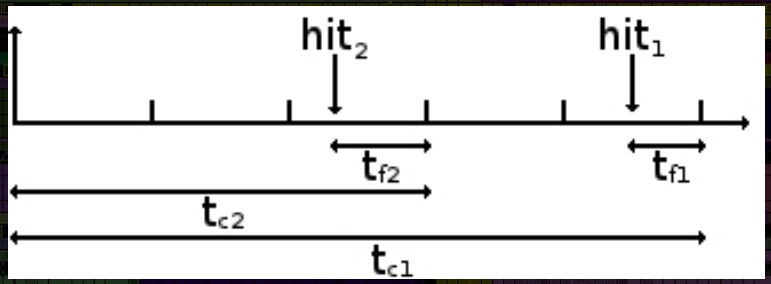
- More virtual bins
- Narrower bins
- Homogeneous bin distributio

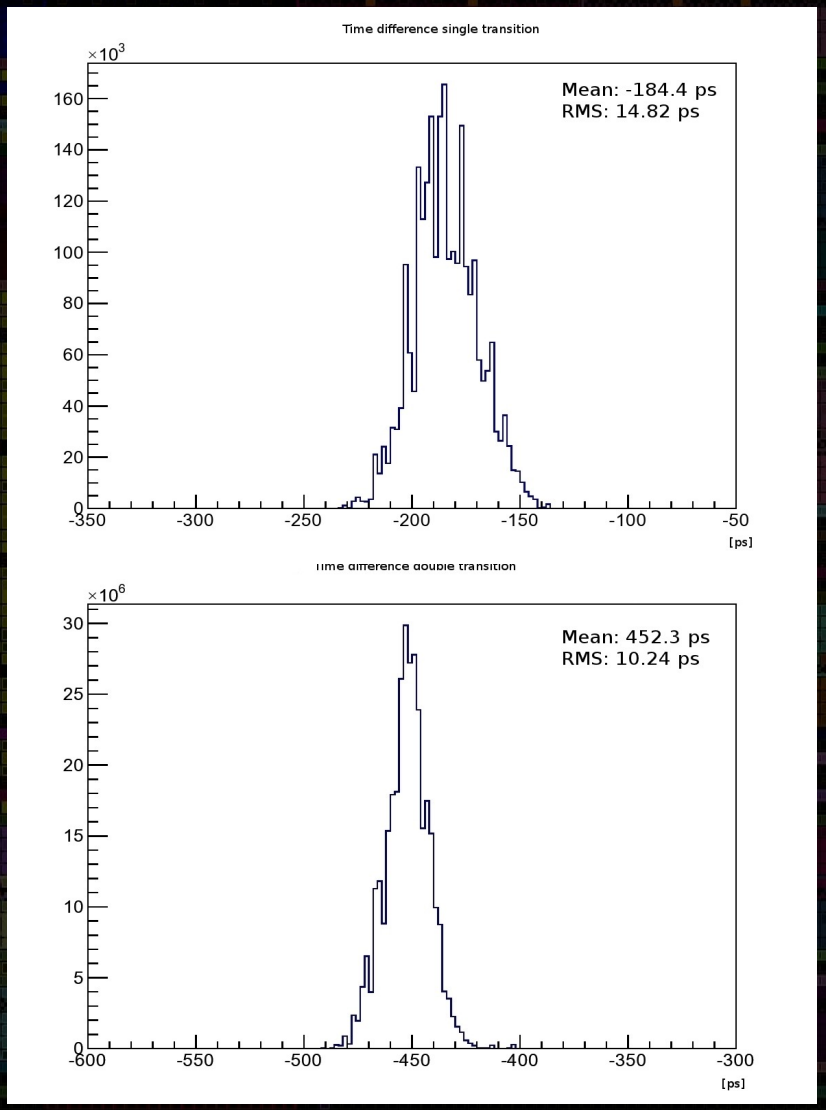


Bins: ~520
Mean: ~10 ps
Max: ~35 ps

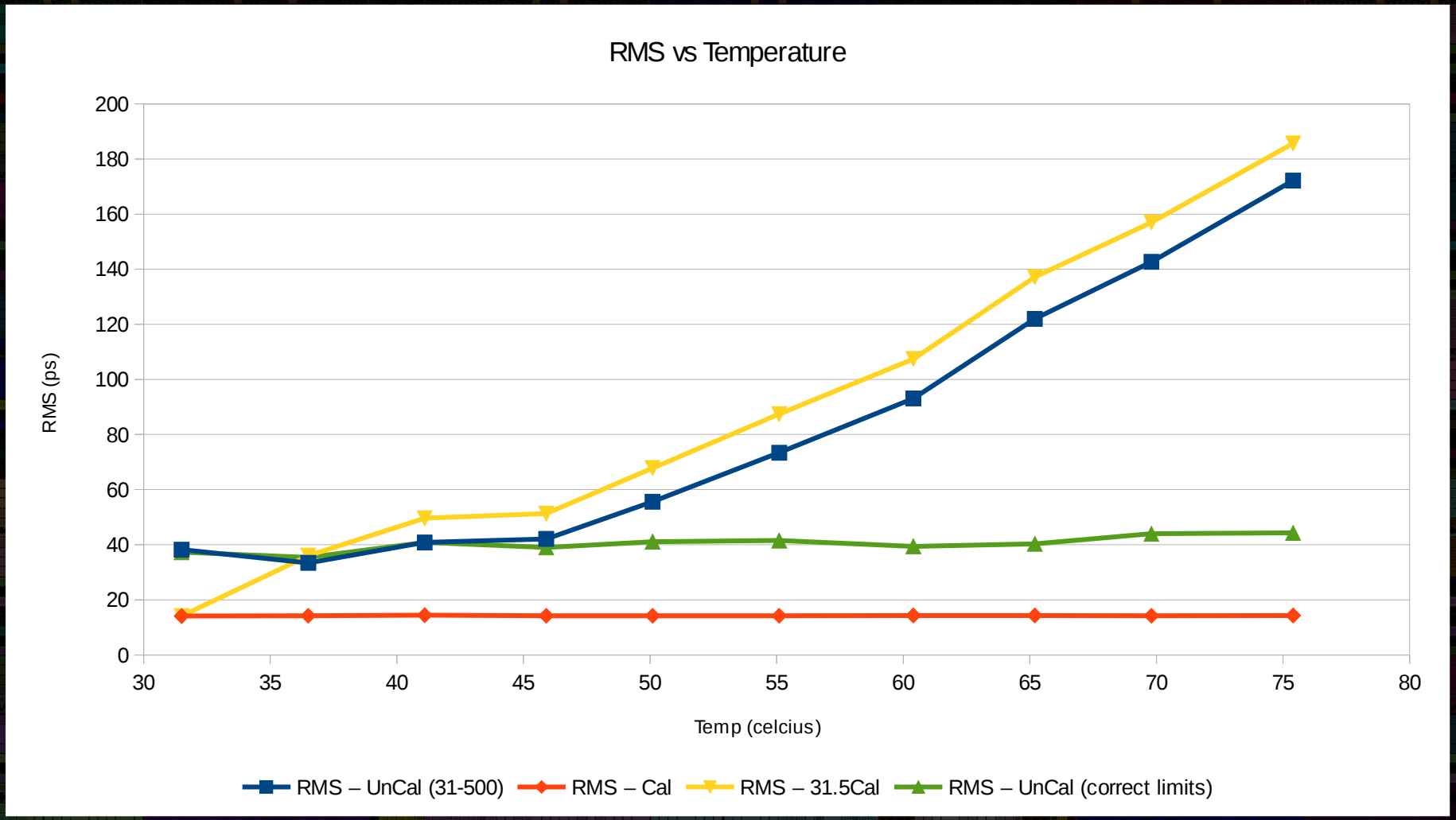
Statistical Error & Precision

- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps against same clock
- Precision: 10.34 ps / √2 = 7.3 ps
- Effect of 2 transitions: 14.82 ps / 10.34 ps = 1.43 factor

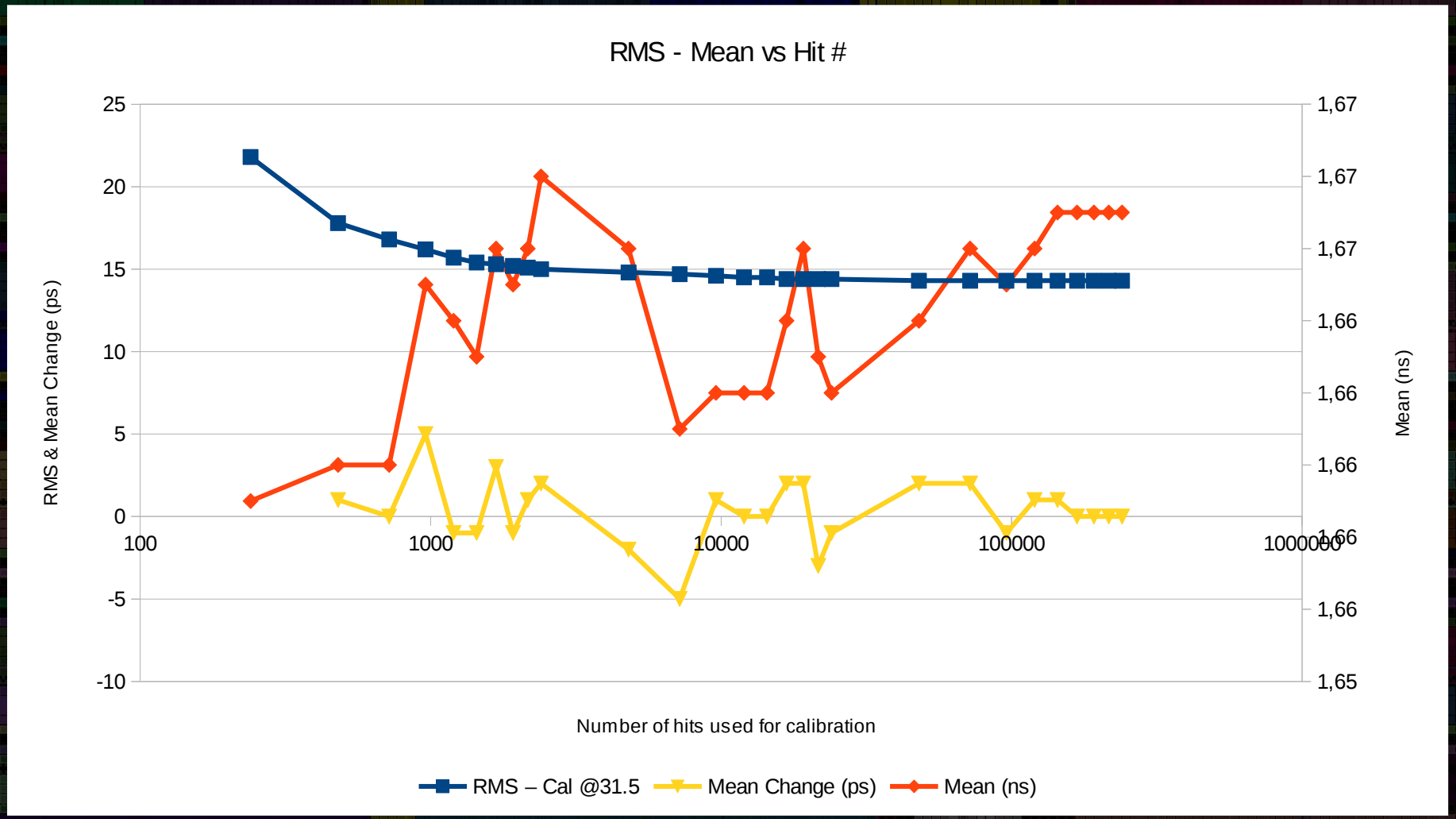


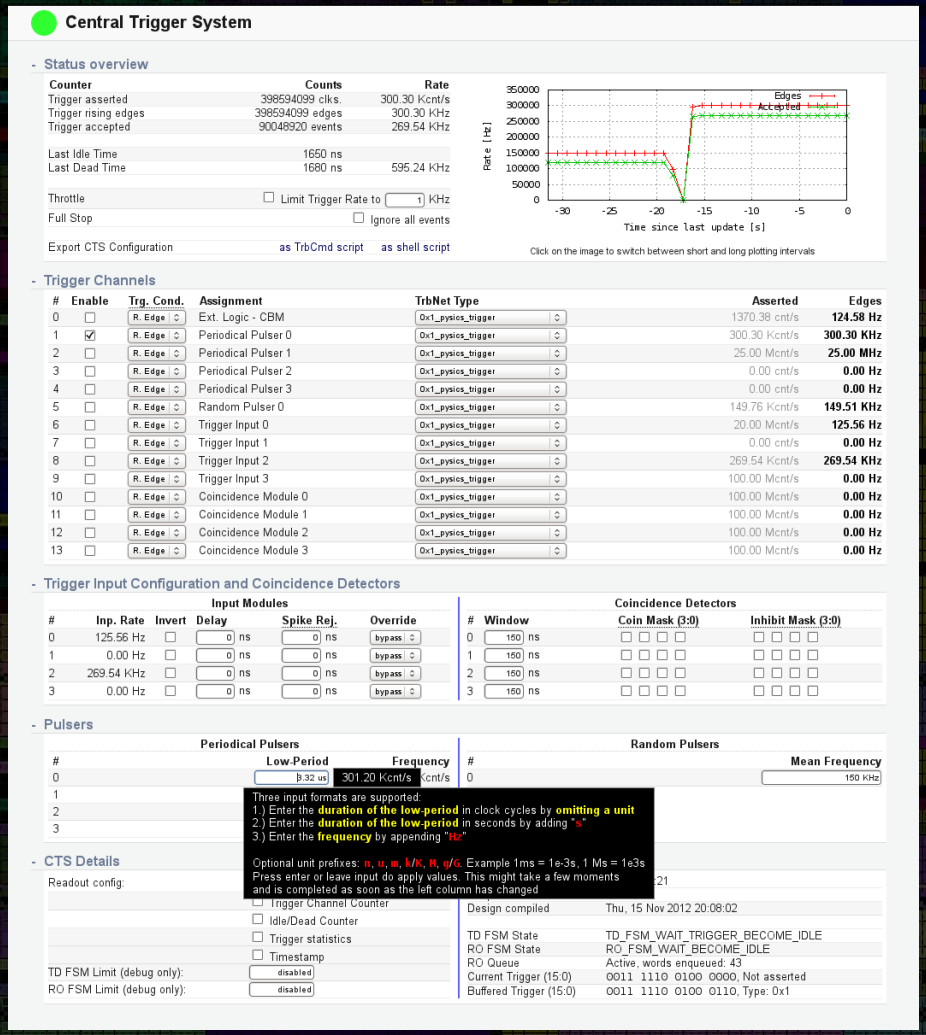


Precision vs Temperature



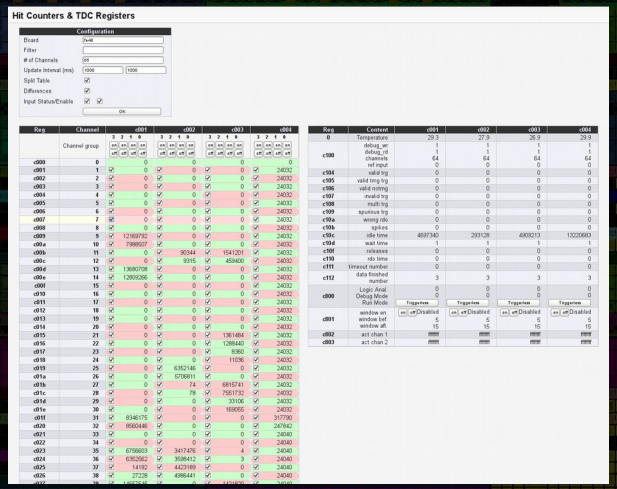
Precision & Mean vs Statistics



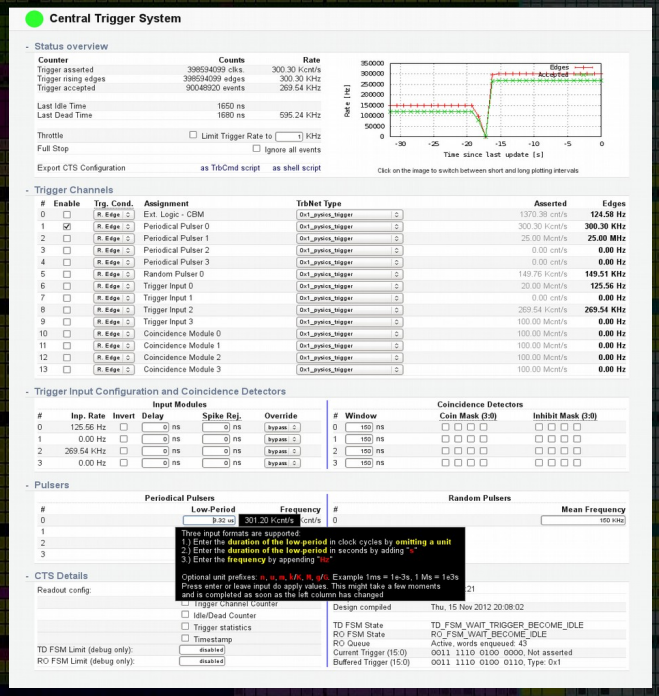


- Extendible and modular structure
- Master and slave mode operation
- Up to 16 independent trigger modules
- 4 channel TDC for trigger time
- 8 general purpose trigger inputs
- Coincidence detection
- Periodic & Random pulser
- On-board and off-board trigger distribution
- Trigger generation from TDC channel inputs
- Tested successfully during the CBM and PANDA test beams with slave and master modes

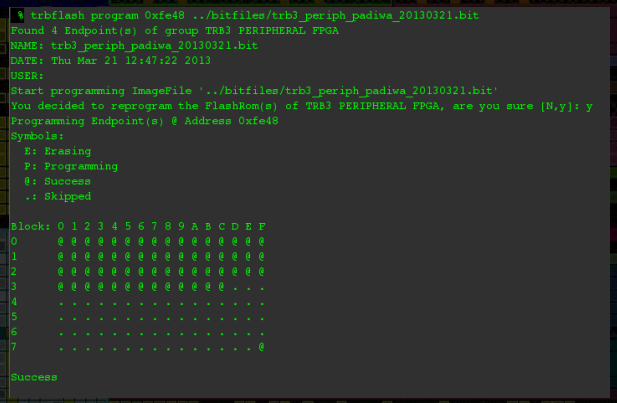
Outline : Hardware : TDC : CTS : Software : Applications : Conclusion



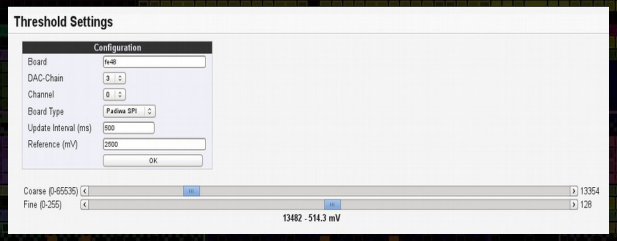
TDC
readout & channel
monitoring & control



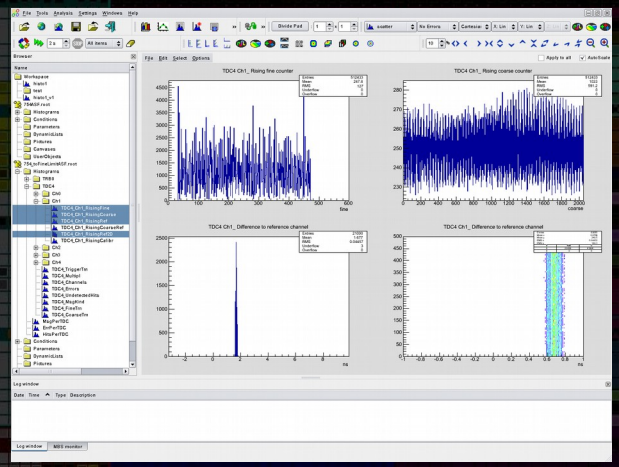
Trigger
processing & control



Console based
slow control software
with many features

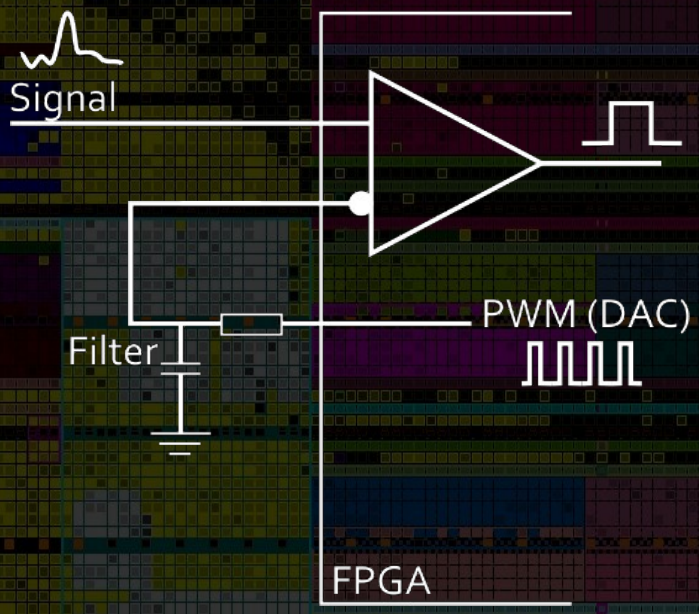


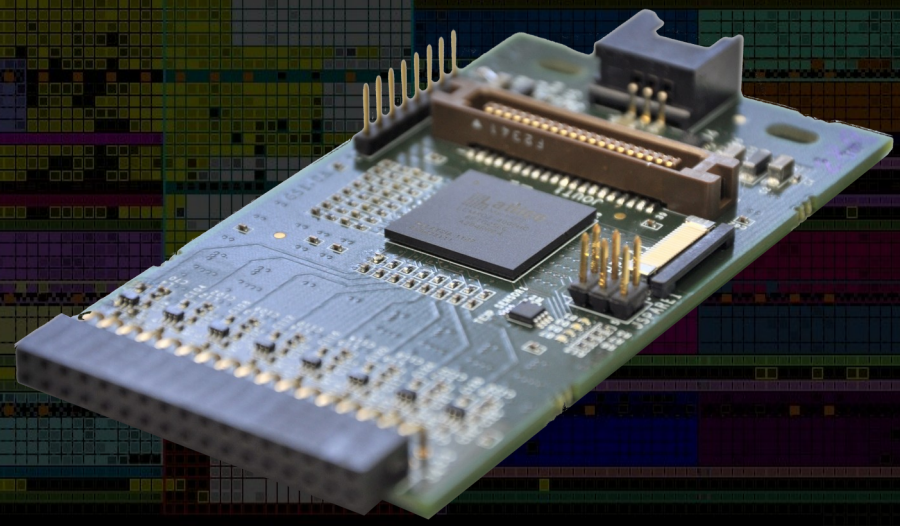
Threshold setting



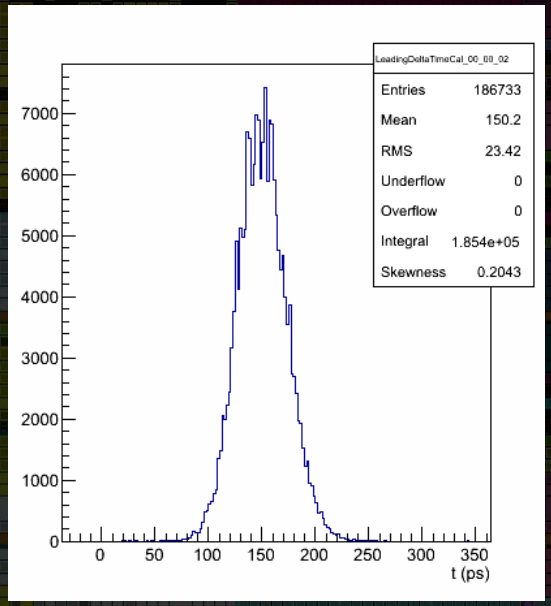
Unpacking & Online Analysis
& DAQ

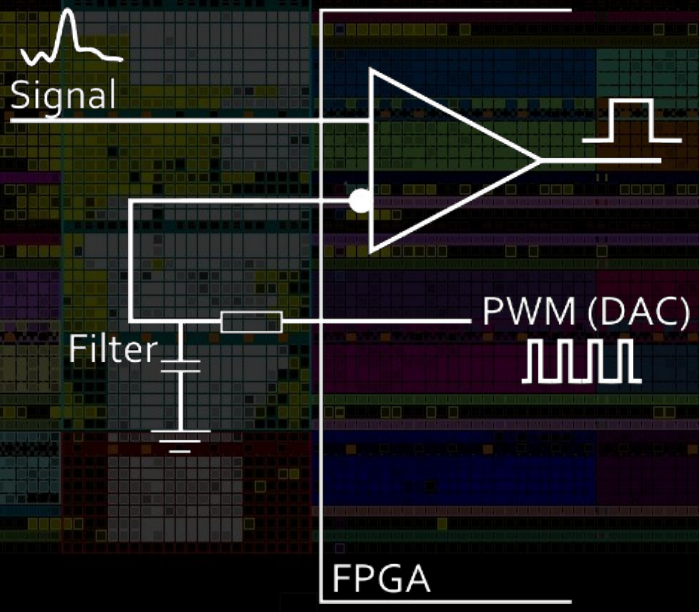
- Pre-amplified with commercial amplifiers (MMICs)
- Input LVDS buffers in FPGAs are used as discriminators – Lattice MachXO2
- The leading edge time and Time over Threshold is encoded in the digital pulse
- The thresholds are set by FPGA via PWM and low pass filter
- FEE is placed directly at the detector, only digital signals are sent out
- Time measurements are done by TDCs implemented in FPGA (TRB3)





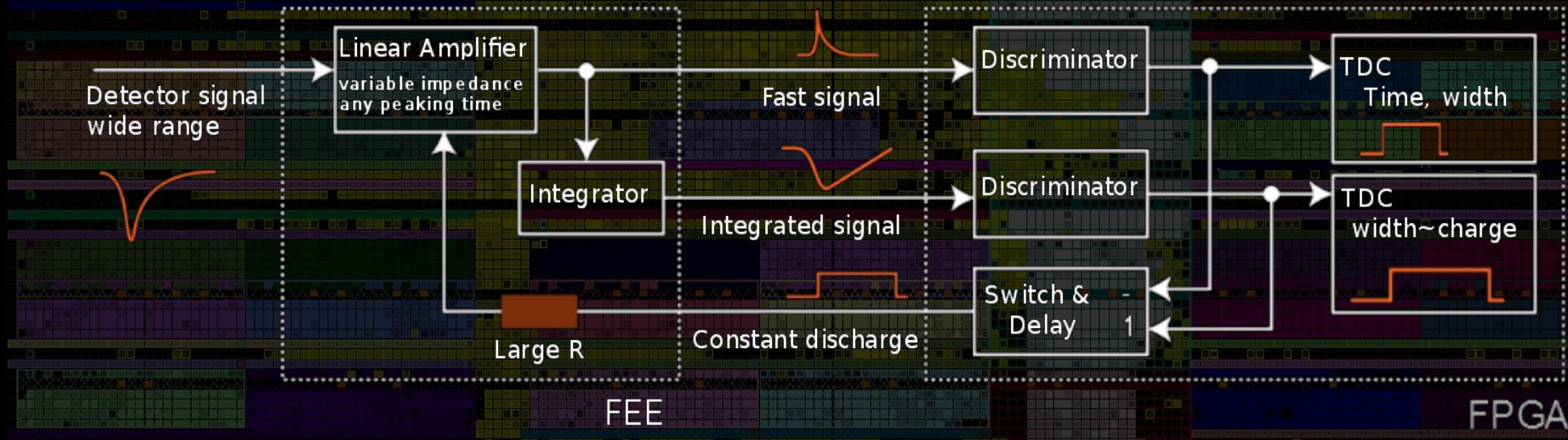
- Test setup: 500 μV, 6 ns width, analogue signal as input to PCB, amplification x40
- Threshold is set on the reference LVDS input PWM + low-pass with a resolution of <100 μV
- Pulser test: ~23 ps
- Single phototelectron laser test with MCP: ~70ps
- FEE cost (without PCB+connectors) per channel only 0.56€ (16 channel version)
- Tested at the PANDA DIRC and Barrel DIRC beam times in 2012, 2013, 2014

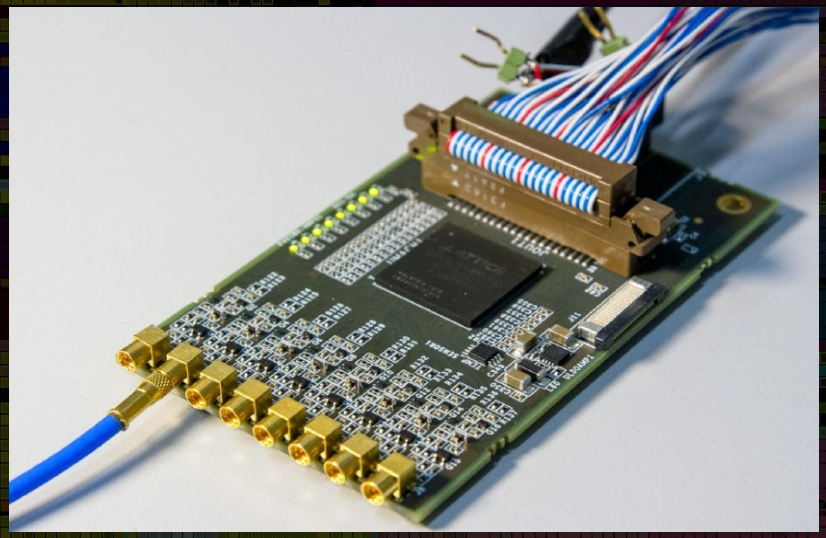




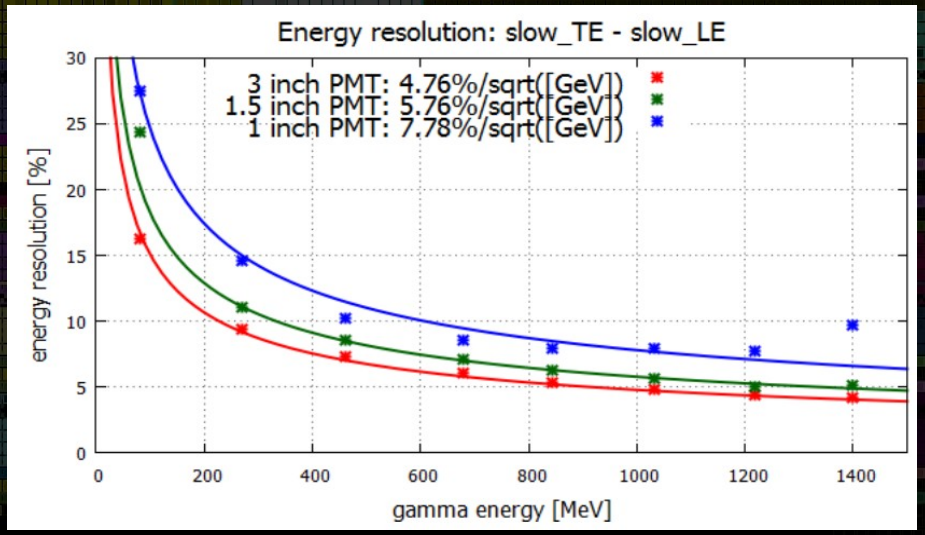
Idea: Modified Wilkinson ADC

- The input signal is integrated with a capacitor
- The capacitor is discharged using a current source → fast crossing of zero
- Measure time necessary to reach zero

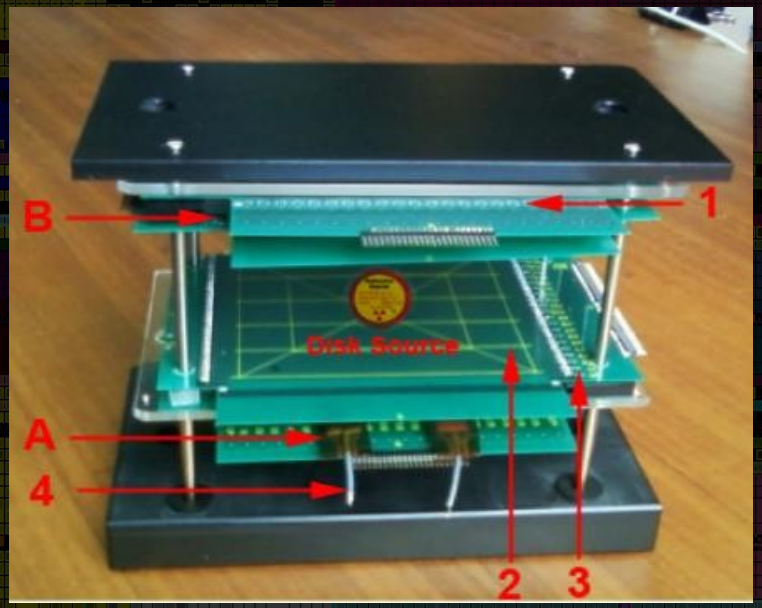




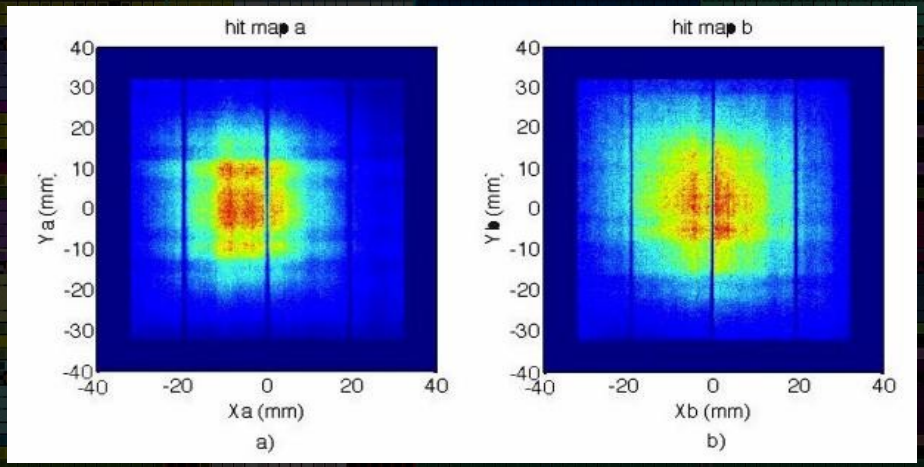
- Tested in lab with pulser and in gamma beam in Mainz (MAMI)
- Charge precision in lab: 0.5% (no walk correction)
- Charge precision: as low as 5% (no walk correction)



- Positron Emission Tomography (PET) for molecular imaging
- Approach is RPC (Resistive Plate Chambers) based
- Simulations suggest factor 8 better performance over the best commercial tomography [1][2]
- Animal PET Prototype demonstrated 0.4 mm image resolution with TRB2 [3]
- Prototype for high resolution animal PET scanner and low sensitivity (for cost reasons) whole body human scanner is under development



A-detector a; B-detector b; I-X strips; 2-Y strips;
3-signal division network; 4-high voltage connections. [3]



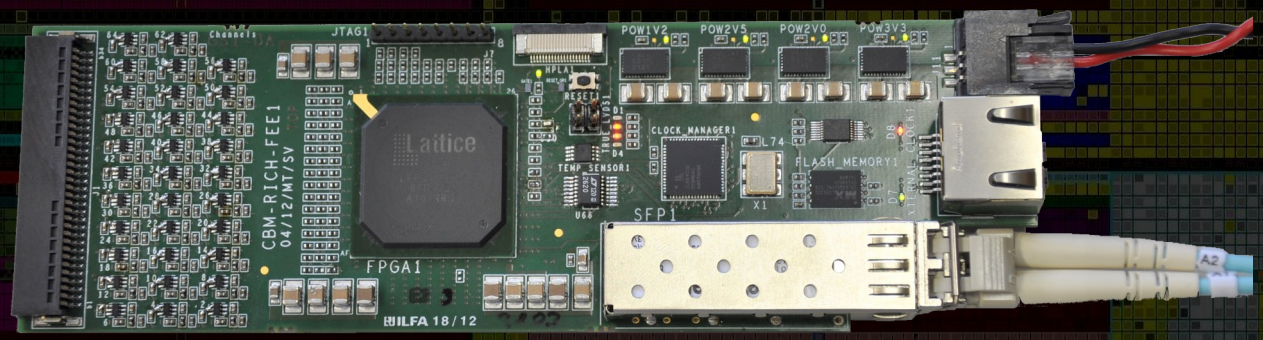
Hit map in a) detector a, and in b) detector b. The shadowed vertical lines correspond to the 0.35 mm spacers used to define the gap width. [3]

[1] A. Blanco et al., Nucl. Instr. and Meth. A602 (2009) 780;

[2] M. Couceiro et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 2651;

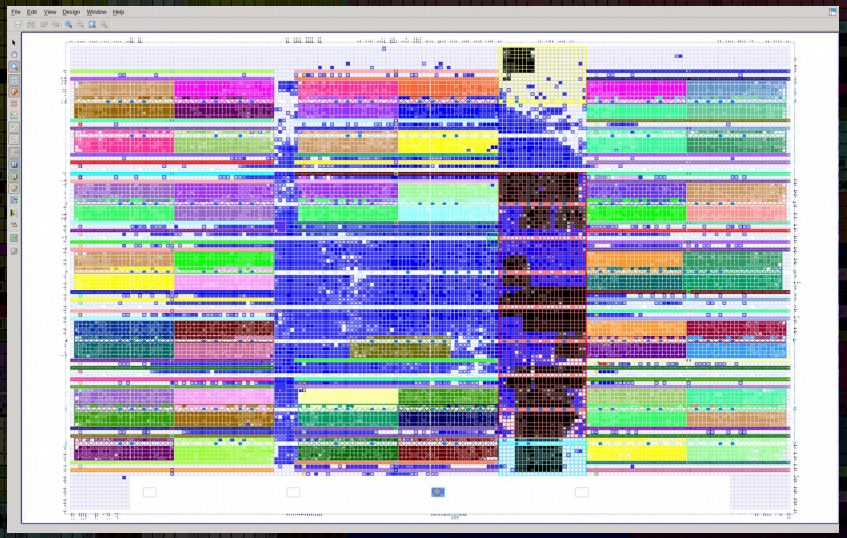
[3] P. Martins et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 3760

FEE & 65 Channel TDC



- 64 signals from detector
- Amplification
- Thresholds
- Input signal discrimination
- Time measurement
- Data readout

- Trigger signal is digitised for reference time (65th channel)
- Data readout through 2GBit/s optical link
- 5x16 cm to be plugged on the back of an MCP-PMT
- Very high density for FEE & 65 channel TDC + DAQ + Power
- Tested during the CBM October 2012 test beam
- The Sync message is processed at the internal TRB3-CTS and distributed to 4 FEEs
- Half detector readout with CBMRICH-FEE, other half with nXYTER



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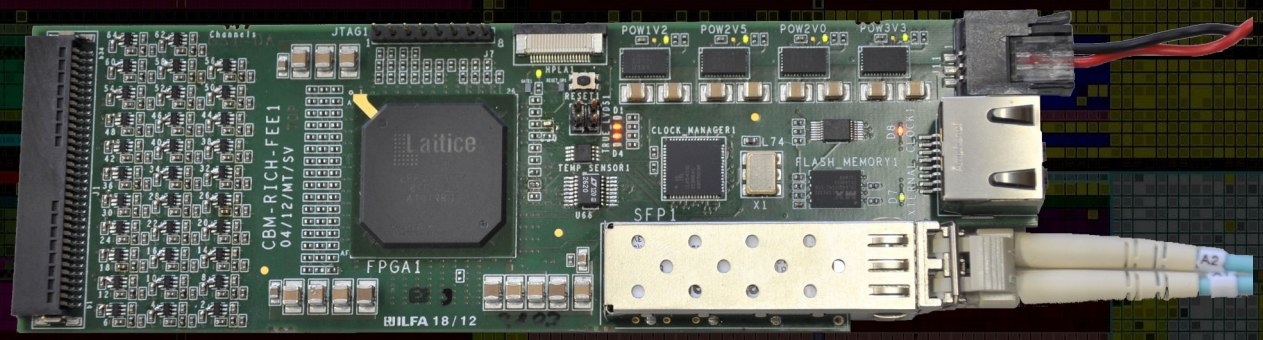

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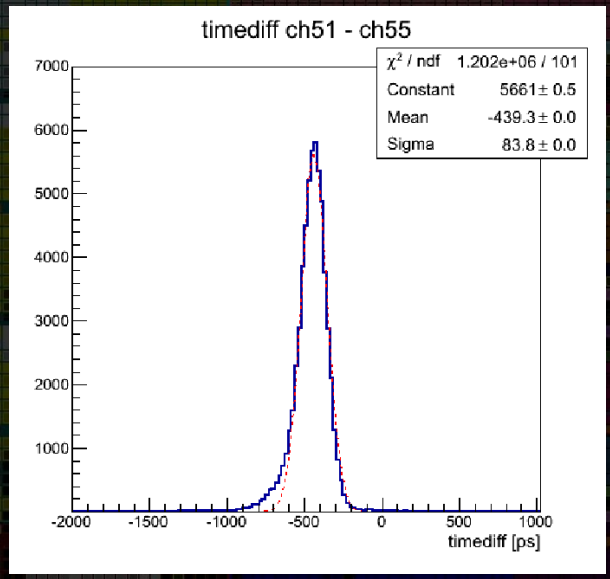

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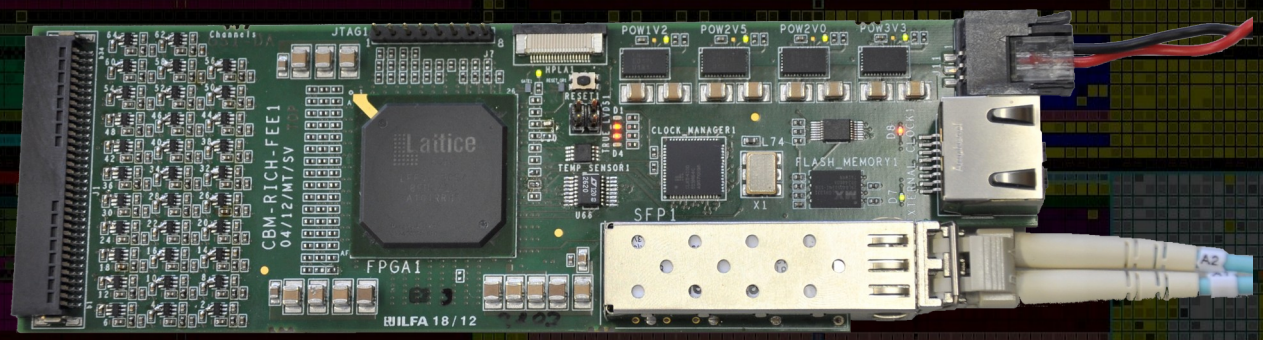

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