

FPGA-TDC Status and Plans

Cahit Uğur¹

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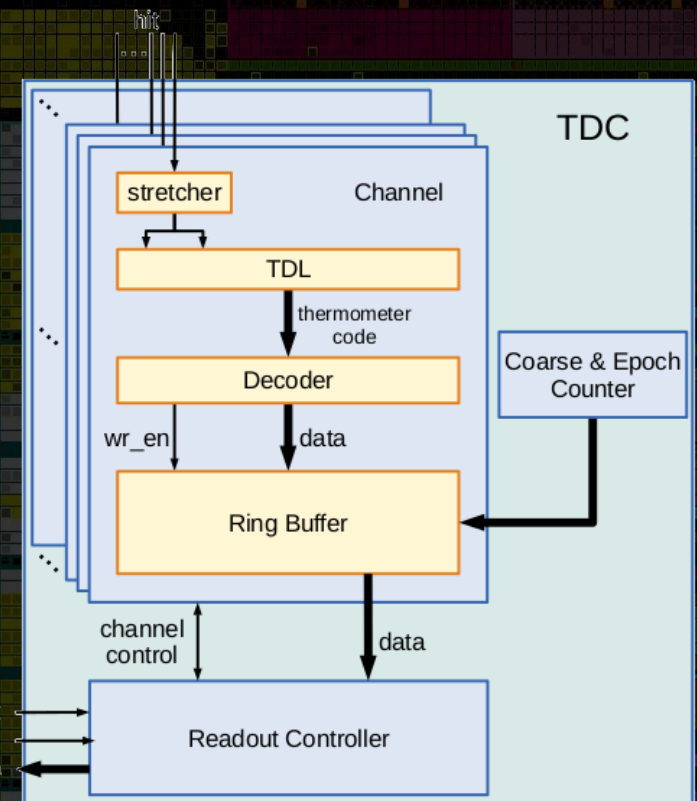
*Joint CBM / Panda DAQ Developments
"Kick-off" Meeting
19-20 February 2015, GSI*

Outline : TDC : Applications : Plans : Conclusion

- Outline
- TDC status – Single/Double Edge Measurements
- Applications
- Future Plans
- Conclusion & Outlook

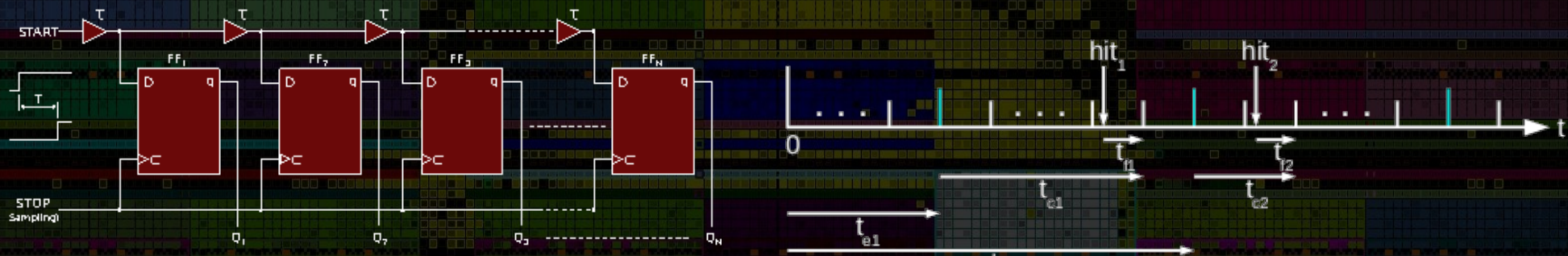
Outline : TDC : Applications : Plans : Conclusion

- Tapped Delay Line for fine time interpolator
- Coarse & Epoch counters for long measurement range
- Stretcher for short pulses & double edge
- Decoder: thermocode \rightarrow binary
- Ring buffer
- Calibration hits from an on-chip oscillator



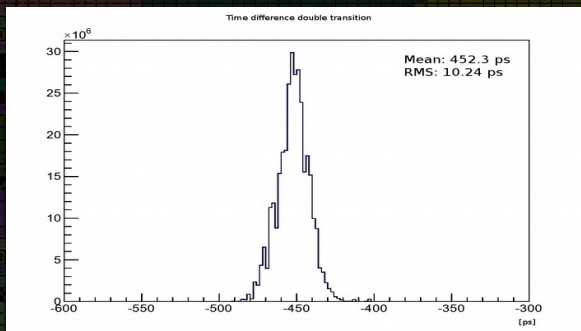
Simplified architecture of the TDC

Outline : TDC : Applications : Plans : Conclusion

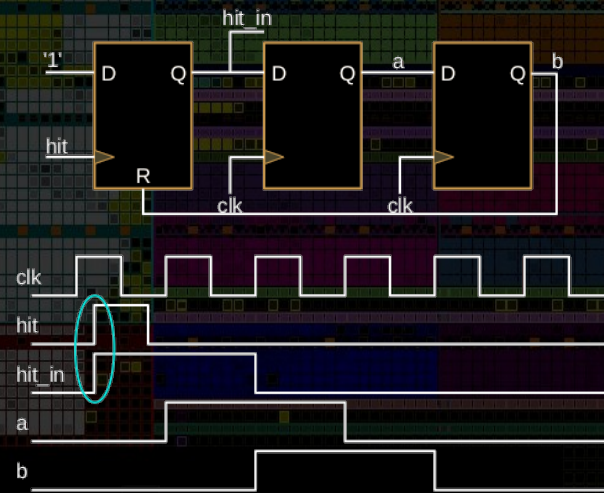


Tapped Delay Line method with common stop signal

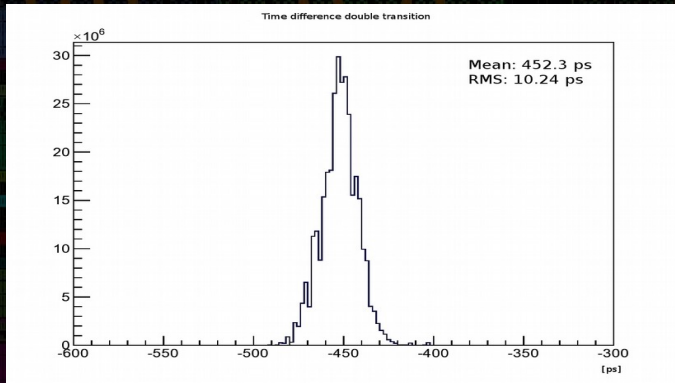
- $\Delta t = (t_{e2} + t_{c2} - t_{f2}) - (t_{e1} + t_{c1} - t_{f1})$
- RMS measured on two channel: ~10 ps
- Stretcher for short pulses (~500 ps)



Time precision test

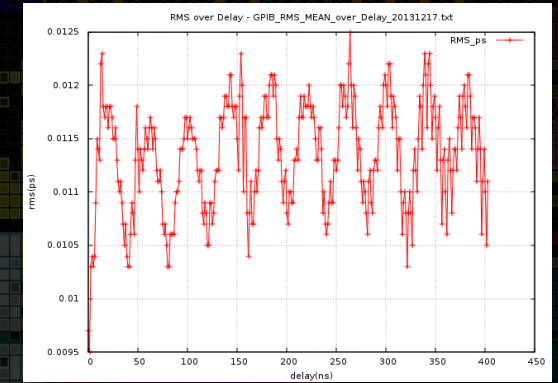


Outline : TDC : Applications : Plans : Conclusion



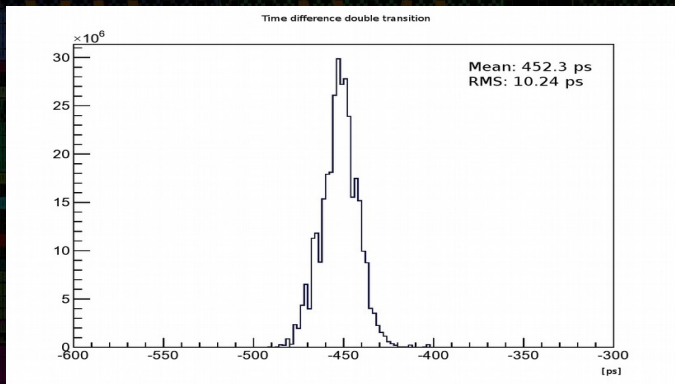
Time precision - ToF

Single edge measurement
RMS ~ 10 ps
 Δ RMS < 3 ps



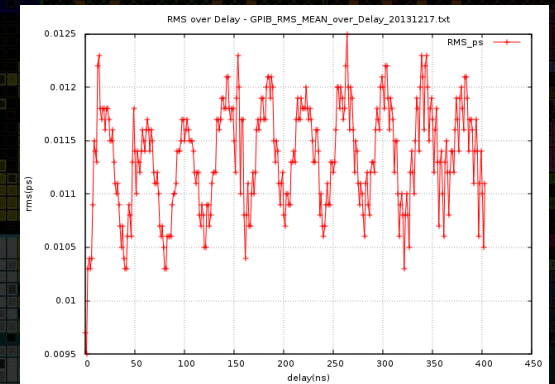
Precision vs mean

Outline : TDC : Applications : Plans : Conclusion



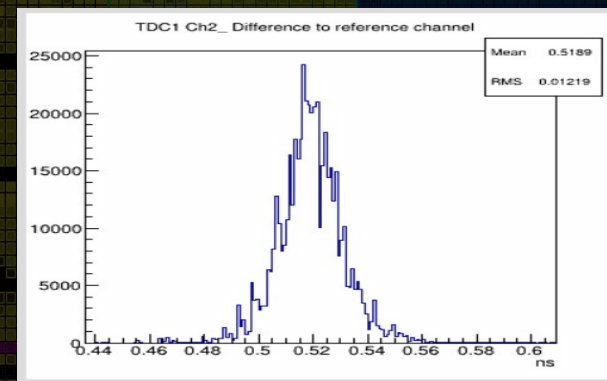
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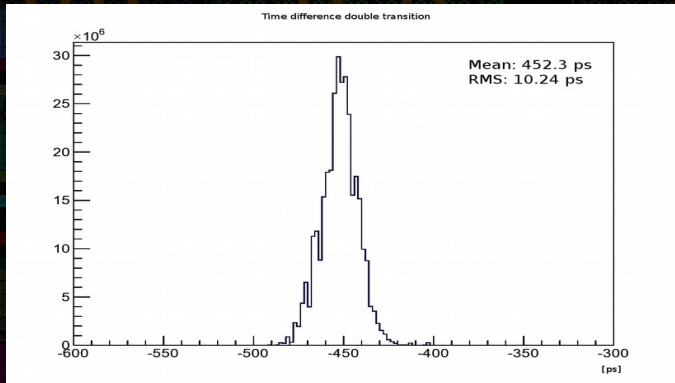
Precision vs mean

ToT measurement on 2 channels
Short pulse measurement



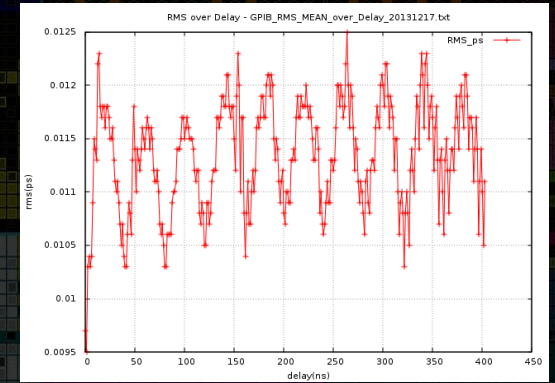
ToT on 2 channels

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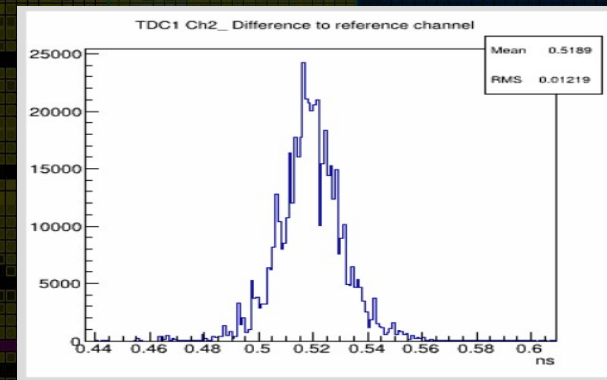
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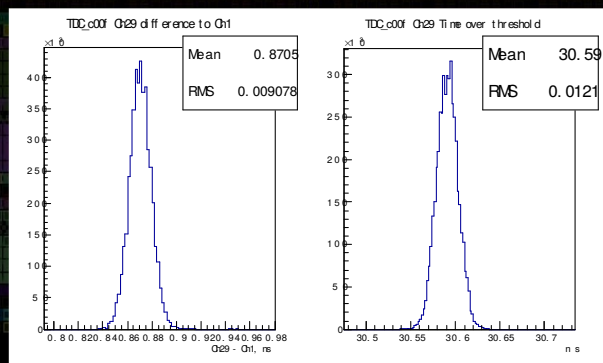


Precision vs mean

ToT measurement on 2 channels
Short pulse measurement



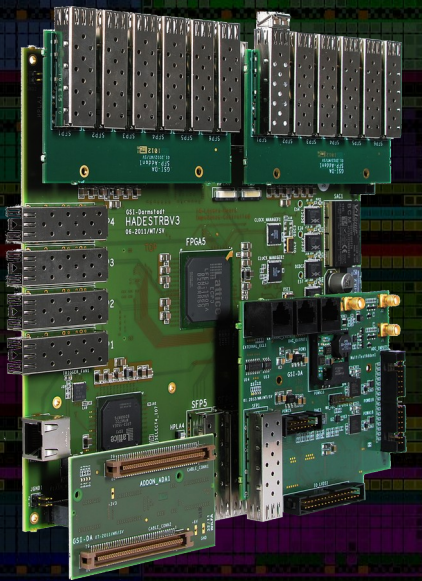
ToT on 2 channels



ToT on a single channel

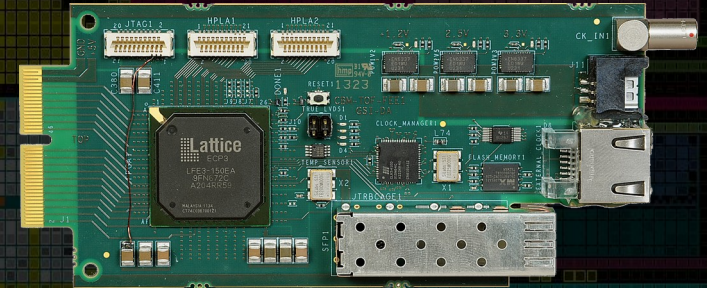
ToT measurement on a single channel

Outline : TDC : Applications : Plans : Conclusion



TRB3

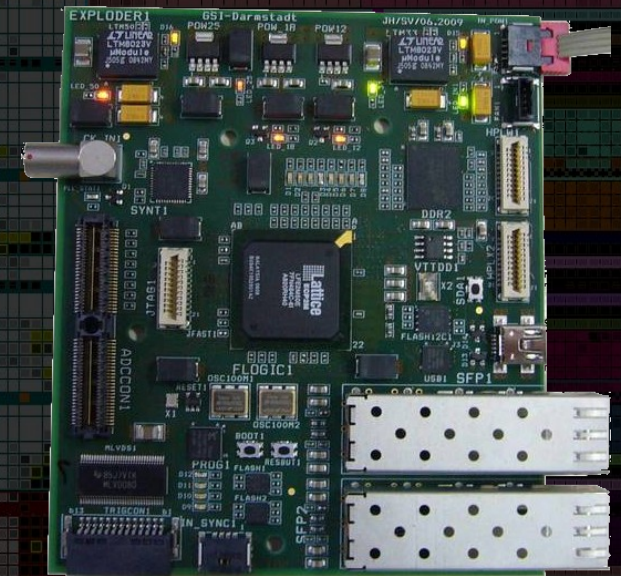
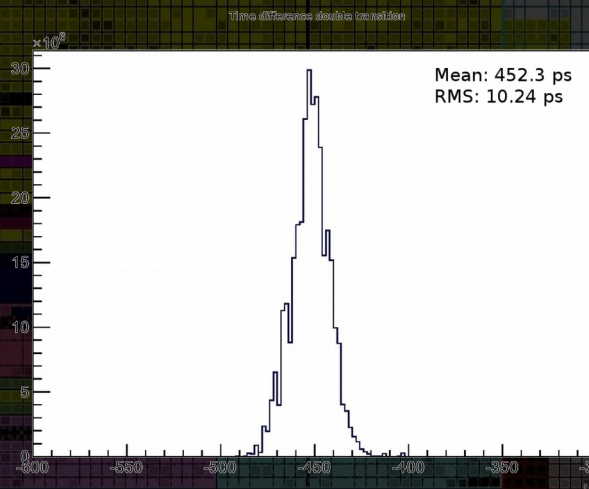
- TDC design is tested with 2 different Lattice FPGA families on 6 different boards with 2 different readout protocols
- Similar results are obtained from all of the devices
- No curve fittings or cuts are applied to the results
- The TDC can be adapted for ToF, ToT or Charge measurements



CbmTof & CbmRich



Febex3 & Tamex3

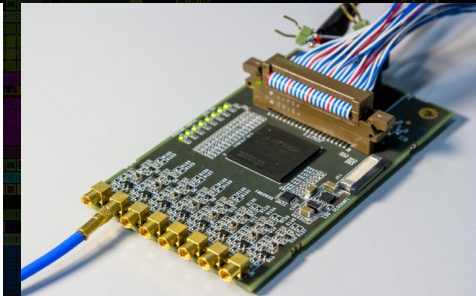
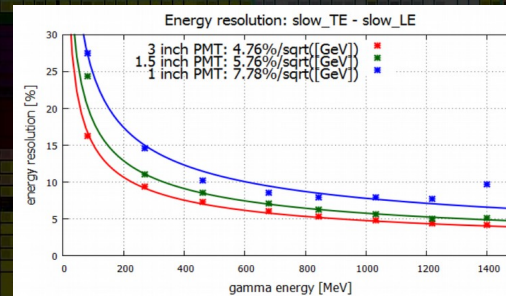


Febex2

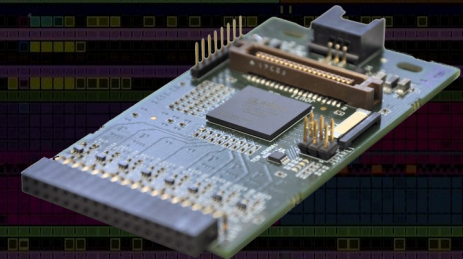
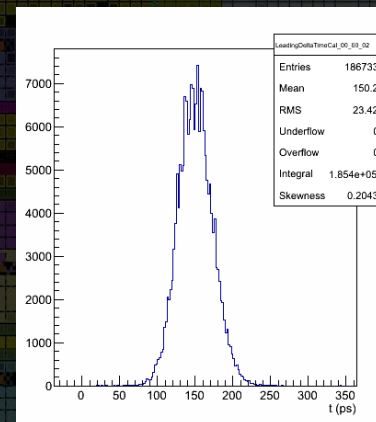
Outline : TDC : Applications : Plans : Conclusion

Tested with ...

- PaDiWa Amps for charge measurements
- Tested in lab with pulser and in gamma beam in Mainz (MAMI)
- Charge precision in lab: 0.5% (no walk correction)



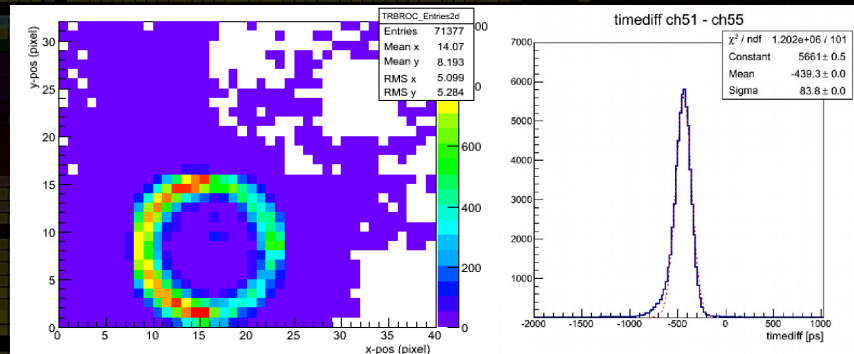
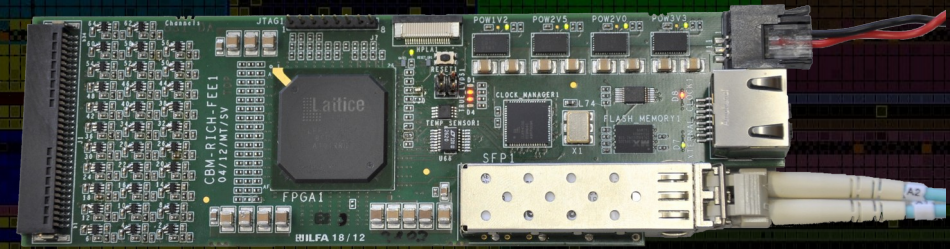
- PaDiWa FEE
- Pulser test: ~ 23 ps
- Single phototelectron laser test with MCP: ~ 70 ps



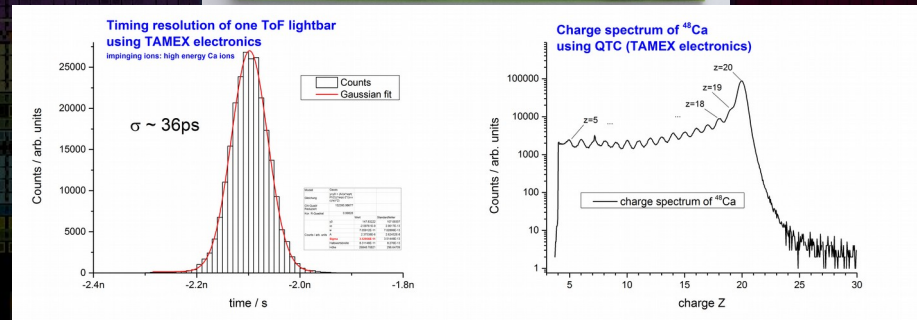
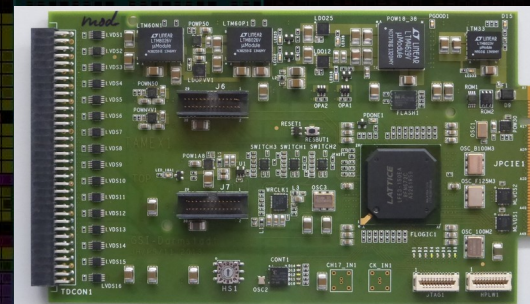
Outline : TDC : Applications : Plans : Conclusion

Tested with ...

- CBM-RICH in October 2012
- FEE + 65 Ch TDC
- 83ps RMS due to FEE design error



- TAMEX in September 2014
- Time (10ps) & Charge (0,9%) measurements
- Full detector precision 36ps



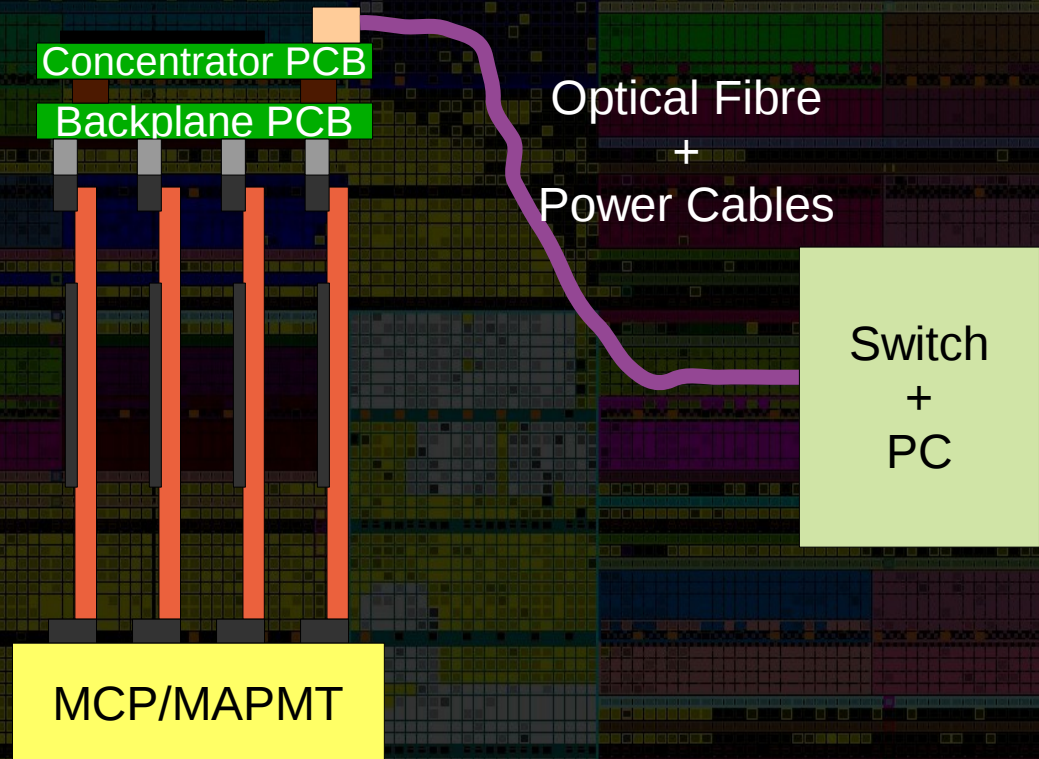
Outline : TDC : Applications : **Plans** : Conclusion

The plans are ...

- to finalise the tests of the double edge measurement in a single channel
- to increase the number of channels per FPGA (back) to 64
- to increase the TDC clock frequency to 240MHz (or better 360MHz) for a synchronous system – PANDA & CBM
- to implement TDC in the next generation Lattice FPGA ECP5 for the DIRICH board

Outline : TDC : Applications : Plans : Conclusion

- DIRC-RICH → DIRICH: Joint development of Panda-DIRC, CBM-RICH and HADES-RICH
- Padiwa + TDC
- Higher Integration needed to put TDC also on Padiwa
- We have to keep form factor → ECP3-150 too big
- New Lattice-FPGA available: ECP5-85F
 - 32 channels ToT, ~10ps precision TDC
 - Very good price: ~40€
 - 4 channels <3.2Gbps, 1.1V, 80mW static power
 - 17x17mm² for 381caBGA (same size as MachXO2)
 - All features needed



32 pin 2mm connector	<p>Low Power Amps</p> <ul style="list-style-type: none"> - 24dB - Currently: MMICS BGA2803 - 13mW/ch. 	<p>ECP5 FPGA</p> <ul style="list-style-type: none"> - Discriminator (LVDS inputs) - DACs for thresholds - High precision (~10ps RMS)TDC - DAQ via TRB-Net - <3Gbps-Transceivers - Scalers, etc. e.g. coincidence logic 	<p>Power Supply linear</p>
	<p style="writing-mode: vertical-rl; transform: rotate(180deg);"><=100 pin ERM5 connector</p>		

Outline : TDC : Applications : Plans : Conclusion

- Multi-purpose FPGA based TDC with 48 channels Precision $< 20\text{ps}$ RMS on all channels

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- 64 channels in single FPGA



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 - 64 channels in single FPGA
 - TDC @240MHz (or better 360MHz) for synchronous system – PANDA & CBM



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- Double edge detection in single TDC channel under tests, also in beamtime
- 64 channels in single FPGA
- TDC @240MHz (or better 360MHz) for synchronous system – PANDA & CBM
- TDC on DIRICH



TRB3 Community

Developers

Cahit Uğur	TDC
Jan Michel	TrbNet & DAQ
Grzegorz Korcyl	GbE
Manuel Penshuck	CTS
Michael Traxler	Organisation & Hardware
Ludwig Meier	Slow Control Software
Jörn Adamczewski-Musch	DAQ & Analysis
Sergey Linev	DAQ & Analysis
Matthias Hoek	Unpacking & Analysis

Active Users

Marek Pałka
Adrian Zink
PANDA DIRC Groups in Mainz & GSI
CBM RICH & CBM ToF

Christian Pauly
Andreas Neiser

PANDA Barrel DIRC
PANDA ToF
CBM – RICH
HADES MDC FEE
Mainz A2 Collaboration

Detector Groups

PANDA Disk DIRC
CBM Forward Calorimeter
CBM – ToF
HADES Calorimeter
Mainz Neutron Detector

Coimbra PET Scanner
ATLAS

and many more to come...



Thank you!

Backup Slides



JAGIELLONIAN
UNIVERSITY
IN KRAKÓW



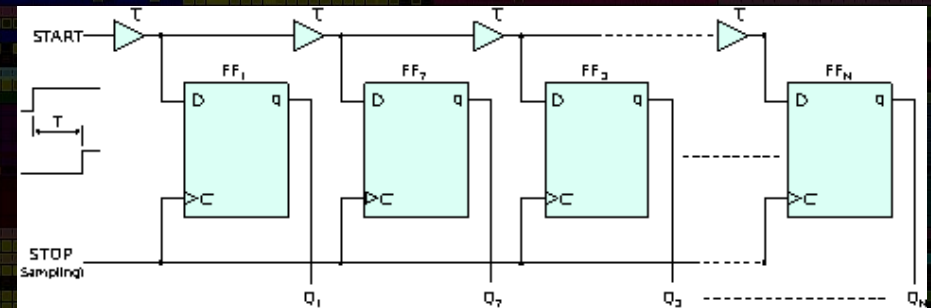
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MAINZ



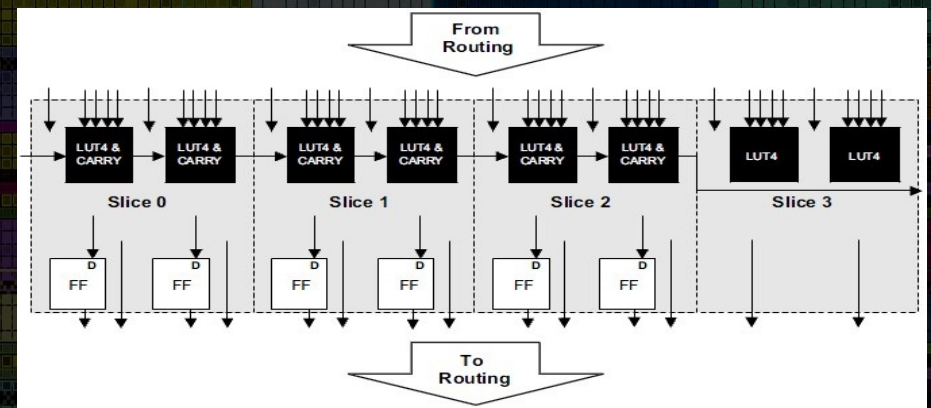
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FRANKFURT AM MAIN

Tapped Delay Line Method

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line



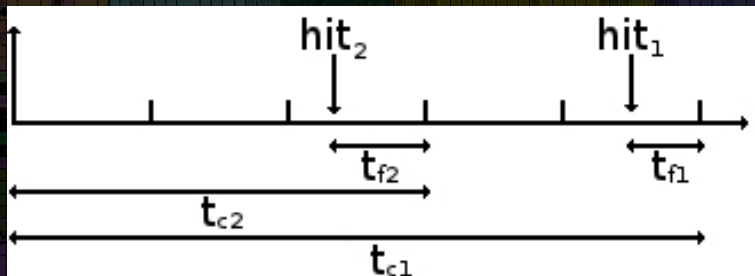
Tapped Delay Line Method



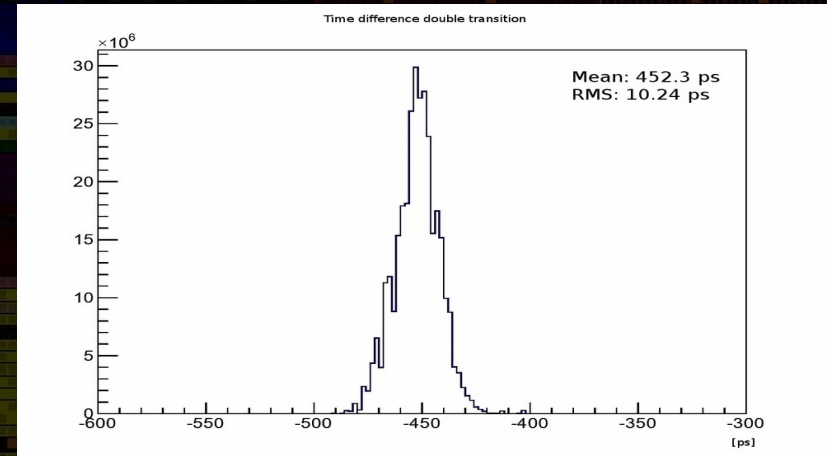
PFU Diagram

Laboratory Test Results

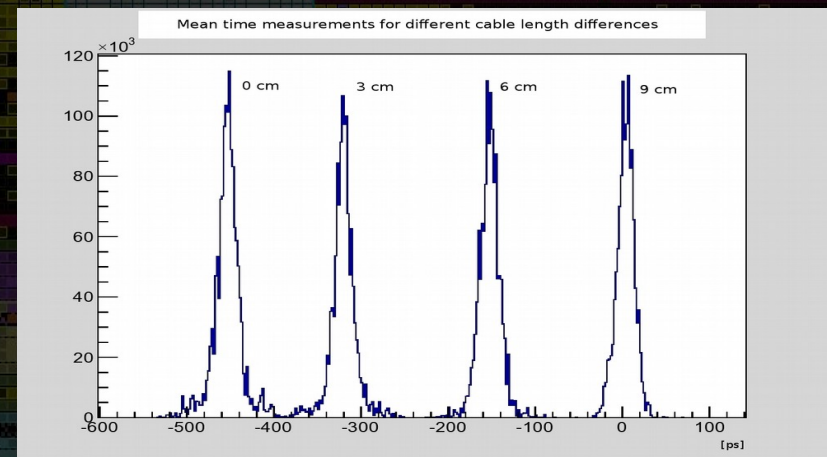
- Time difference measured between 2 channels
- $\Delta t = (t_{\text{coarse1}} - t_{\text{coarse2}}) - (t_{\text{fine1}} - t_{\text{fine2}})$
- RMS measured: 10.34 ps against the same clock
- Precision: $10.34 \text{ ps} / \sqrt{2} = 7.3 \text{ ps RMS}$



Time difference between two measurements

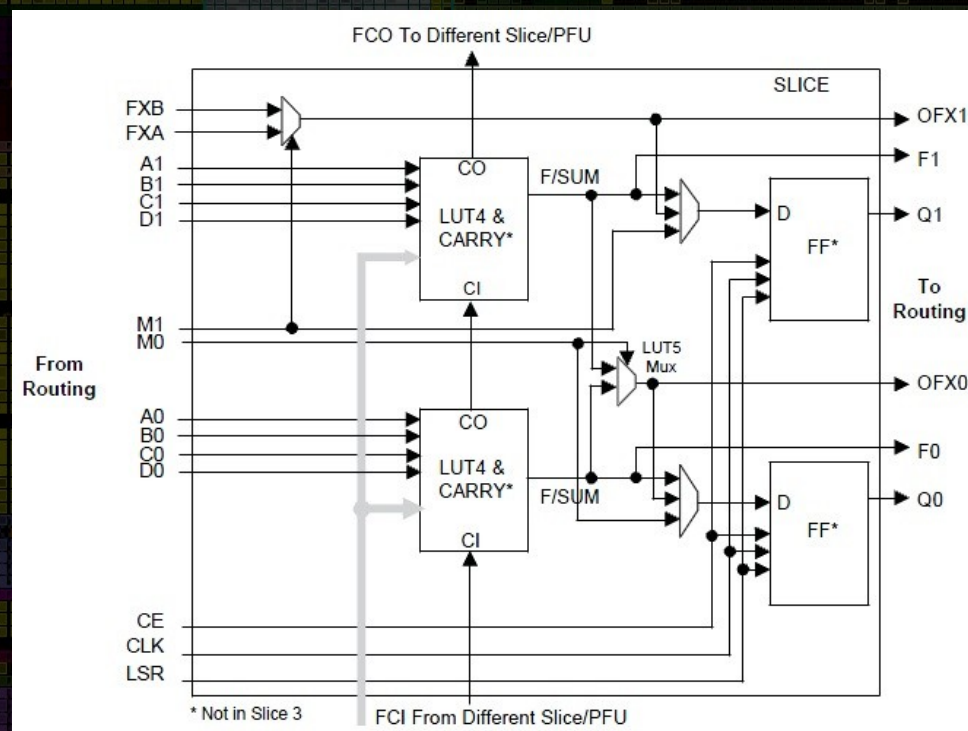
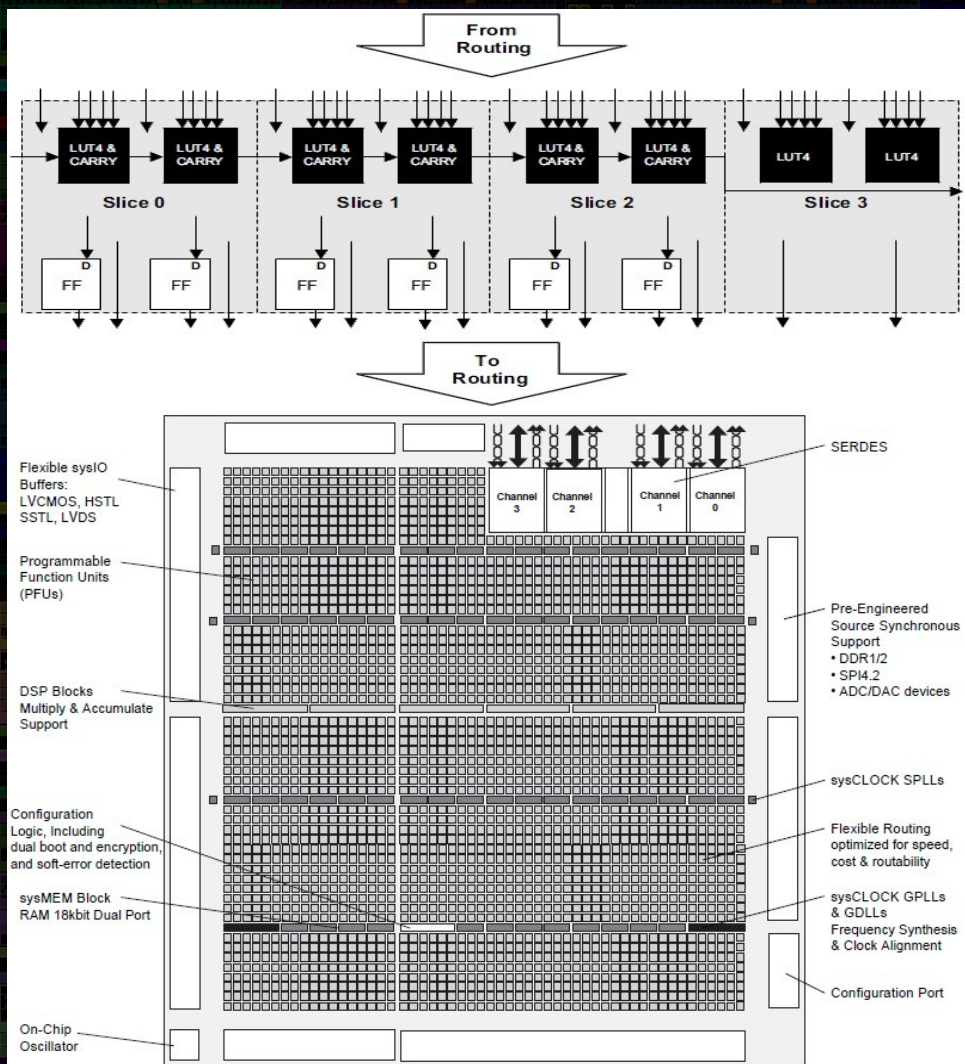


Time precision test



Mean measurement test

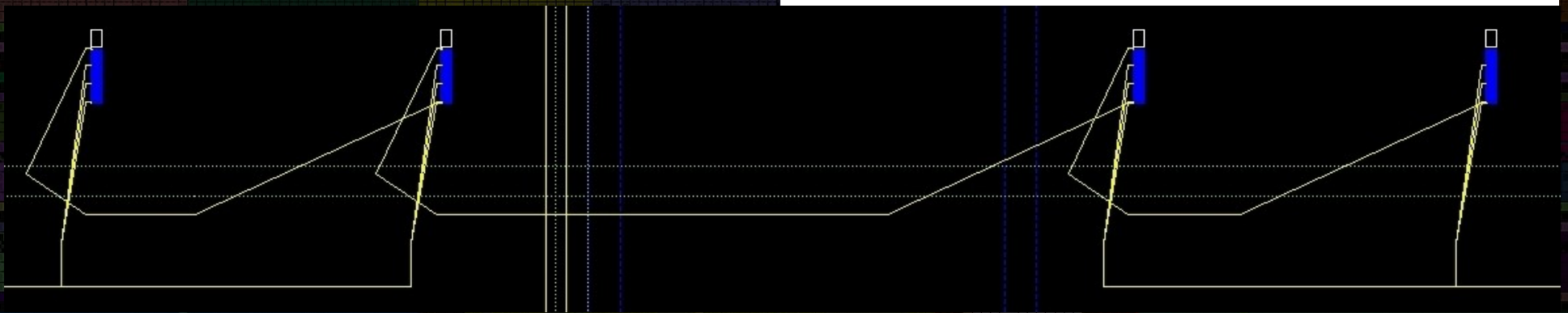
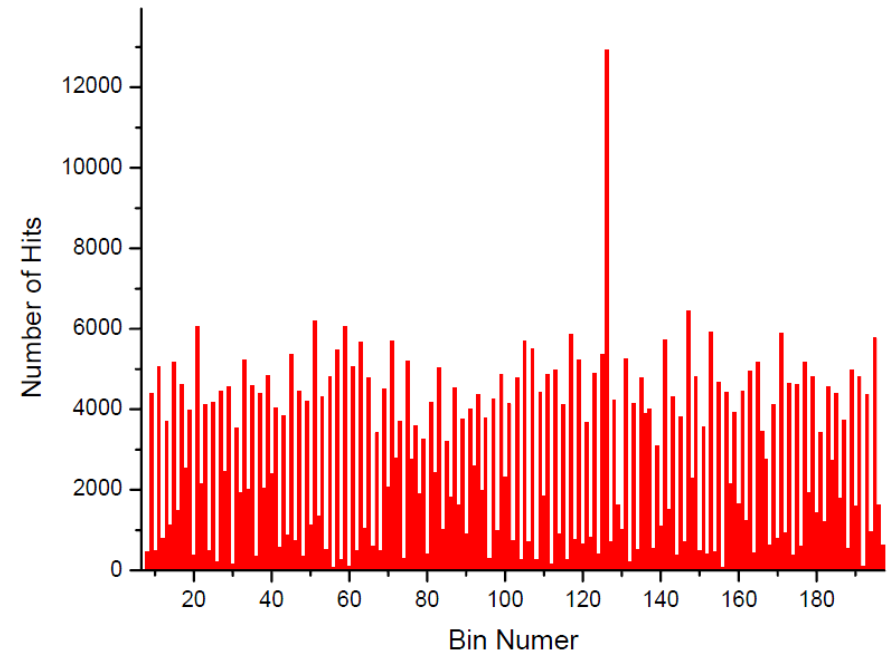
Architecture of TDC



Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floor-plan

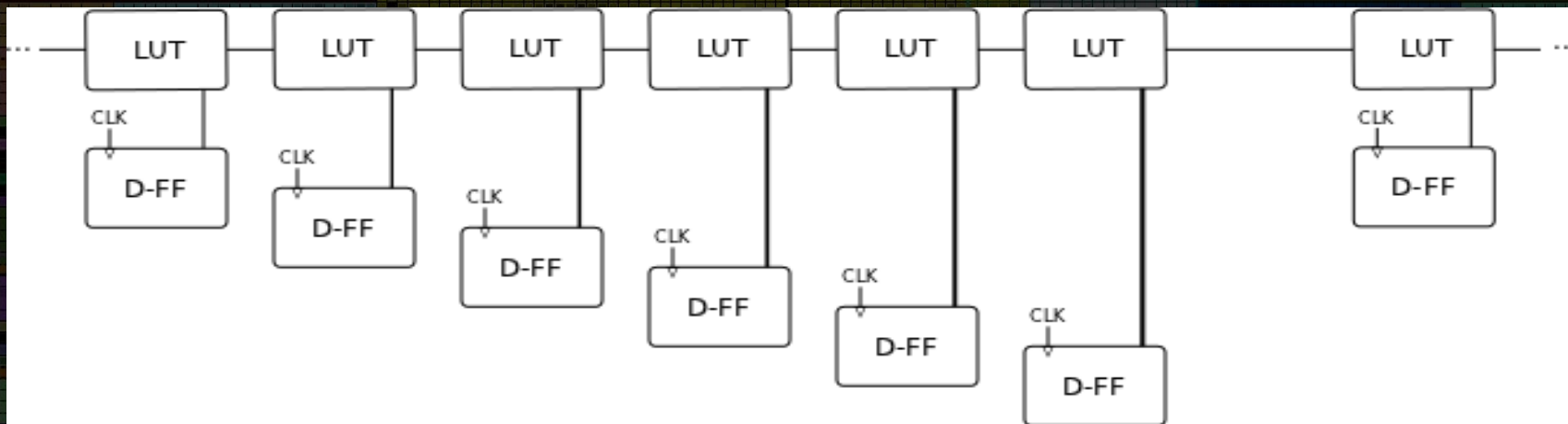
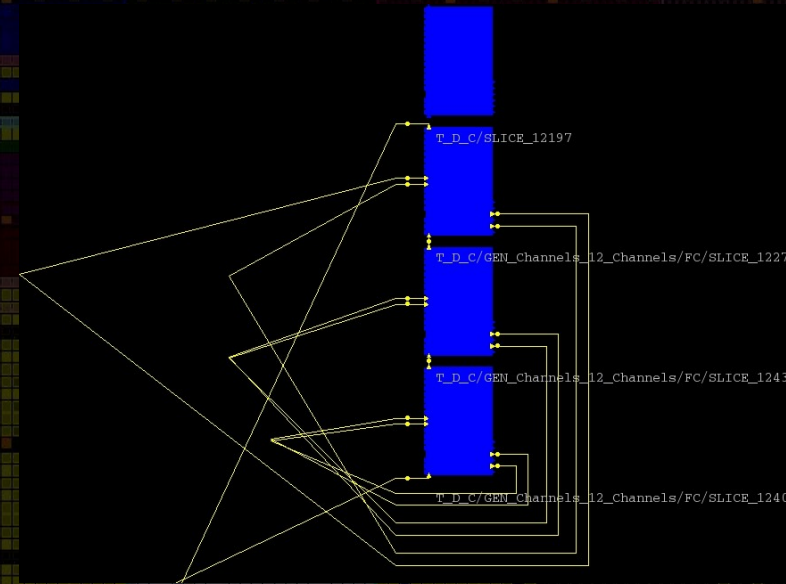
Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture



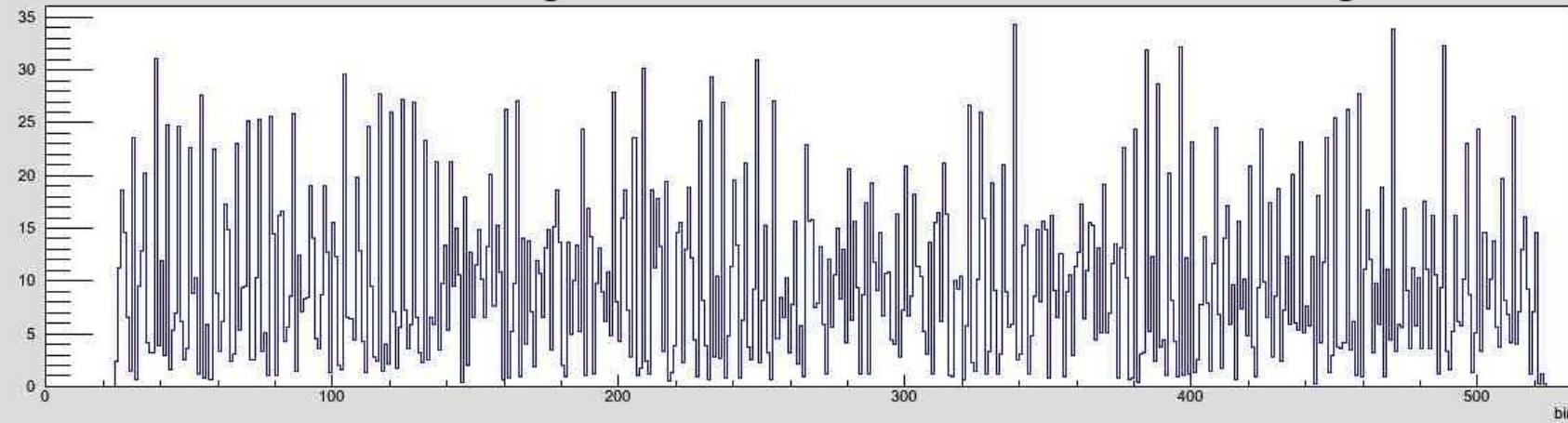
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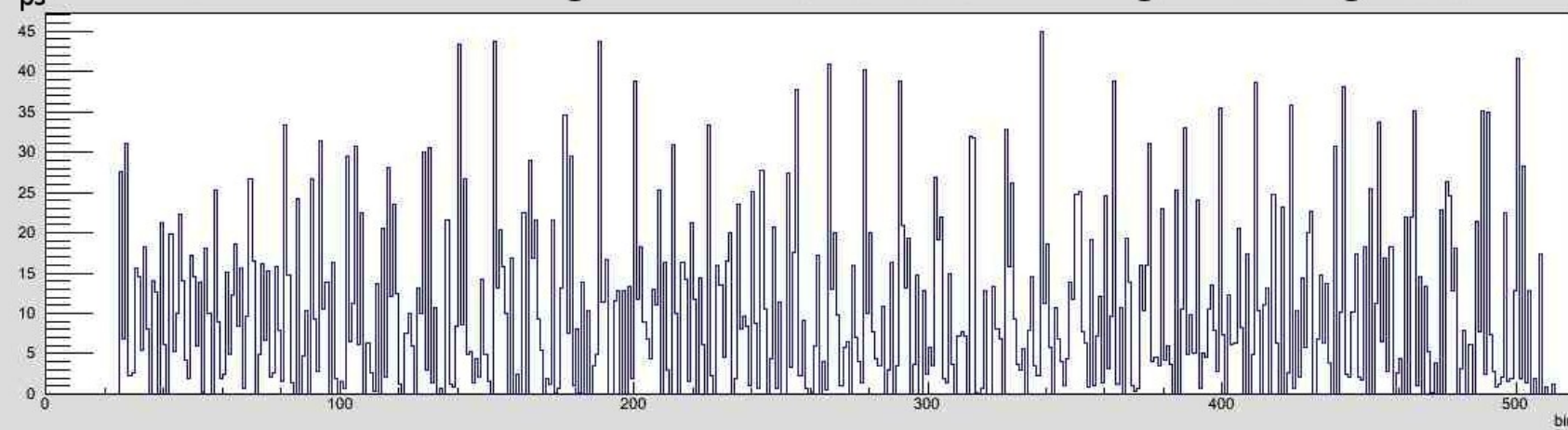
Architectural Effects of FPGA

ps Bin width histogram of a channel with shorter routings



Mean: ~10 ps
Max: ~35 ps

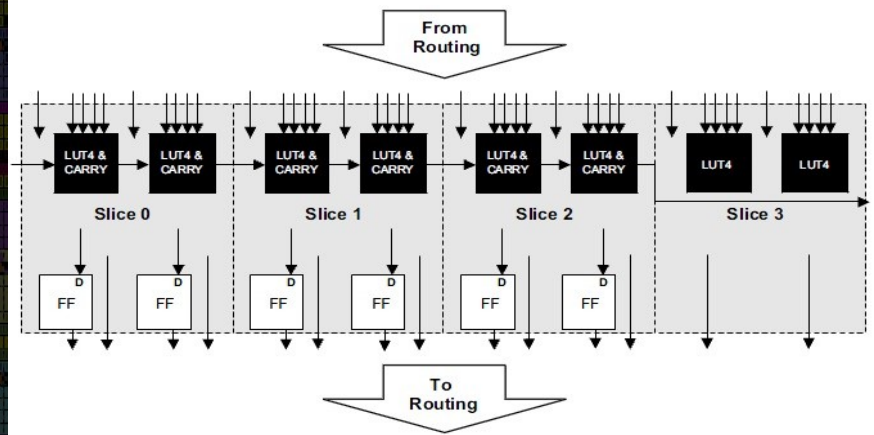
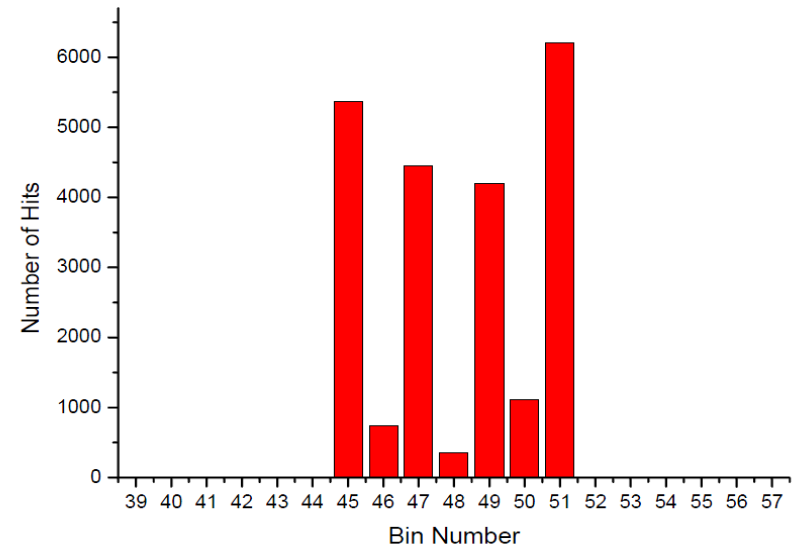
ps Bin width histogram of a channel with longer routings



Mean: ~15 ps
Max: ~45 ps

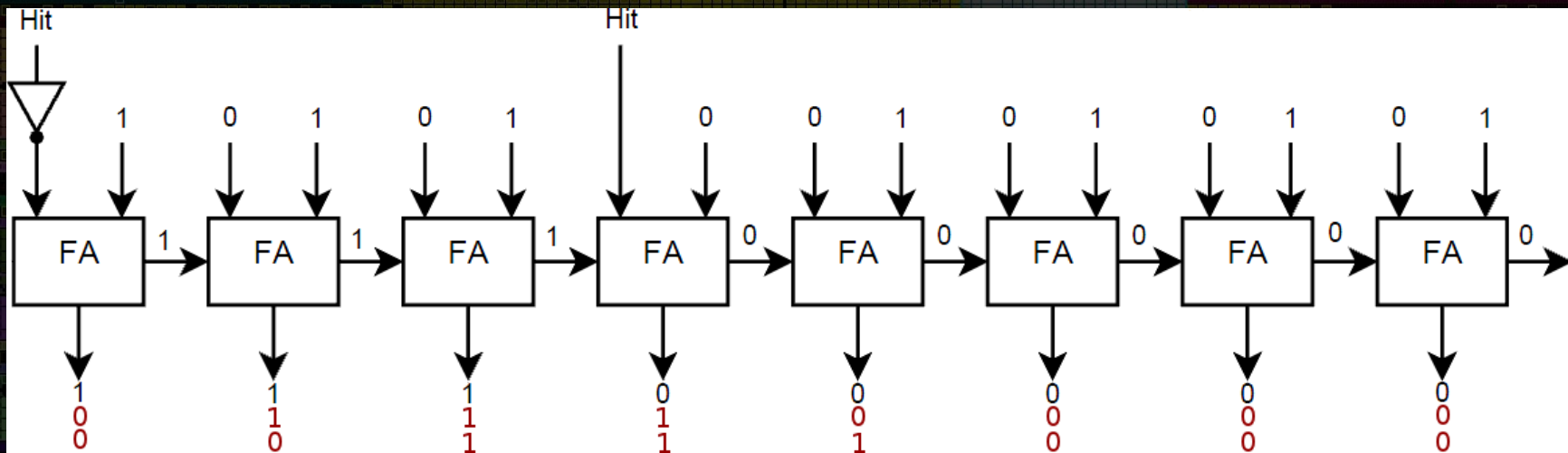
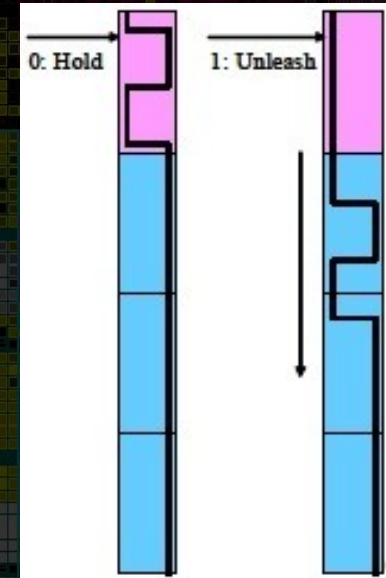
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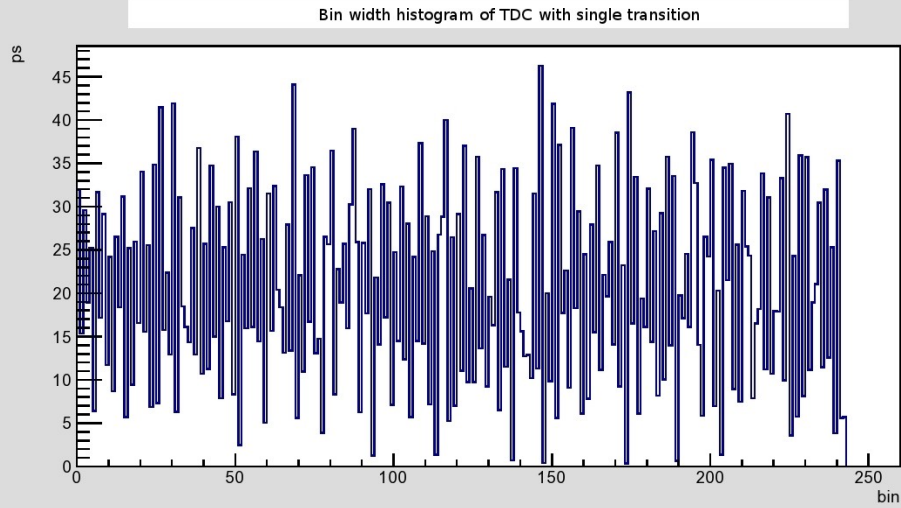
Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced

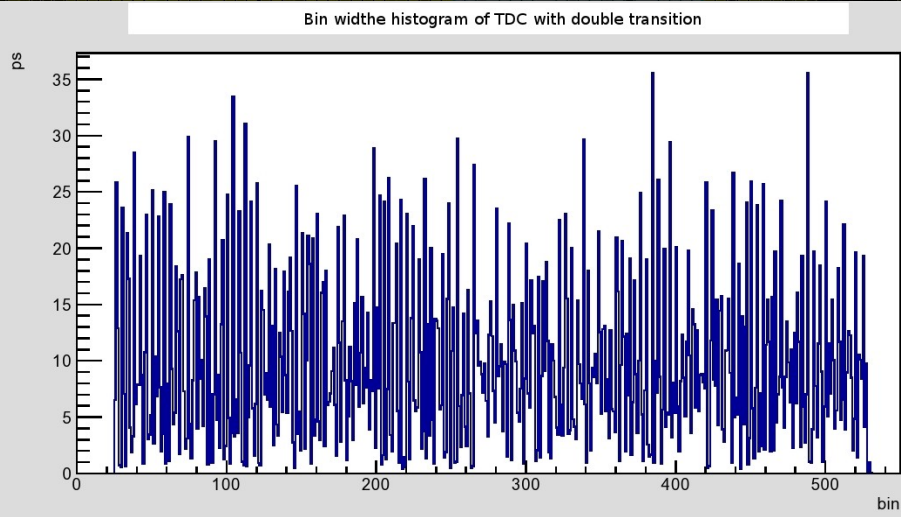


Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distribution



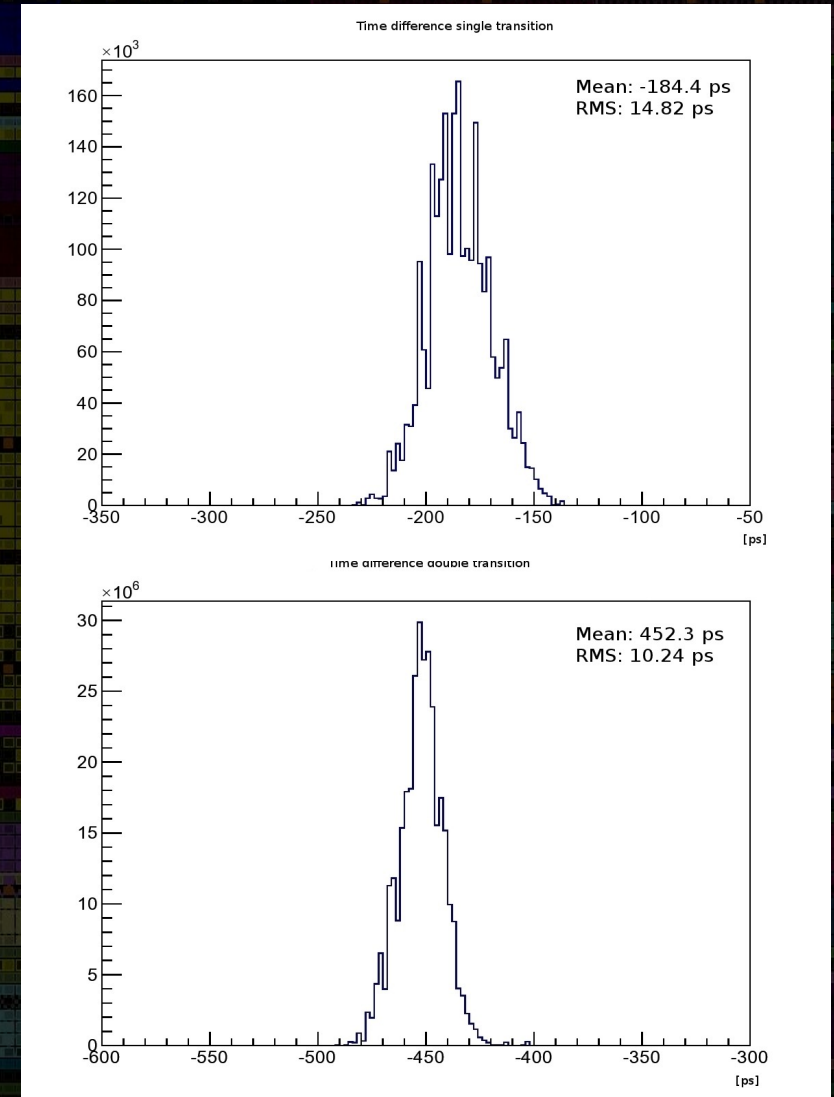
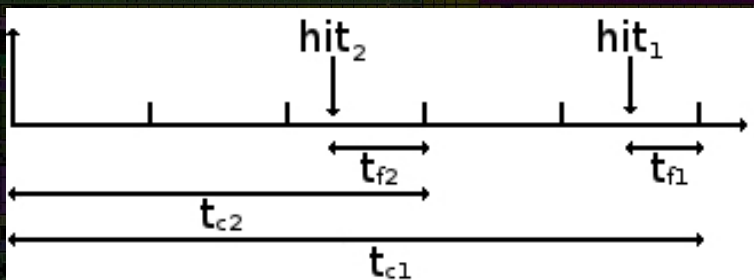
Bins: ~240
Mean: ~20 ps
Max: ~45 ps



Bins: ~520
Mean: ~10 ps
Max: ~35 ps

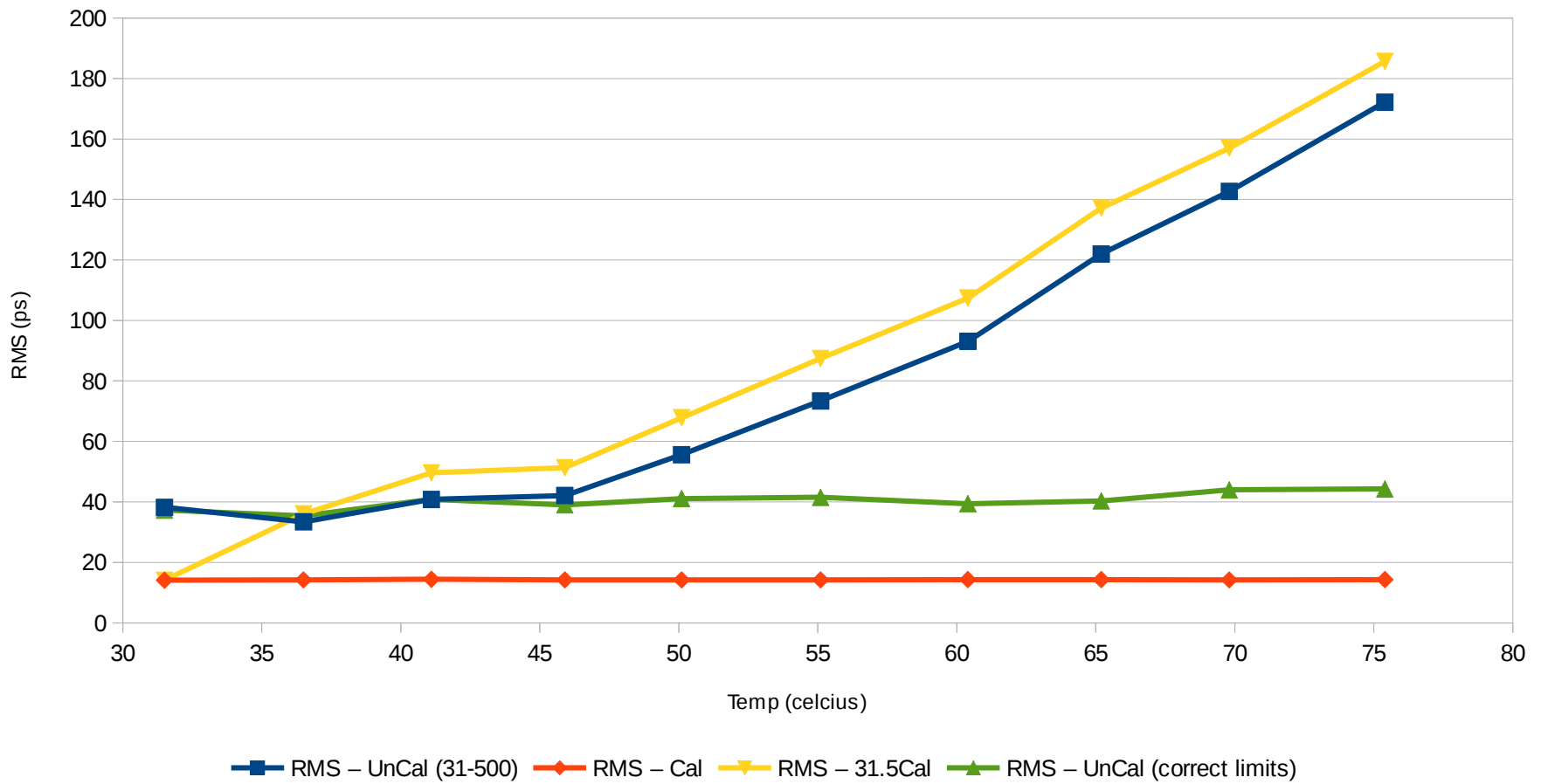
Statistical Error & Precision

- Time difference measured between 2 channels
- $\Delta t = (t_{\text{coarse1}} - t_{\text{coarse2}}) - (t_{\text{fine1}} - t_{\text{fine2}})$
- RMS measured: 10.34 ps
against same clock
- Precision: $10.34 \text{ ps} / \sqrt{2} = 7.3 \text{ ps}$
- Effect of 2 transitions:
 $14.82 \text{ ps} / 10.34 \text{ ps} = 1.43 \text{ factor}$



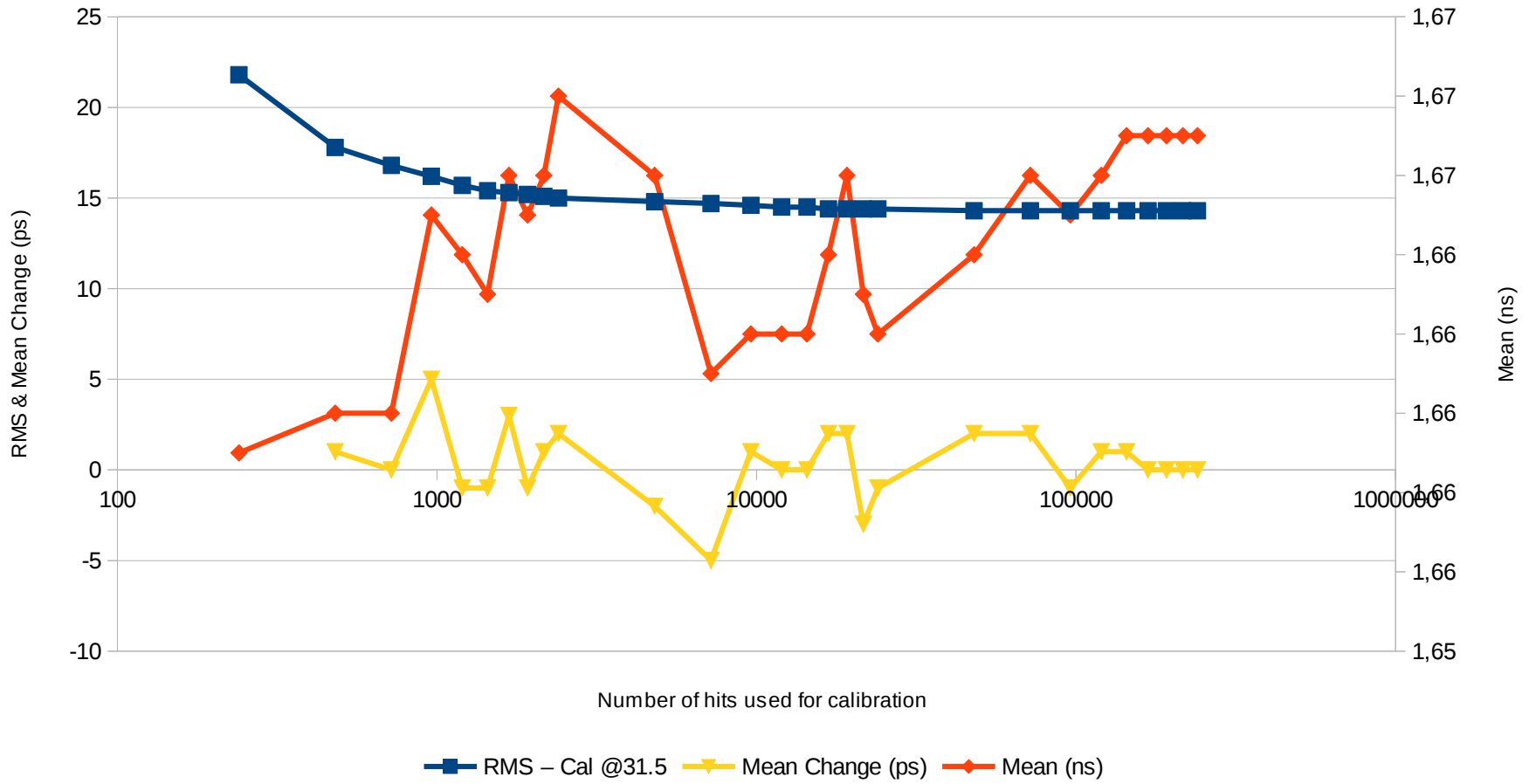
Precision vs Temperature

RMS vs Temperature



Precision & Mean vs Statistics

RMS - Mean vs Hit



Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

Central Trigger System

Status overview

Counter	Counts	Rate
Trigger asserted	398694099 clk.s	300.30 Kcnt/s
Trigger rising edges	398694099 edges	300.30 KHz
Trigger accepted	90048920 events	269.54 KHz

Last Idle Time: 1650 ns
Last Dead Time: 1680 ns, 595.24 KHz

Throttle: Limit Trigger Rate to 1 KHz
Full Stop: Ignore all events

Export CTS Configuration: as TrbCmd script as shell script

Trigger Channels

#	Enable	Trg. Cond.	Assignment	TrbNet Type	Asserted	Edges
0	<input type="checkbox"/>	R. Edge	Ext. Logic - CBM	Ox1_pysics_trigger	1370.38 cnt/s	124.58 Hz
1	<input checked="" type="checkbox"/>	R. Edge	Periodical Pulser 0	Ox1_pysics_trigger	300.30 Kcnt/s	300.30 KHz
2	<input type="checkbox"/>	R. Edge	Periodical Pulser 1	Ox1_pysics_trigger	25.00 Mcnt/s	25.00 MHz
3	<input type="checkbox"/>	R. Edge	Periodical Pulser 2	Ox1_pysics_trigger	0.00 cnt/s	0.00 Hz
4	<input type="checkbox"/>	R. Edge	Periodical Pulser 3	Ox1_pysics_trigger	0.00 cnt/s	0.00 Hz
5	<input type="checkbox"/>	R. Edge	Random Pulser 0	Ox1_pysics_trigger	149.76 Kcnt/s	149.51 KHz
6	<input type="checkbox"/>	R. Edge	Trigger Input 0	Ox1_pysics_trigger	20.00 Mcnt/s	125.56 Hz
7	<input type="checkbox"/>	R. Edge	Trigger Input 1	Ox1_pysics_trigger	0.00 cnt/s	0.00 Hz
8	<input type="checkbox"/>	R. Edge	Trigger Input 2	Ox1_pysics_trigger	269.54 Kcnt/s	269.54 KHz
9	<input type="checkbox"/>	R. Edge	Trigger Input 3	Ox1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
10	<input type="checkbox"/>	R. Edge	Coincidence Module 0	Ox1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
11	<input type="checkbox"/>	R. Edge	Coincidence Module 1	Ox1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
12	<input type="checkbox"/>	R. Edge	Coincidence Module 2	Ox1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
13	<input type="checkbox"/>	R. Edge	Coincidence Module 3	Ox1_pysics_trigger	100.00 Mcnt/s	0.00 Hz

Trigger Input Configuration and Coincidence Detectors

Input Modules					Coincidence Detectors				
#	Inp. Rate	Invert	Delay	Spike Rej.	Override	#	Window	Coin Mask (3:0)	Inhibit Mask (3:0)
0	125.56 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	0	100 ns	<input type="checkbox"/>	<input type="checkbox"/>
1	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	1	100 ns	<input type="checkbox"/>	<input type="checkbox"/>
2	269.54 KHz	<input type="checkbox"/>	0 ns	0 ns	bypass	2	100 ns	<input type="checkbox"/>	<input type="checkbox"/>
3	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	bypass	3	100 ns	<input type="checkbox"/>	<input type="checkbox"/>

Pulsers

Periodical Pulsers			Random Pulsers	
#	Low-Period	Frequency	#	Mean Frequency
0	8.32 us	301.20 Kcnt/s	0	150 KHz
1				
2				
3				

Three input formats are supported:
1) Enter the duration of the low-period in clock cycles by omitting a unit
2) Enter the duration of the low-period in seconds by adding "s"
3) Enter the frequency by appending "Hz"

Optional unit prefixes: n, u, m, k/K, M, g/G. Example 1ms = 1e-3s, 1 Ms = 1e3s
Press enter or leave input do apply values. This might take a few moments and is completed as soon as the left column has changed

CTS Details

Readout config: 21

<input type="checkbox"/> Trigger Channel Counter	Design compiled	Thu, 15 Nov 2012 20:08:02
<input type="checkbox"/> Idle/Dead Counter	TD FSM State	TD FSM_WAIT_TRIGGER_BECOME_IDLE
<input type="checkbox"/> Trigger statistics	RO FSM State	RO FSM_WAIT_BECOME_IDLE
<input type="checkbox"/> Timestamp	RO Queue	Active, words enqueued: 43
TD FSM Limit (debug only): disabled	Current Trigger (15:0)	0011 1110 0100 0000, Not asserted
RO FSM Limit (debug only): disabled	Buffered Trigger (15:0)	0011 1110 0100 0110, Type: 0x1

- Extendible and modular structure
- Master and slave mode operation
- Up to 16 independent trigger modules
- 4 channel TDC for trigger time
- 8 general purpose trigger inputs
- Coincidence detection
- Periodic & Random pulser
- On-board and off-board trigger distribution
- Trigger generation from TDC channel inputs
- Tested successfully during the CBM and PANDA test beams with slave and master modes

Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

Hit Counters & TDC Registers

Configuration

Board: **mb**

Fiber: **0**

of Channels: **0**

Update Interval (ms): **1000**

Start Value: **0**

Differences: **0**

Input Status/Enable: **0**

Reg	Channel	Q01	Q02	Q03	Q04	Reg	Channel	Q01	Q02	Q03	Q04
c000	0	0	0	0	0	c100	0	0	0	0	0
c001	1	0	0	0	0	c101	1	0	0	0	0
c002	2	0	0	0	0	c102	2	0	0	0	0
c003	3	0	0	0	0	c103	3	0	0	0	0
c004	4	0	0	0	0	c104	4	0	0	0	0
c005	5	0	0	0	0	c105	5	0	0	0	0
c006	6	0	0	0	0	c106	6	0	0	0	0
c007	7	0	0	0	0	c107	7	0	0	0	0
c008	8	0	0	0	0	c108	8	0	0	0	0
c009	9	0	0	0	0	c109	9	0	0	0	0
c00a	10	0	0	0	0	c10a	10	0	0	0	0
c00b	11	0	0	0	0	c10b	11	0	0	0	0
c00c	12	0	0	0	0	c10c	12	0	0	0	0
c00d	13	0	0	0	0	c10d	13	0	0	0	0
c00e	14	0	0	0	0	c10e	14	0	0	0	0
c00f	15	0	0	0	0	c10f	15	0	0	0	0
c010	16	0	0	0	0	c110	16	0	0	0	0
c011	17	0	0	0	0	c111	17	0	0	0	0
c012	18	0	0	0	0	c112	18	0	0	0	0
c013	19	0	0	0	0	c113	19	0	0	0	0
c014	20	0	0	0	0	c114	20	0	0	0	0
c015	21	0	0	0	0	c115	21	0	0	0	0
c016	22	0	0	0	0	c116	22	0	0	0	0
c017	23	0	0	0	0	c117	23	0	0	0	0
c018	24	0	0	0	0	c118	24	0	0	0	0
c019	25	0	0	0	0	c119	25	0	0	0	0
c01a	26	0	0	0	0	c11a	26	0	0	0	0
c01b	27	0	0	0	0	c11b	27	0	0	0	0
c01c	28	0	0	0	0	c11c	28	0	0	0	0
c01d	29	0	0	0	0	c11d	29	0	0	0	0
c01e	30	0	0	0	0	c11e	30	0	0	0	0
c01f	31	0	0	0	0	c11f	31	0	0	0	0
c020	32	0	0	0	0	c120	32	0	0	0	0
c021	33	0	0	0	0	c121	33	0	0	0	0
c022	34	0	0	0	0	c122	34	0	0	0	0
c023	35	0	0	0	0	c123	35	0	0	0	0
c024	36	0	0	0	0	c124	36	0	0	0	0
c025	37	0	0	0	0	c125	37	0	0	0	0
c026	38	0	0	0	0	c126	38	0	0	0	0

TDC readout & channel monitoring & control

Threshold Settings

Configuration

Board: **mb**

DAC-Chain: **0**

Channel: **0**

Board Type: **FPGA**

Update Interval (ms): **1000**

Reference (mV): **500**

OK

Coarse (0-65535): **13354**

Fine (0-255): **128**

13482 - 514.3 mV

Threshold setting

Central Trigger System

Status overview

Counter: 39859409 counts, 300.30 KHz, 360000

Trigger asserted: 39859409 edges, 300.30 KHz, 200000

Trigger accepted: 39046920 events, 299.94 KHz, 200000

Last Life Time: 1650 ns

Last Dead Time: 1650 ns, 595.24 KHz

Throttle: Limit Trigger Rate to KHz

Full Stop: ignore all events

Export CTS Configuration: as TiNet script or as shell script

Trigger Channels

#	Enable	Trig. Cond.	Assignment	TiNet Type	Asserted	Edges
0	<input type="checkbox"/>	<input type="checkbox"/>	Ext. Logic - CDM	Ext. Logic - CDM	1070.58 counts	124.50 KHz
1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Periodical Pulser 0	Ext. Logic - CDM	300.30 KHz	300.30 KHz
2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Periodical Pulser 1	Ext. Logic - CDM	25.00 Mcnts/s	25.00 MHz
3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Periodical Pulser 2	Ext. Logic - CDM	0.00 cnts/s	0.00 Hz
4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Periodical Pulser 3	Ext. Logic - CDM	0.00 cnts/s	0.00 Hz
5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Random Pulser 0	Ext. Logic - CDM	149.75 KHz	149.51 KHz
6	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Trigger Input 0	Ext. Logic - CDM	20.00 Mcnts/s	125.56 KHz
7	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Trigger Input 1	Ext. Logic - CDM	0.00 cnts/s	0.00 Hz
8	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Trigger Input 2	Ext. Logic - CDM	209.54 KHz	209.54 KHz
9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Trigger Input 3	Ext. Logic - CDM	100.00 Mcnts/s	0.00 Hz
10	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Coincidence Module 0	Ext. Logic - CDM	100.00 Mcnts/s	0.00 Hz
11	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Coincidence Module 1	Ext. Logic - CDM	100.00 Mcnts/s	0.00 Hz
12	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Coincidence Module 2	Ext. Logic - CDM	100.00 Mcnts/s	0.00 Hz
13	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Coincidence Module 3	Ext. Logic - CDM	100.00 Mcnts/s	0.00 Hz

Trigger Input Configuration and Coincidence Detectors

#	Imp. Rate	Invert	Delay	Spike Rej.	Override	# Window	Coincidence Detectors	Coin Mask (E0)	Inhibit Mask (E0)
0	125.56 Hz	<input type="checkbox"/>	0 ns	0 ns	System 2	0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
1	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	System 2	1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	209.54 KHz	<input type="checkbox"/>	0 ns	0 ns	System 2	2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	0.00 Hz	<input type="checkbox"/>	0 ns	0 ns	System 2	3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Pulsers

#	Low-Period	Frequency	#	Random Pulsers	Mean Frequency
0	332 ns	301.20 KHz	0	0	100 kHz
1					
2					
3					

CTS Details

Readout config:

Optional unit prefixes: **n, u, m, M, G, T**. Example $1ms = 1e-3s$, $1Ms = 1e3s$. Press enter or leave input do apply values. This might take a few moments until is completed as soon as the left column has changed.

Design compiled: Thu, 15 Nov 2012 20:08:02

Idle/Dead Counter

Trigger statistics

Timestamp

TD FSM Limit (debug only): **enabled**

RO FSM Limit (debug only): **enabled**

TD FSM State: **TD_FSM_WAIT_TRIGGER_BECOME_IDLE**

RO FSM State: **RO_FSM_WAIT_BECOME_IDLE**

Current Trigger (15.0): **0011 1110 0100 0000**. Not asserted

Buffered Trigger (15.0): **0011 1110 0100 0010**. Type: 0x1

Trigger processing & control

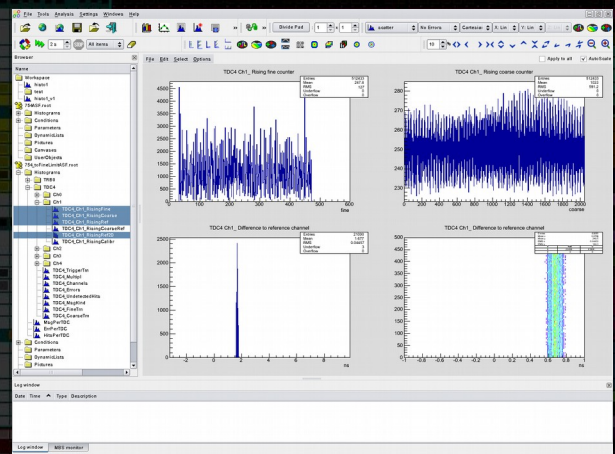
```

# tbcflash program 0xf48 .../bitfiles/tbcl_periph_padiwa_20130321.bit
Found 4 Endpoint(s) of group TRB3 PERIPHERAL FPGA
NAME: trb3_periph_padiwa_20130321.bit
DATE: Thu Mar 21 12:47:22 2013
USER:
Start programming ImageFile './bitfiles/trb3_periph_padiwa_20130321.bit'
You decided to reprogram the FlashMem(s) of TRB3 PERIPHERAL FPGA, are you sure (N,y,y)
Programming Endpoint(s) @ Address 0xf48
Symbols:
E: Erasing
P: Programming
S: Success
.: Skipped

Block: 0 1 2 3 4 5 6 7 8 9 A B C D E F
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
6 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
8 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
B 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
C 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
D 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
E 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
F 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Success
    
```

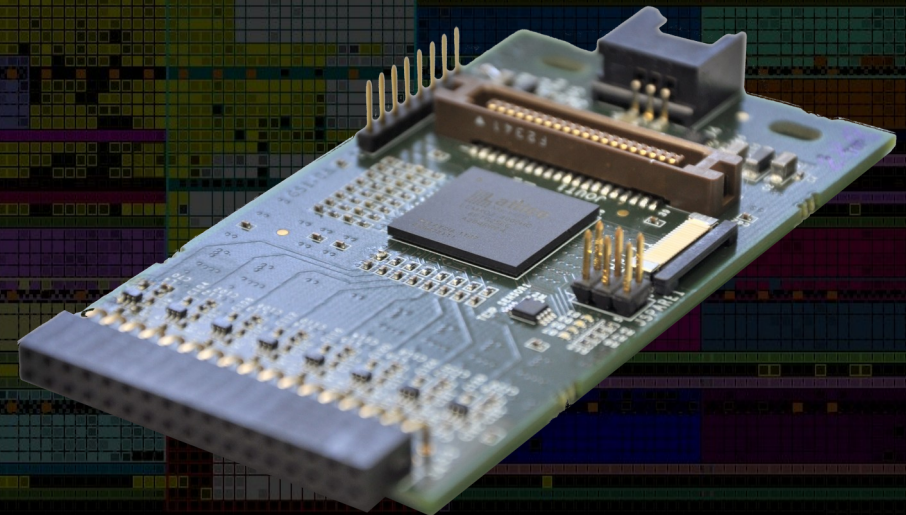
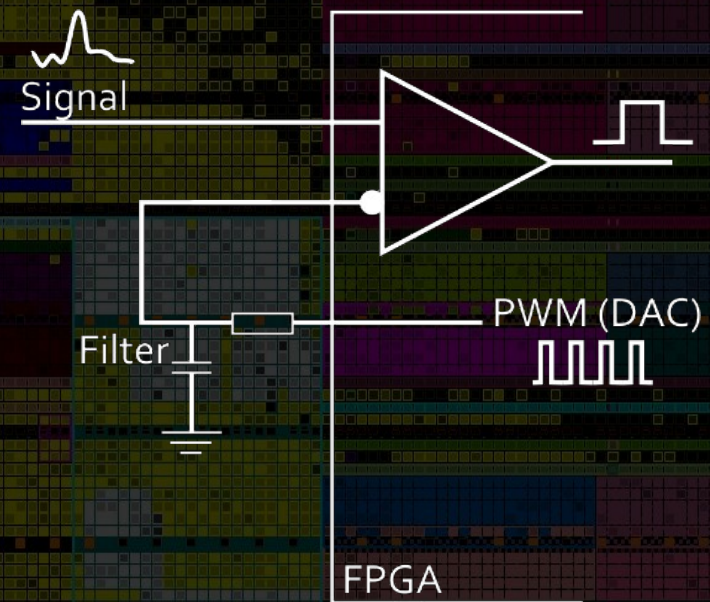
Console based slow control software with many features



Unpacking & Online Analysis & DAQ

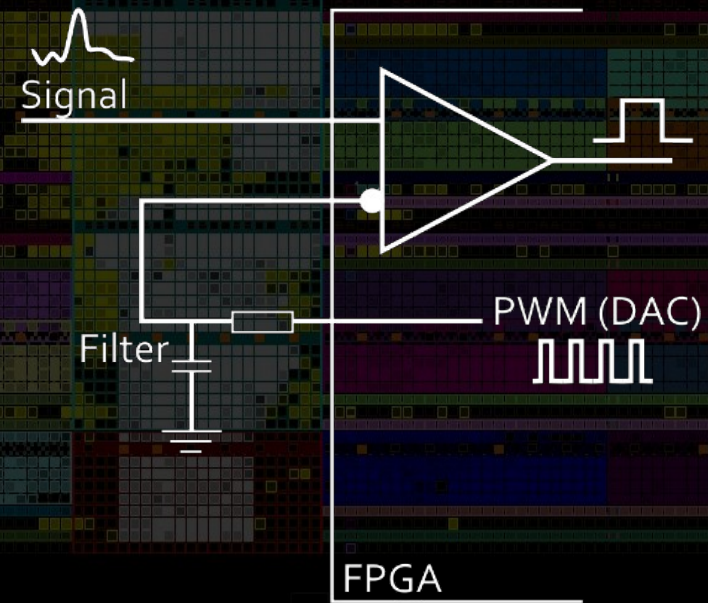
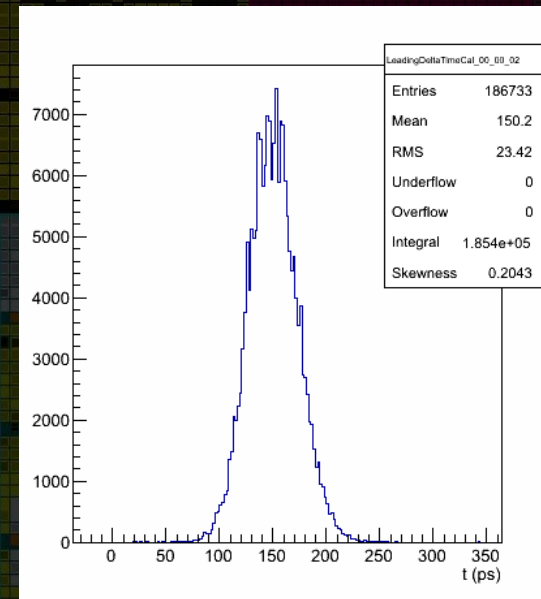
Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

- Pre-amplified with commercial amplifiers (MMICs)
- Input LVDS buffers in FPGAs are used as discriminators – Lattice MachXO2
- The leading edge time and Time over Threshold is encoded in the digital pulse
- The thresholds are set by FPGA via PWM and low pass filter
- FEE is placed directly at the detector, only digital signals are sent out
- Time measurements are done by TDCs implemented in FPGA (TRB3)



Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

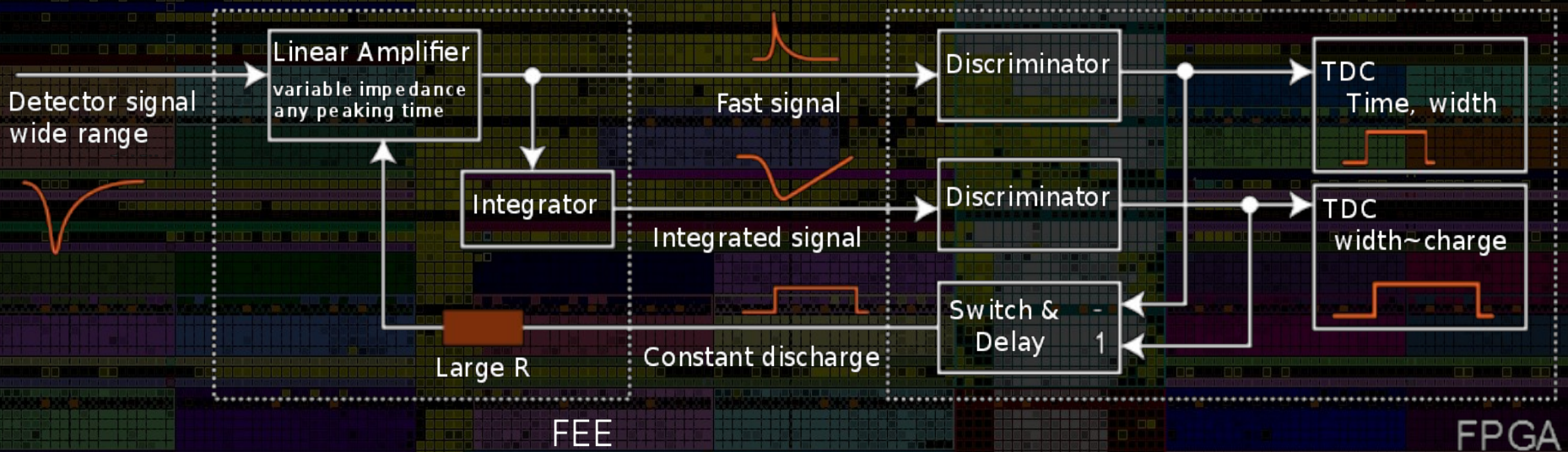
- Test setup: 500 μV , 6 ns width, analogue signal as input to PCB, amplification x40
- Threshold is set on the reference LVDS input PWM + low-pass with a resolution of $<100 \mu\text{V}$
- Pulser test: $\sim 23 \text{ ps}$
- Single phototelectron laser test with MCP: $\sim 70 \text{ ps}$
- FEE cost (without PCB+connectors) per channel only 0.56€ (16 channel version)
- Tested at the PANDA DIRC and Barrel DIRC beam times in 2012, 2013, 2014



Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

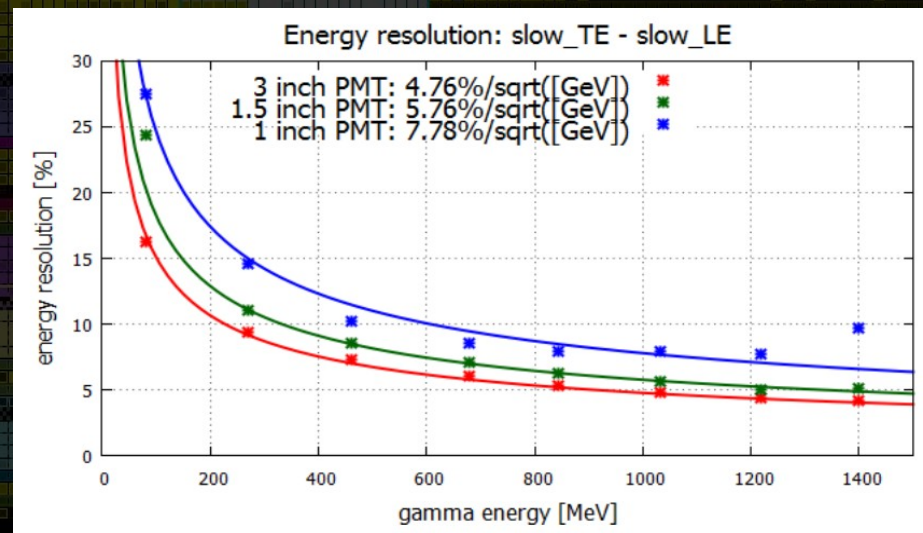
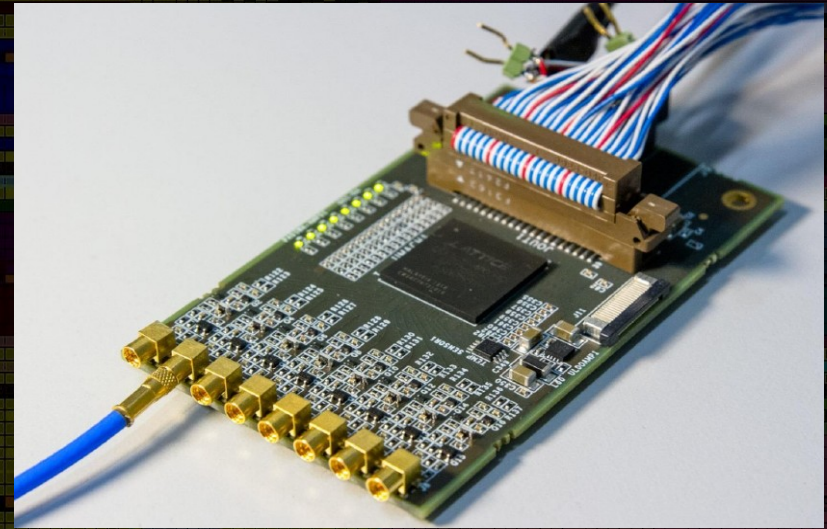
Idea: Modified Wilkinson ADC

- The input signal is integrated with a capacitor
- The capacitor is discharged using a current source \rightarrow fast crossing of zero
- Measure time necessary to reach zero



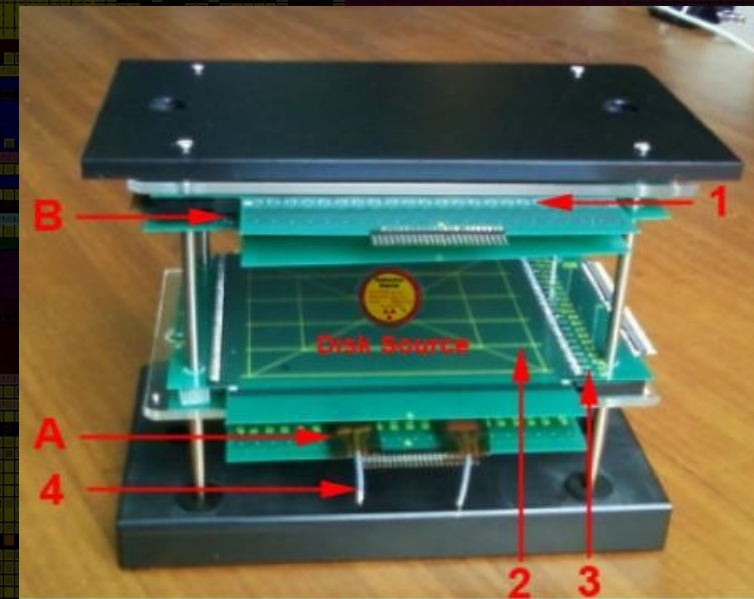
Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

- Tested in lab with pulser and in gamma beam in Mainz (MAMI)
- Charge precision in lab: 0.5% (no walk correction)
- Charge precision: as low as 5% (no walk correction)

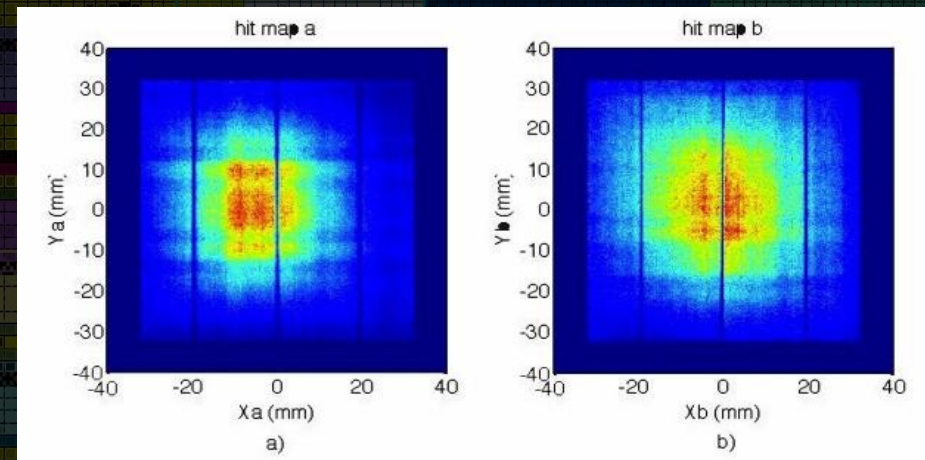


Outline : Hardware : TDC : CTS : Software : Applications : Conclusion

- Positron Emission Tomography (PET) for molecular imaging
- Approach is RPC (Resistive Plate Chambers) based
- Simulations suggest factor 8 better performance over the best commercial tomography [1][2]
- Animal PET Prototype demonstrated 0.4 mm image resolution with TRB2 [3]
- Prototype for high resolution animal PET scanner and low sensitivity (for cost reasons) whole body human scanner is under development



A-detector a; B-detector b; 1-X strips; 2-Y strips; 3-signal division network; 4-high voltage connections. [3]



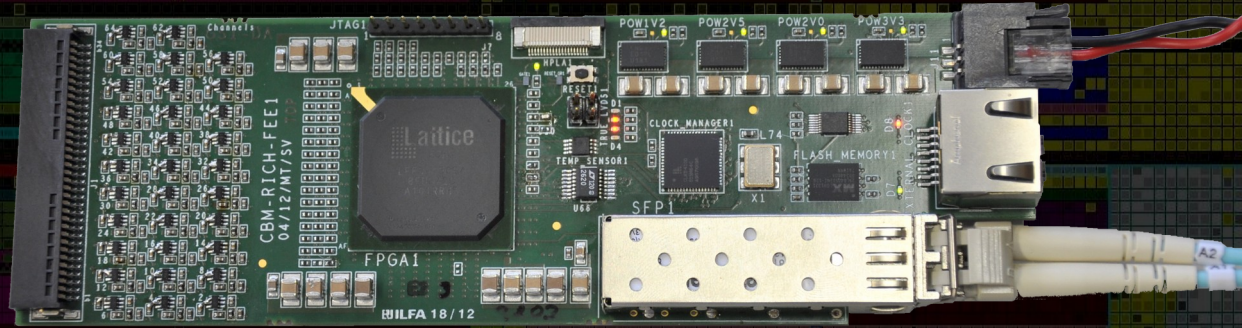
Hit map in a) detector a, and in b) detector b. The shadowed vertical lines correspond to the 0.35 mm spacers used to define the gap width. [3]

[1] A. Blanco et al., Nucl. Instr. and Meth. A602 (2009) 780;

[2] M. Couceiro et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 2651;

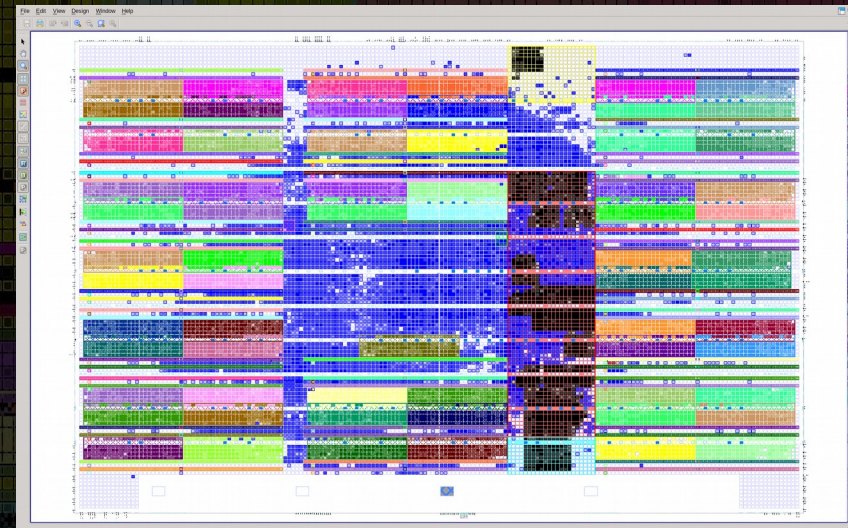
[3] P. Martins et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 3760

FEE & 65 Channel TDC

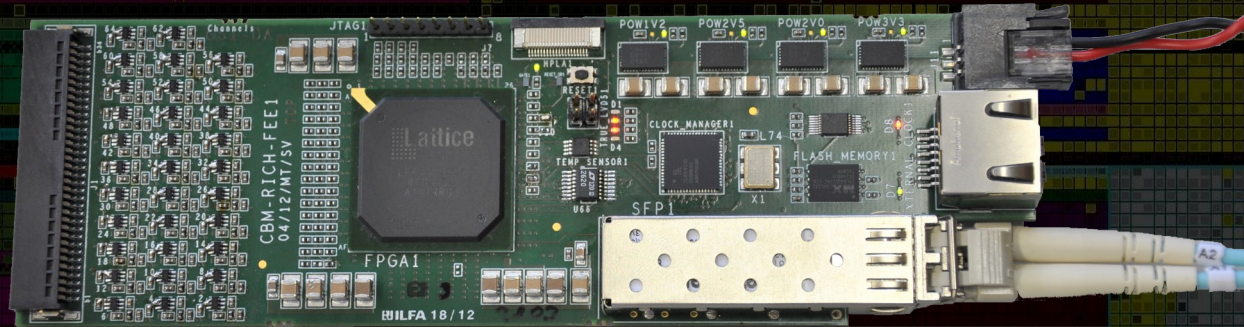


- Trigger signal is digitised for reference time (65th channel)
- Data readout through 2Gbit/s optical link
- 5x16 cm to be plugged on the back of an MCP-PMT
- Very high density for FEE & 65 channel TDC + DAQ + Power
- Tested during the CBM October 2012 test beam
- The Sync message is processed at the internal TRB3-CTS and distributed to 4 FEEs
- Half detector readout with CBMRICH-FEE, other half with nXYTER

- 64 signals from detector
- Amplification
- Thresholds
- Input signal discrimination
- Time measurement
- Data readout

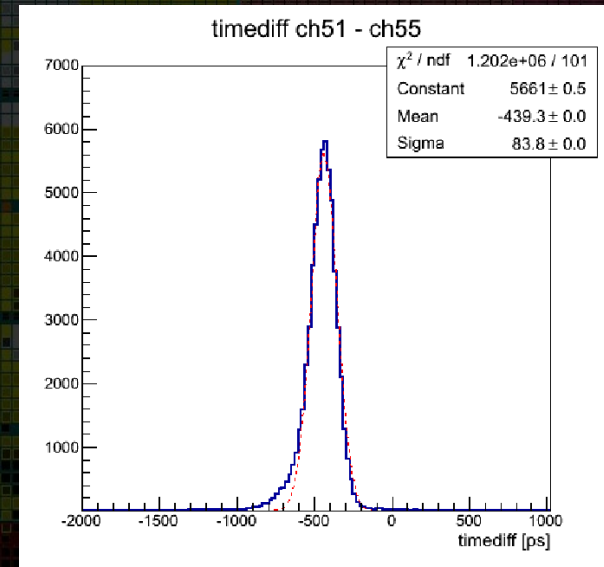


FEE & 65 Channel TDC

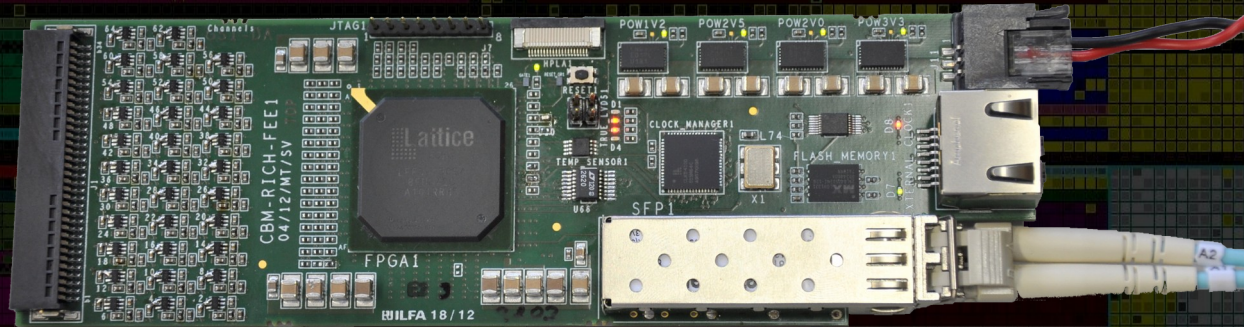


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