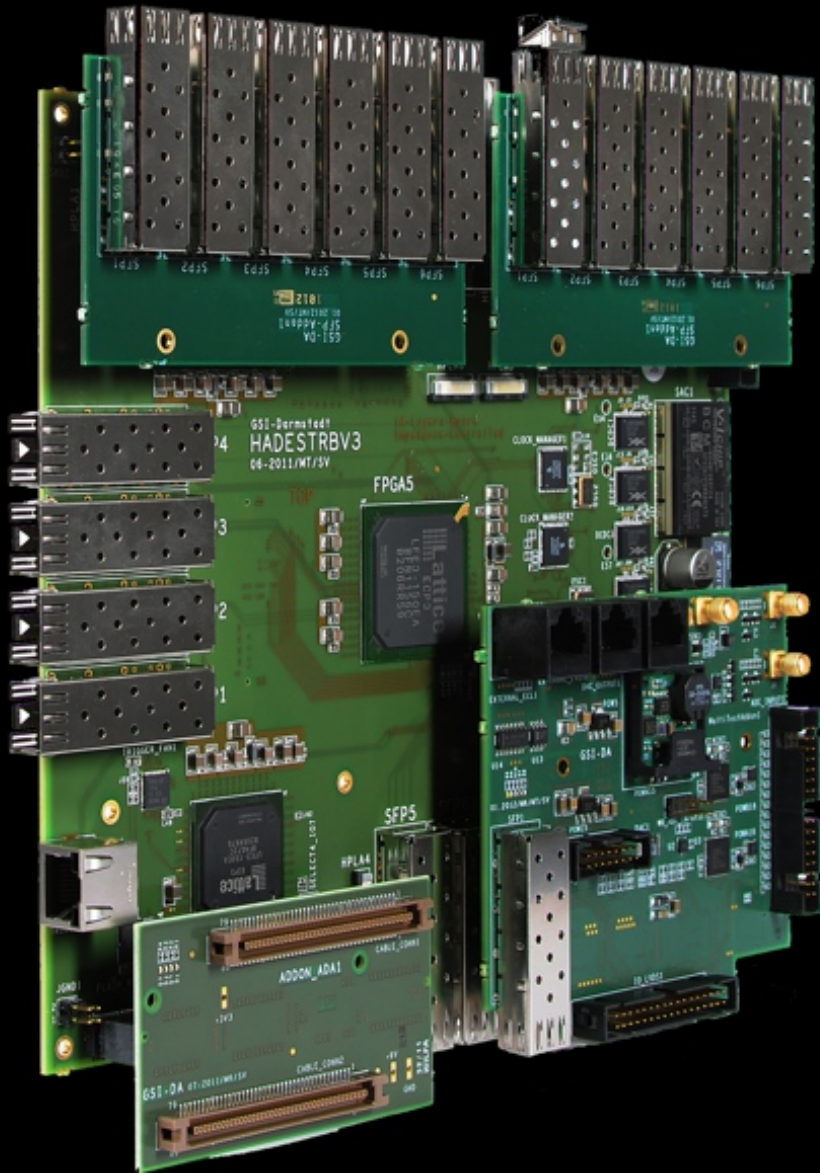


# The TRB3 family

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# Good ol' Trb3



- FPGA platform
  - 5 ECP3 FPGA
  - 8 SFP
- 5 AddOn connectors
  - 208 I/O incl. 6 Serdes
- Stand-alone operation
  - GbE for communication

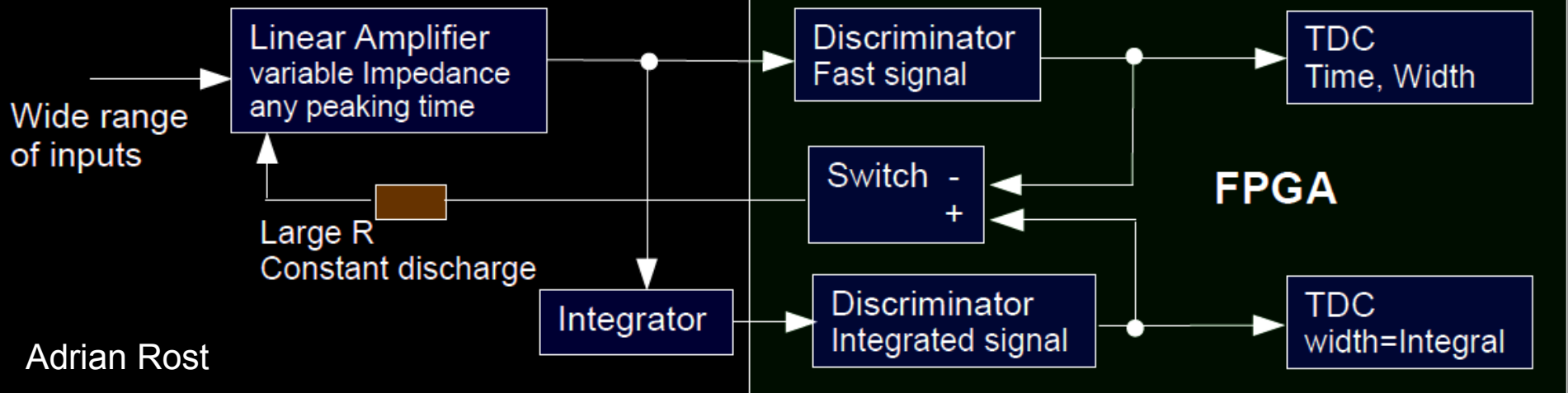
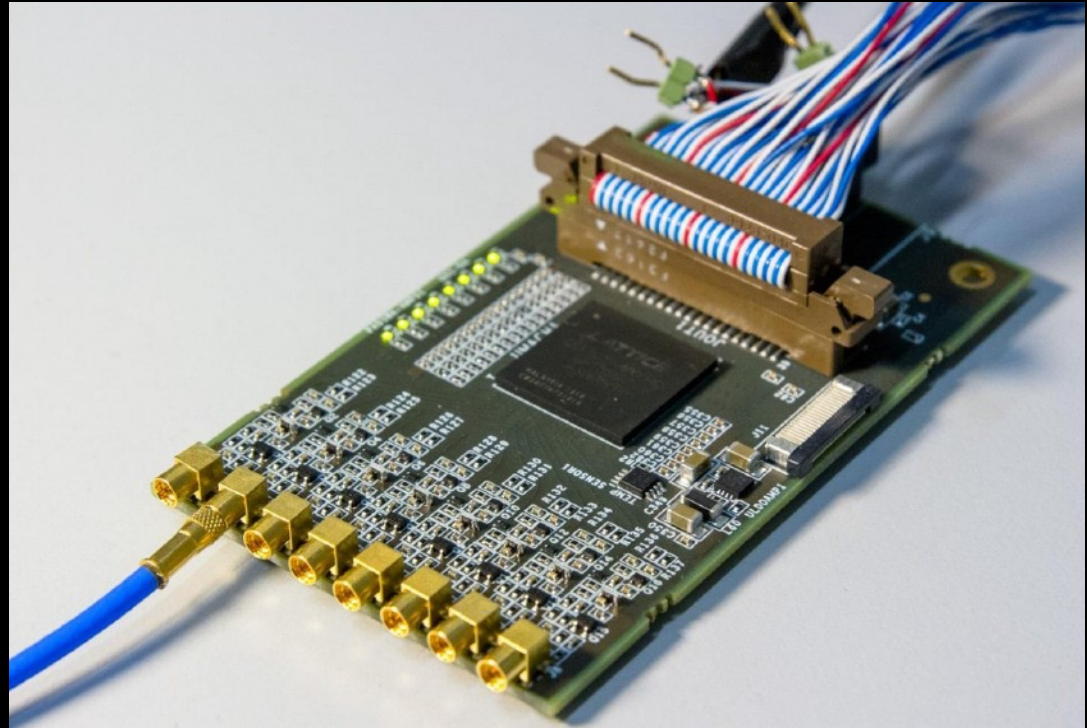
# Trb3 user community

Experiment	Nation	Location	User	Project
CBM MVD	D	Frankfurt	Manuel Penschuck	CBMnet implementation
CBM MVD	D	Frankfurt	Jan Michel	MVD read-out
CBM RICH	D	Gießen	Christian Pauly	
CBM TOF	D	GSI	Jochen Frühauf	comparison of TRB vs. GET4
CBM PSD	Russia	Dubna	Fedor Guber	CBM
A2 Crystal Ball	D	Mainz / MAMI	Andreas Neiser	
A1 Neutron Detektor	D	Mainz / MAMI	Michaela Thiel	Neutron Detektor / PMTs
Panda Barrel Dirc	D	Mainz		
Panda Disc Dirc	D	Gießen	Benno Kroek	
Panda/WASA	D	Erlangen	Adrian Zink(Schmidt)	
Panda Luminosity	D	Mainz	Tobias Weber	Luminosity Monitor
Panda Straws	PL	Cracow	Piotr Salabura	
Panda DAQ + SODA	NL	KVI	Myroslav Kavatsyuk	
HADES Ecal	D	GSI		
HADES Pion Tracker	D	München	Ludwig Maier	
HADES Diamond	D	GSI		
Human/Animal PET	Portugal	Coimbra	Paulo Fonte	
New PET	P	Cracow	Pawel Moskal	innovative PET approach
PET	CH	Zürich/CERN	Werner Luster mann	ETH-Zürich PET
MUSE@PSI	Israel	Jerusalem	Guy Ron	MUSE
MUSE@PSI	USA	Washington/Rutgers	Ron Gilman	MUSE
BM@N, JINR	Russia	Dubna	Vladimir Ladygin	Scifi-hodoscope
HZB	D	Berlin	Thomas Kleisch	Neutronendetektor
NA61	CH	CERN	Jovan Puzovic	NA61 TOF

- Not fully up-to-date, but the list doesn't get shorter

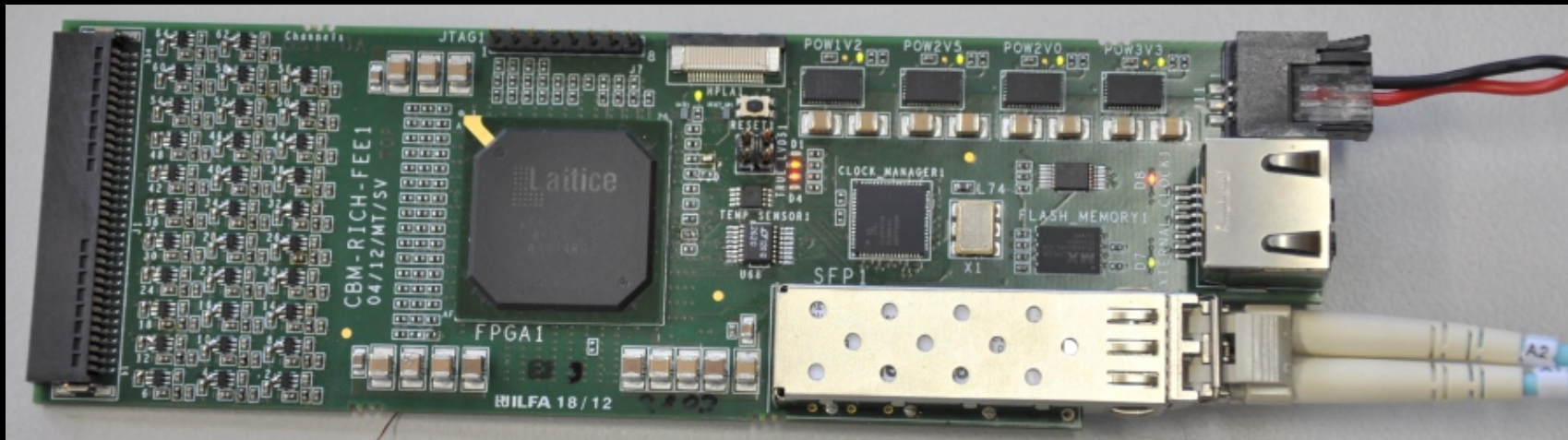
# Front-ends

- Padiwa
  - amplification, discrimination
- Padiwa AMPS: for Ecal applications with amplitude measurement
- TDC in Trb3

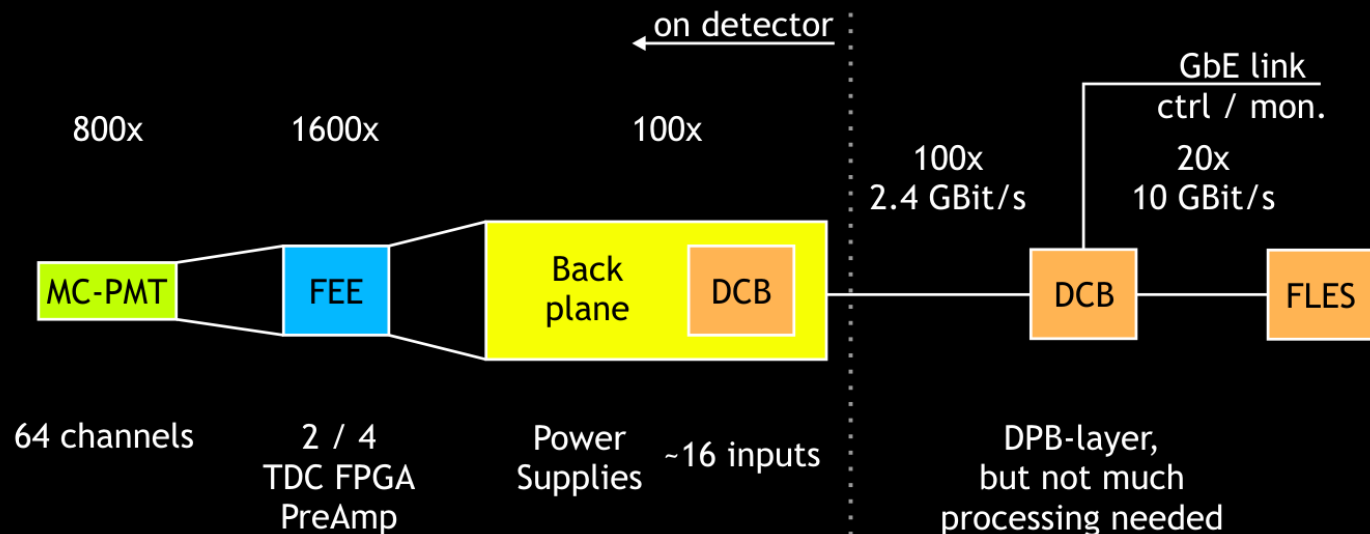


# FEE & DAQ combined

- 2012: CBM RICH prototype



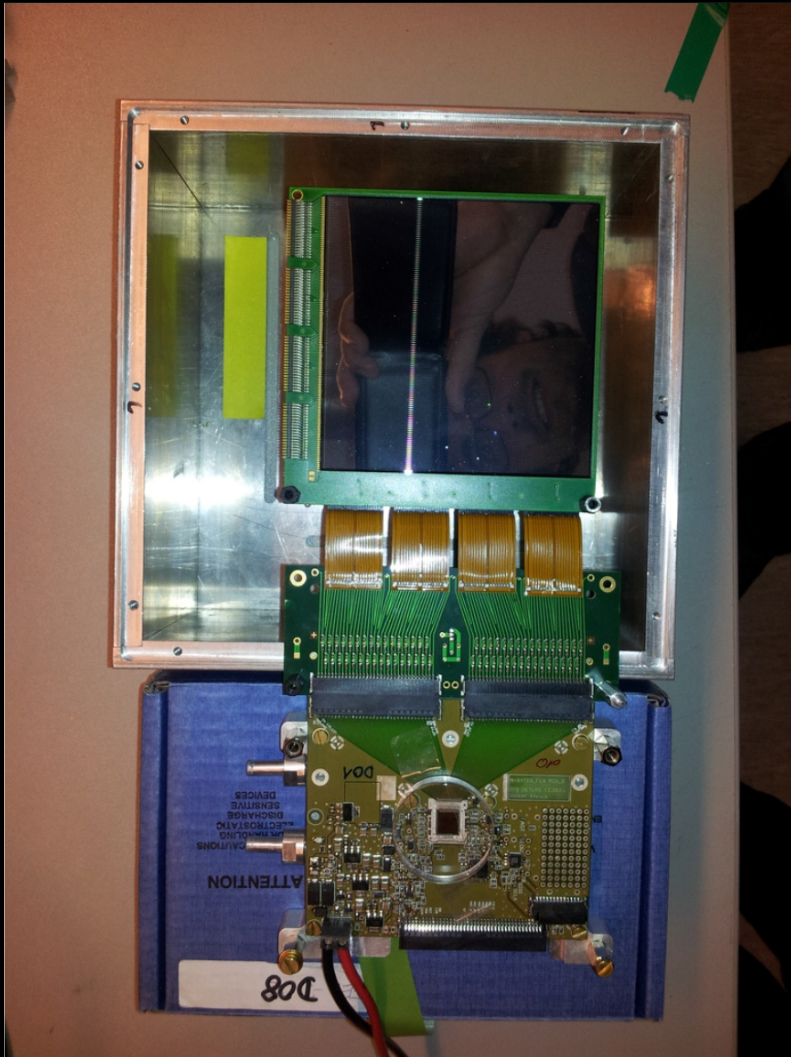
- 2015: DiRiCH Feb (CBM Rich, Panda Dirc)





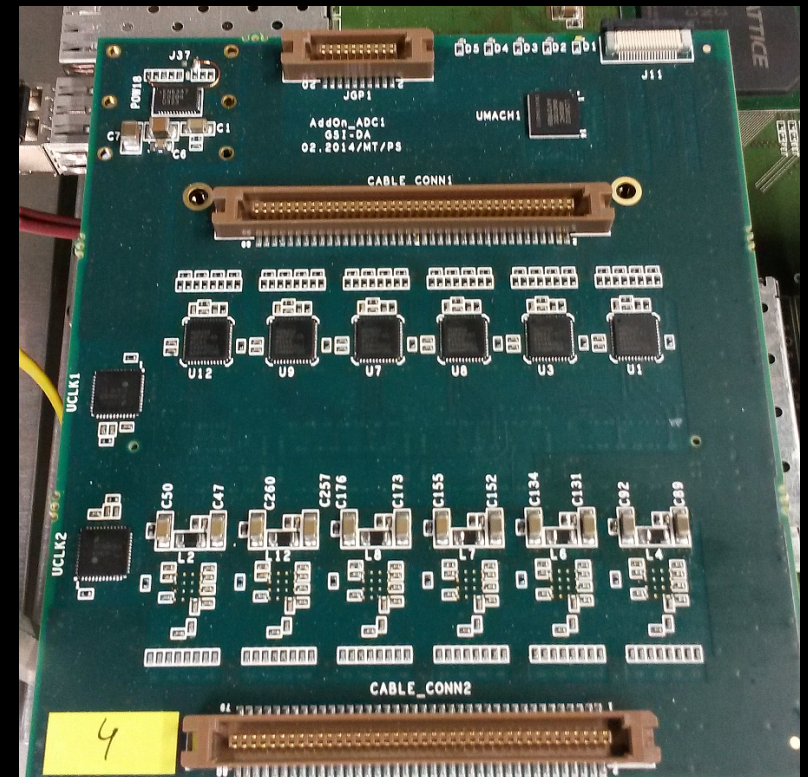
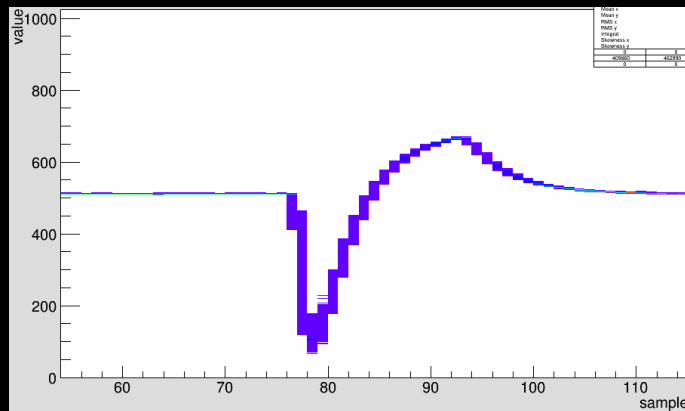
# Other Trb3-based systems

- Hades Pion Tracker
  - Silicon Strips, read out by Nxyter
- CBM MVD Prototype



# 48 channel ADC

- 48 channel / 12 Bit / 65 MSPS
- in-FPGA data processing
  - “basic” by
  - “intermediate” by Andreas Neiser (Mainz)
  - “full featured” Panda Ecal
    - not feasible due to resource usage

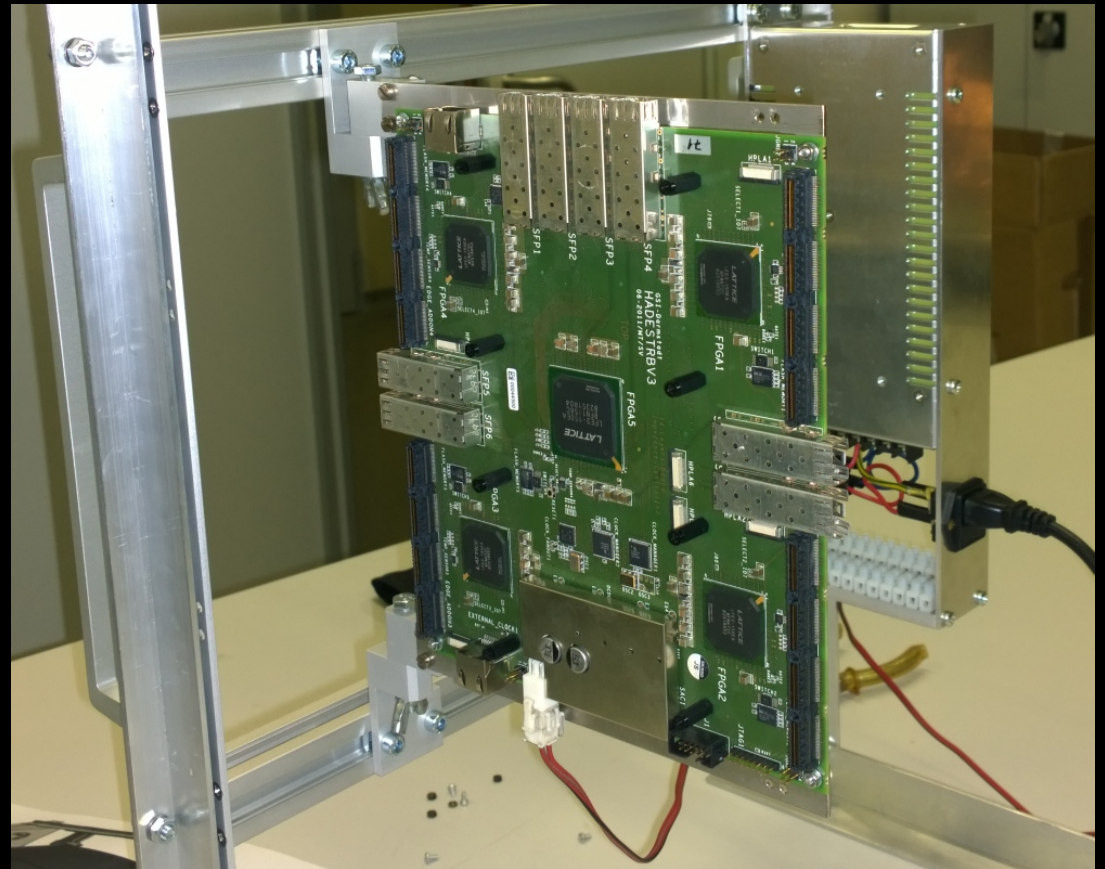




# Mounting Boards

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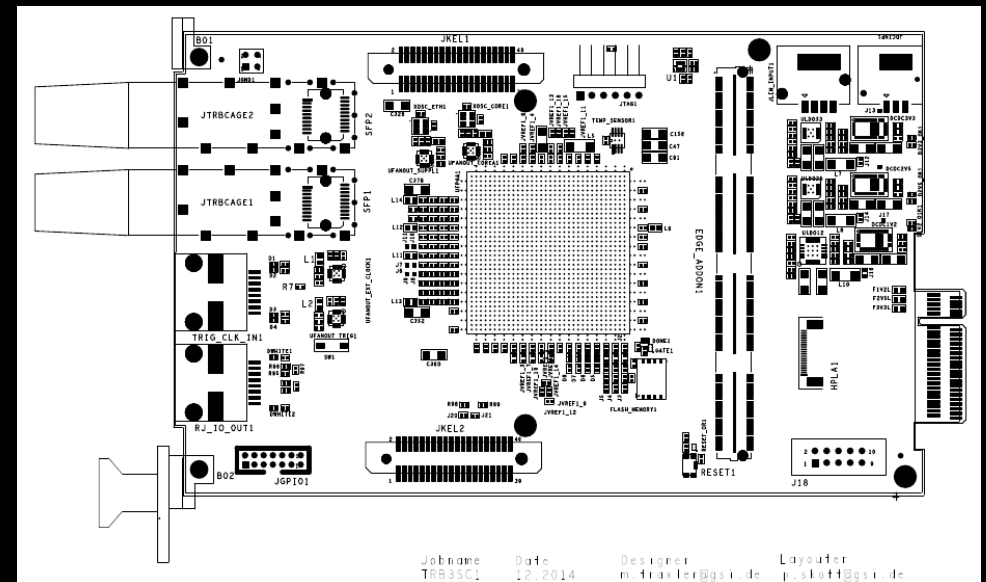
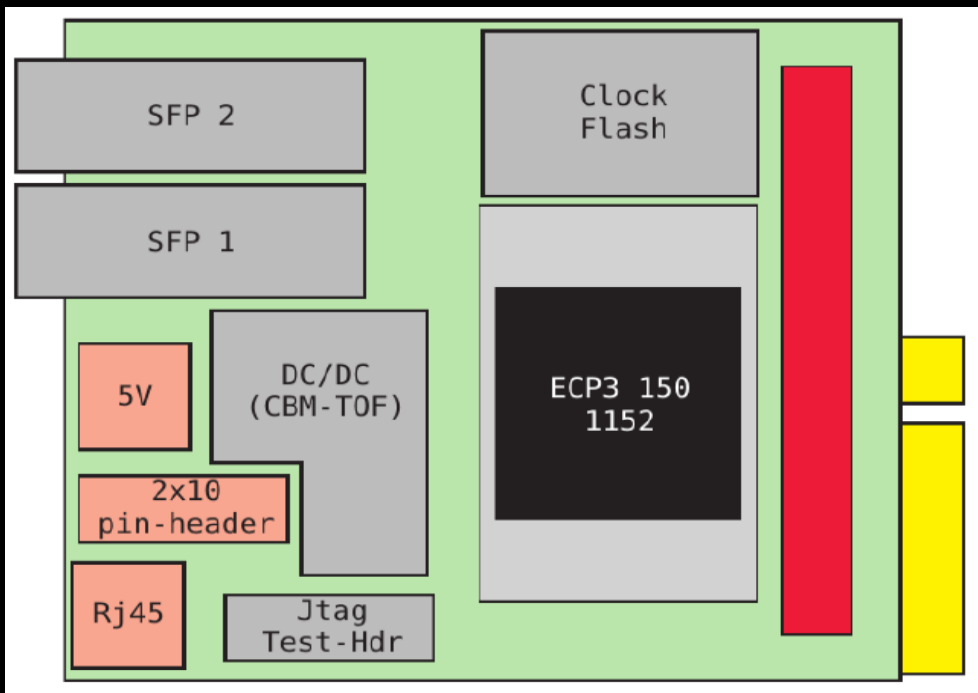
- TRB3 rack holder (by Krakow)





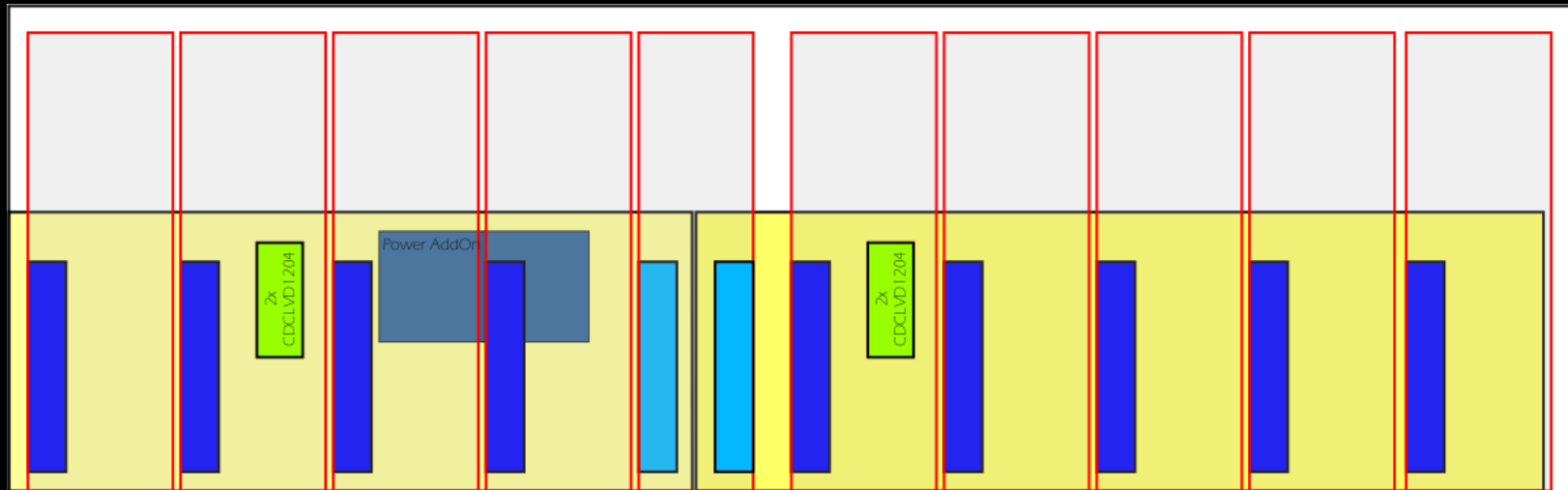
# TRB3sc

- (s)ingle FPGA, (c)rate mount
- Improved I/O: 1 GbE link per FPGA possible
  - up to 8 SFPs on AddOn card
  - 40% more inputs
  - backwards compatible to TRB3 / existing AddOns
- Use caes: tiny setups / high band-width / orderly installations



# TRB3sc backplane

- Very simple backplane, providing star-like 2.5Gbit/s connections plus some LVDS, clock distribution, power supply
- Master & Slave boards are identical
  - master either for control only or combining data to one link
  - master could be replaced with a faster FPGA to get 10GbE connectivity



- 
- Supplementary electronics available
    - clock, trigger distribution, cable adapters ...
  - Huge software repository
    - control & monitoring, on command-line and web and many more
  - In active development due to large group of users & developers