CBM DAQ Overview

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Joint CBM / Panda DAQ Workshop
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CBM Detector Requirements

Hadrons

- measure: π, K → Hadron ID → ToF System
- measure: K, Λ, Σ, Ξ, Ω
- measure: D^0, $D^{\pm}$, D_s, Λ_c → Vertex Detector

Momentum reconstruction:
→ Silicon tracker in Magnet

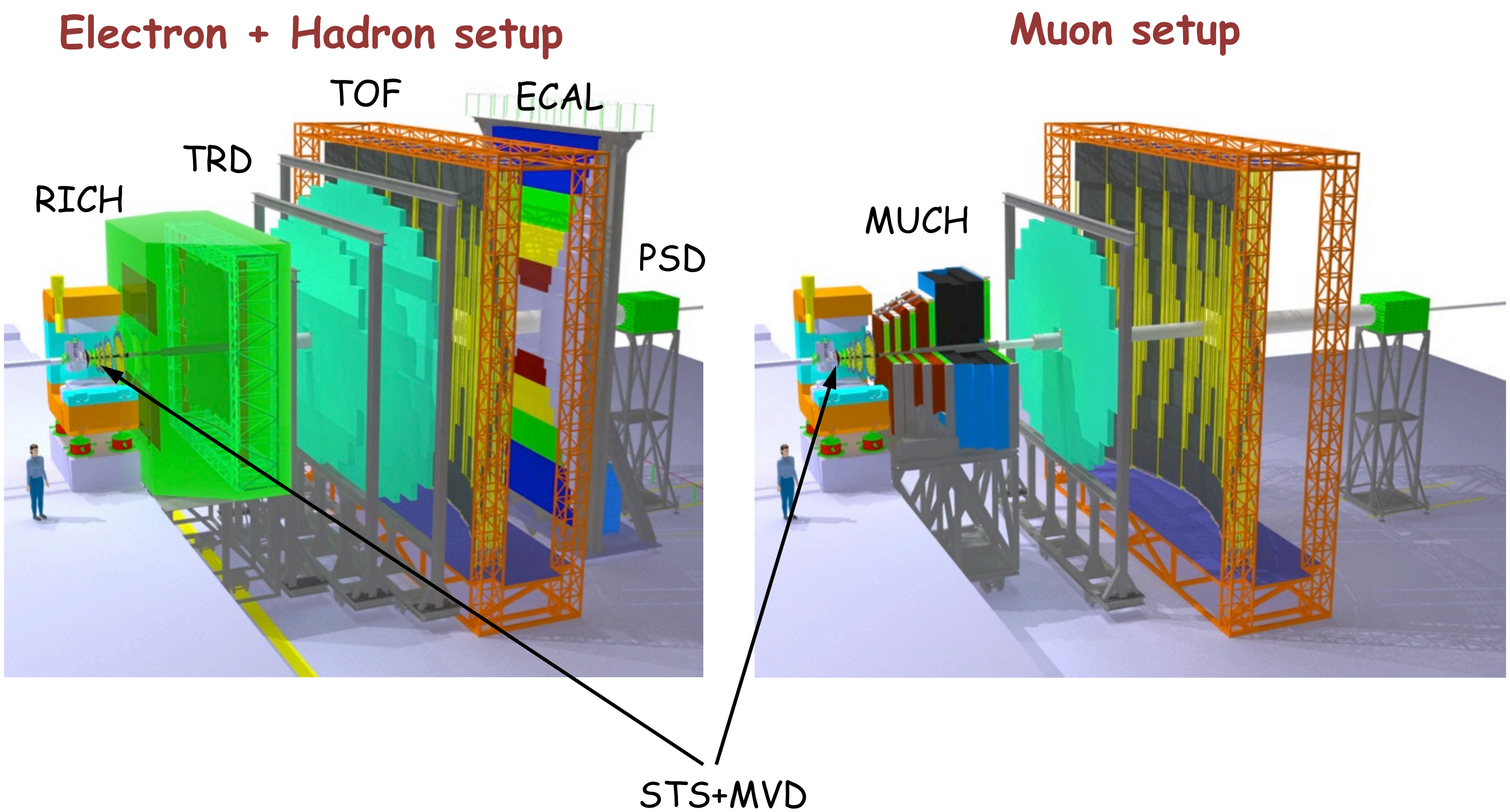
Leptons

- measure: J/ψ, ψ' → e^+e^- or $\mu^+\mu^-$ → e/τ separation → RICH and TRD
- measure: ρ, ω, ϕ → e^+e^- or $\mu^+\mu^-$ → μ separation → Absorber → MUCH

Photons

- measure: γ → ECAL

CBM Setup



Electron + Hadron setup
Muon setup
TOF
ECAL
TRD
RICH
PSD
MUCH
STS+MVD

CBM Trigger Requirements

assume archive rate:
few GB/sec
20 kevents/sec

Hadrons

- measure: π, K — offline
- measure: K, Λ, Σ, Ξ, Ω — offline >10 AGeV; trigger <10 AGeV
- measure: D^0, $D^\pm$, D_s, Λ_c — trigger

trigger on displaced vertex

drives FEE/DAQ architecture

Leptons

- measure: J/ψ, ψ' → (e^+e^- or) $\mu^+\mu^-$ — trigger μ+μ- (trigger e+e-)
- measure: ρ, ω, ϕ → e^+e^- or $\mu^+\mu^-$ — offline for e^+e^-; trigger for μ+μ- ?

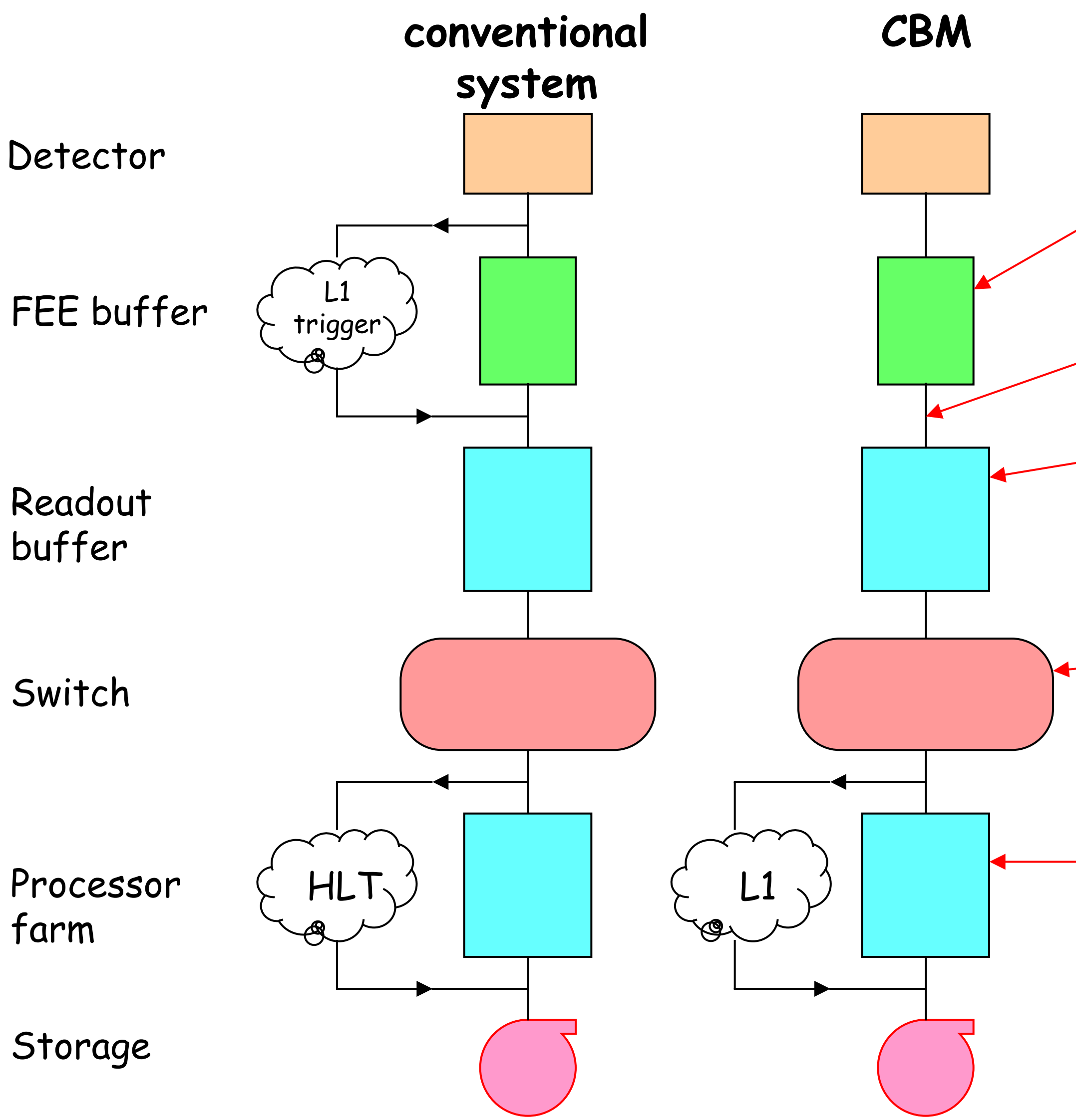
μ identification

(trigger on high p_t e^+ - e^- pair)

Photons

- measure: γ — offline ?

CBM DAQ Architecture



Self-triggered Front-end all hits shipped to DAQ. **Data push architecture**

Fast links

Readout buffer outside radiation area. Many Gbyte storage easily possible. Allows decision times of 100-1000 ms

High-throughput **time slice building**

First event selection done in processor farm.

Note: Self-Triggered FEE inspired by BTeV/FNAL

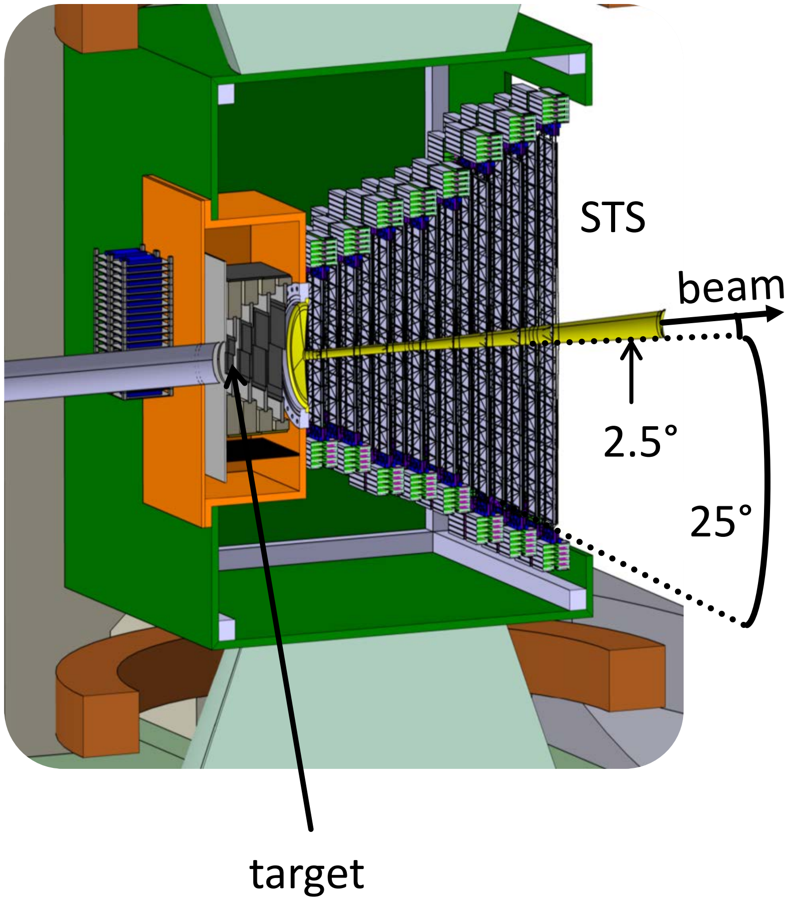
CBM DAQ/Trigger – 4 Key Points

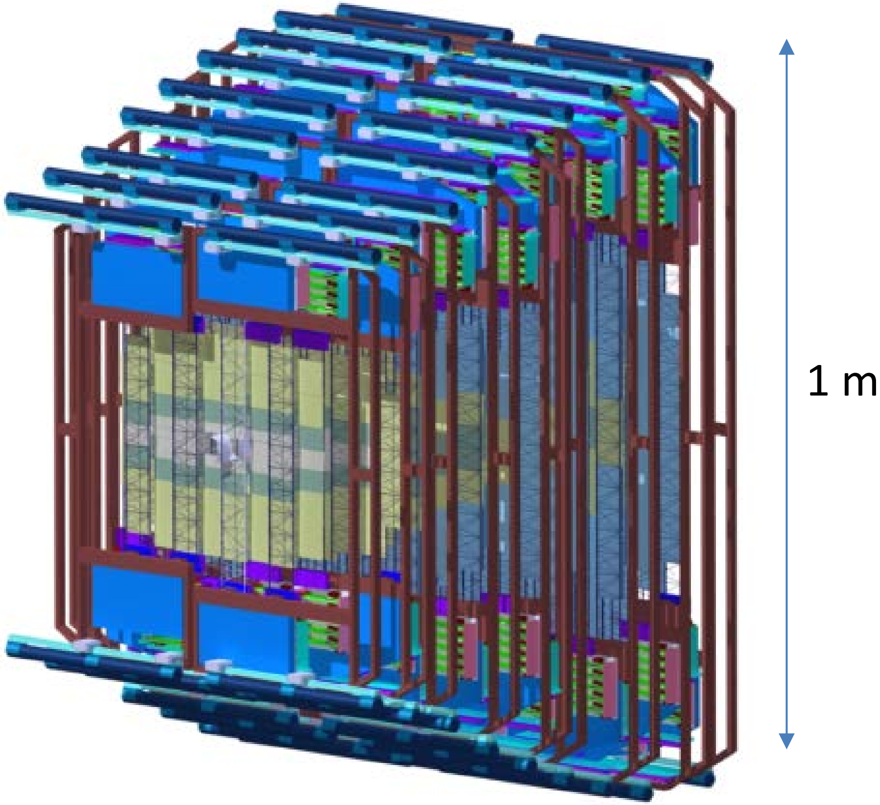
- No hardware trigger
  - All data must be transported
  - Only time available to organize data
    {fixed target + continuous beam → no bunch crossing clock}
- High interaction rates
  - Design point: 10^7 Au+Au int/sec @ 25 A GeV
    → significant radiation levels for FEE
- High raw data volume
  - Scale: 1 TByte/sec
- High channel count; High bandwidth
  - Scale: *see next slide ....*

CBM DAQ: Channel and Data density

- STS, MUCH and TRD have a high channel and data density
  - usage of custom ASICs mandatory
  - up to 1 Gbit/sec per ASIC bandwidth in STS
  - STS is most challenging case
  - STS drives architecture choices

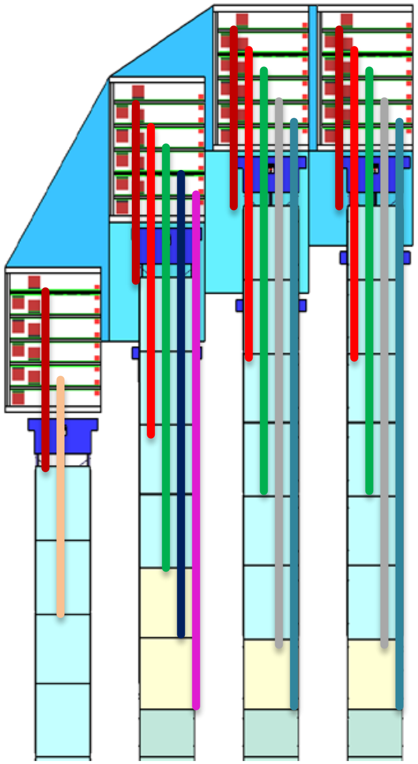
Silicon Tracking System

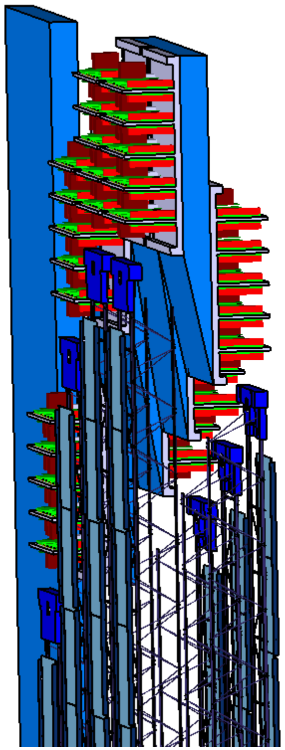


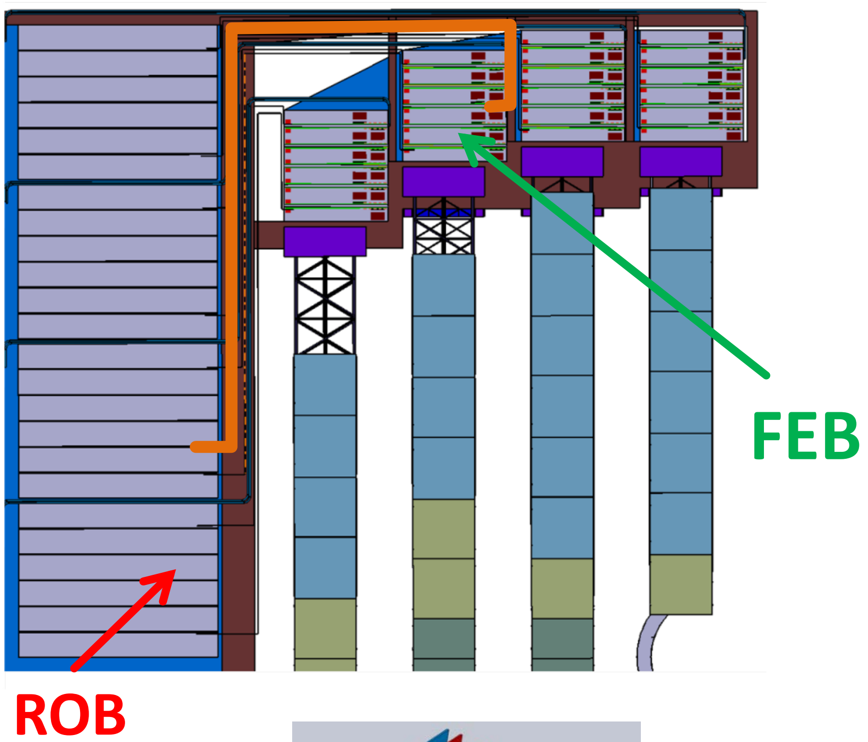


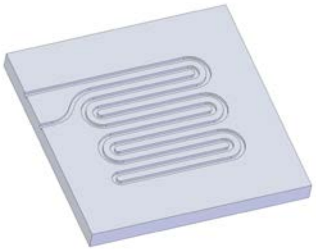
Slide: Johann Heuser

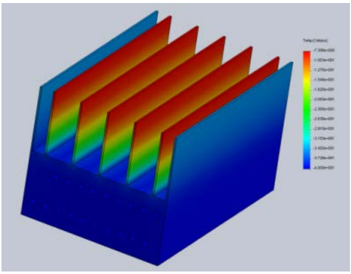
Engineering: stations/cabling/cooling











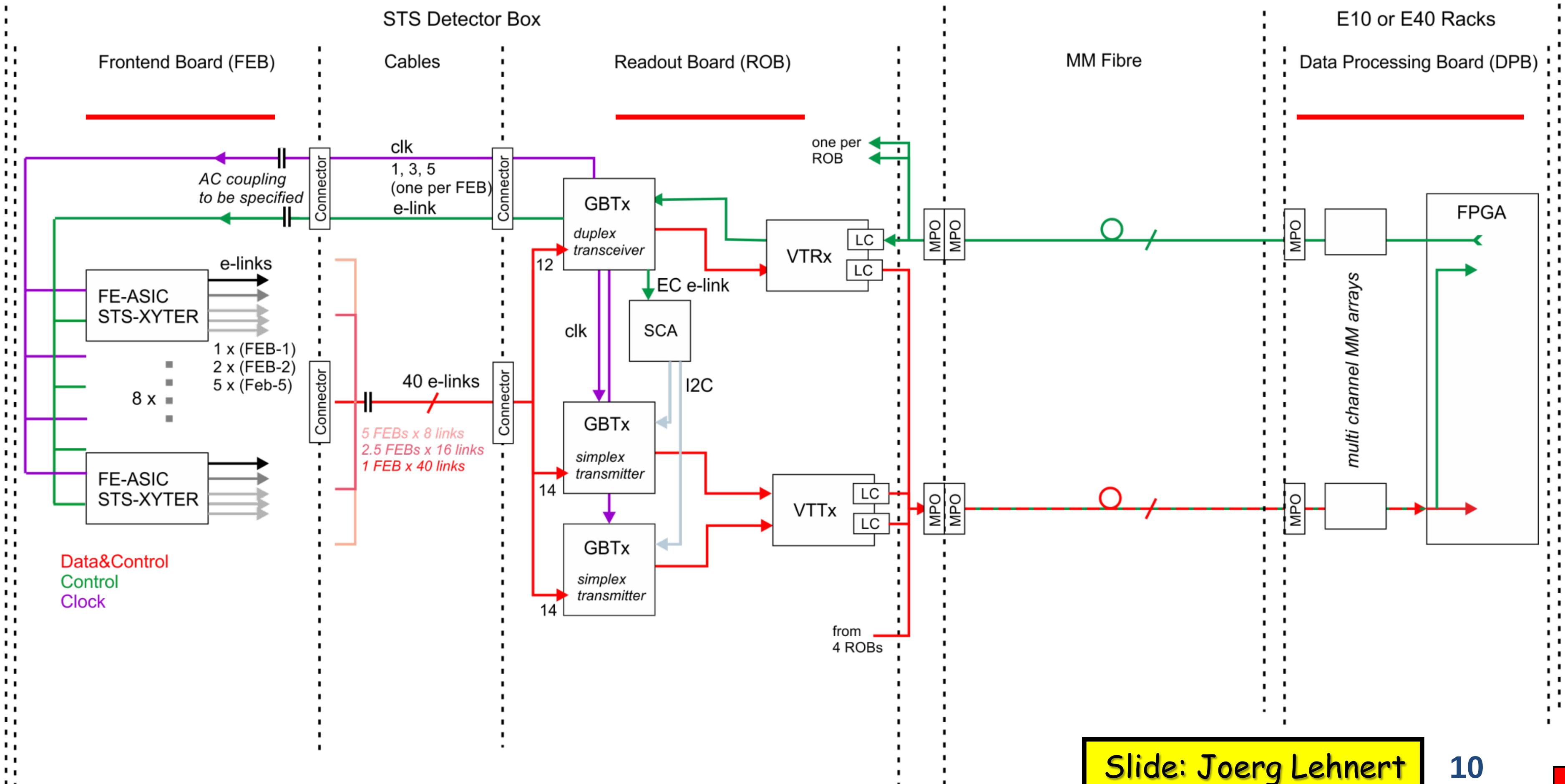
bi-phase CO_2 cooling system
STS electronics total: 42 kW

FEB stack
200 W

Slide: Johann Heuser

Current STS Readout Concept

FEB	Electrical Interface	ROB	Optical Interface	DPB
8 STS-XYTER	SLVS/LVDS 10-42 pairs/FEB	GBTx / VL	4 MM fibers /ROB	



Slide: Joerg Lehnert

STS Readout Board (ROB)

1 master GBTx connected to 1 VTRx transceiver

- Slow control, clock distribution
- Data readout

2 slave GBTx connected to 1 VTTx (twin transmitter)

- Data readout, control responses

1 SCA as slow control interface from master to slaves

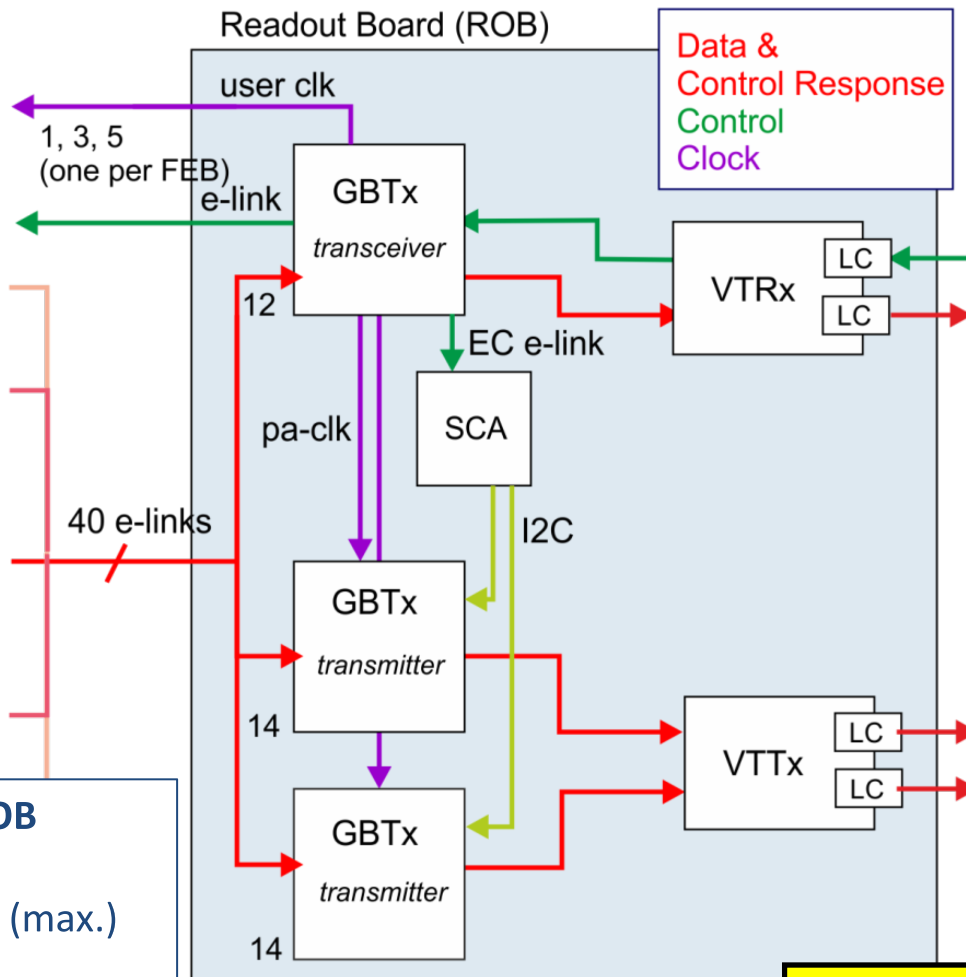
Frontend Side

Clock and Slow Control:

- single clock and slow control downlink to each FEB
- multidrop to 8 ASICs

Input from FEBs:

- 3x14 = **42 e-links@320Mbps**
- GBTx wide bus mode
- input bandwidth 13.44 Gbps



Backend Side

Output to DPBs:

- 1 VTRx, 1 VTTx
- **1 downlink**
- **3 uplinks**
- user bandwidth 3x4.48 = **13.44 Gbps**

SCA:

- I2C masters for slave GBTx control
- Use additional slow control features?

Minimized number of FEB-ROB connections:
on FEB side from 8+2 to 40+2 (max.) differential pairs

Slide: Joerg Lehnert

CBM DAQ: Most Data via GBTx

- All CBM sub-systems with high data density use GBTx

Detector	#channels	#ASICs	#GBTx
STS	1800k	~15k	~3000
MUCH (SIS-100)	180k	~1.5k	~400
TRD (SIS-100)	290k	~9k	~1400

- Others, like ToF, plan to use GBTx too

CBM and FEE Radiation Levels 1

- TID and NIEL per 'CBM-Year'

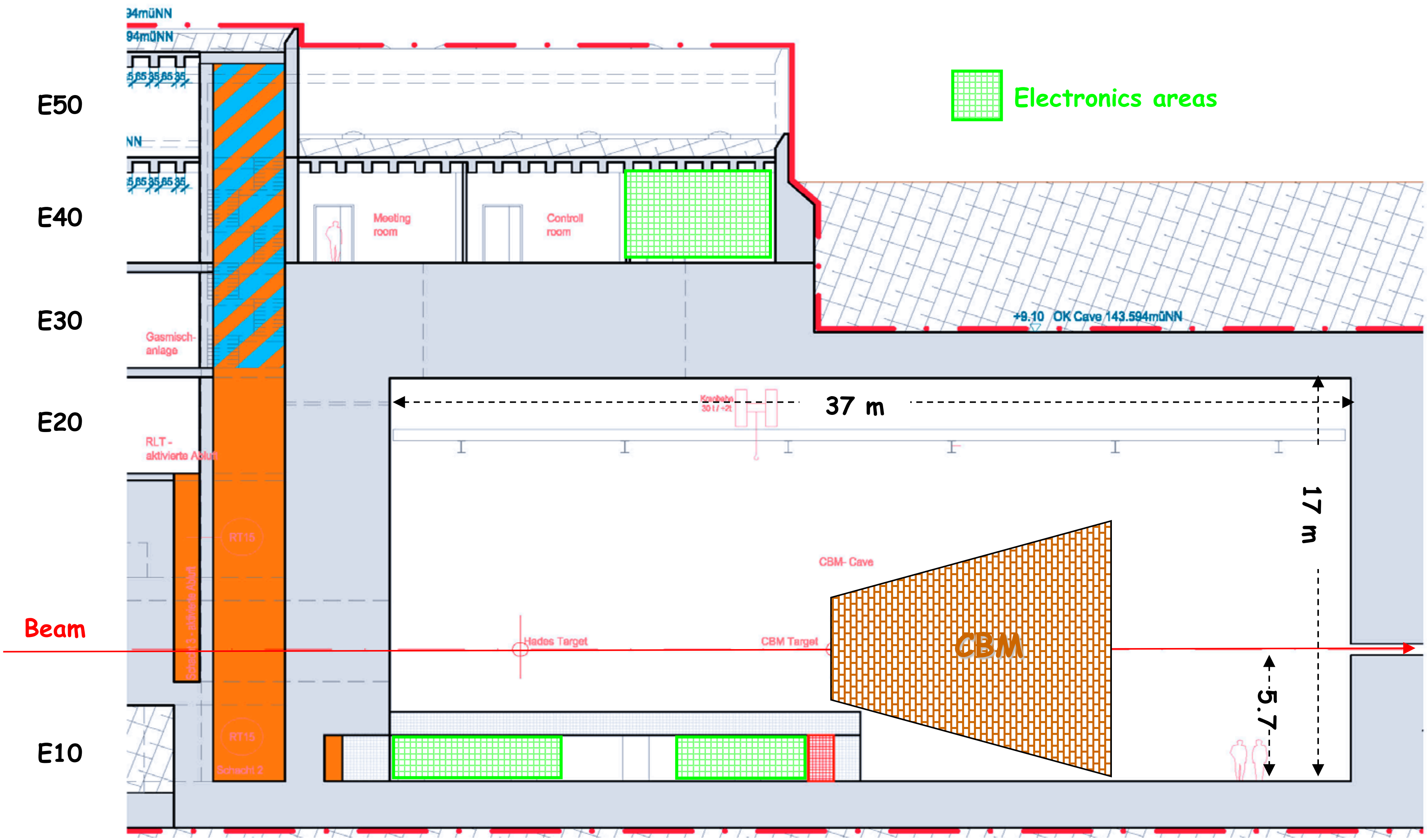
Old Calculations
Will be updated soon

Detector	TID [Gy / yr]	NIEL [/cm² / yr]	Fast Hadrons [h/ (cm² s)]
STS-30cm	1000	$3\ 10^{12}$	100 k
STS-100cm	100	$1\ 10^{12}$	20 k
MUCH-1 inner	1000	$8\ 10^{13}$	700 k
MUCH-1 outer	100	$5\ 10^{12}$	30 k
RICH (120cm)	10	$3\ 10^{10}$	2 k
TRD-1 inner	200	$2\ 10^{12}$	60 k
TRD-1 outer	2	$3\ 10^{10}$	1 k
TOF inner	100	$3\ 10^{11}$	50k
TOF outer	2	$5\ 10^{10}$	1 k

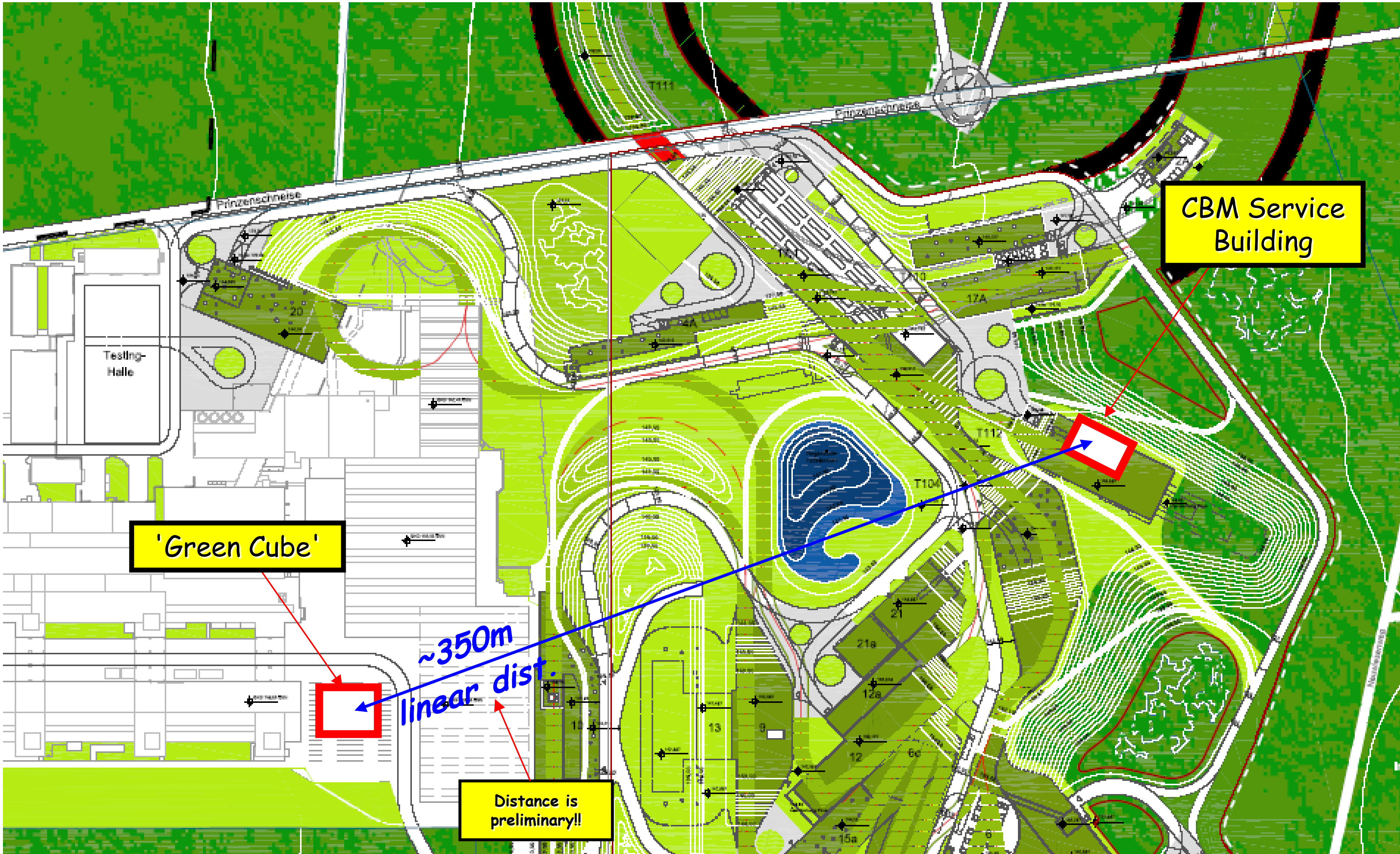
CBM and FEE Radiation Levels 2

- Compared to LHC+ inner tracker modest
  - CBM requires 'radiation tolerant' components
- TID not a key issue
  - For FEE 10 kGy or 1 Mrad
  - Easy to achieve in modern ASIC technologies
- NEIL neither
  - Exceptions: Opto transceivers + MUCH inner edge
- SEU robustness required
  - Limits where FPGAs can be used
    - Typ SEU cross section: 1 10^{-14} SEU/bit
    - Modern FPGA: ~100 Mbit config
    - 100k flux → 1 SEU per 10 sec

Electronics Areas in E10 and E40



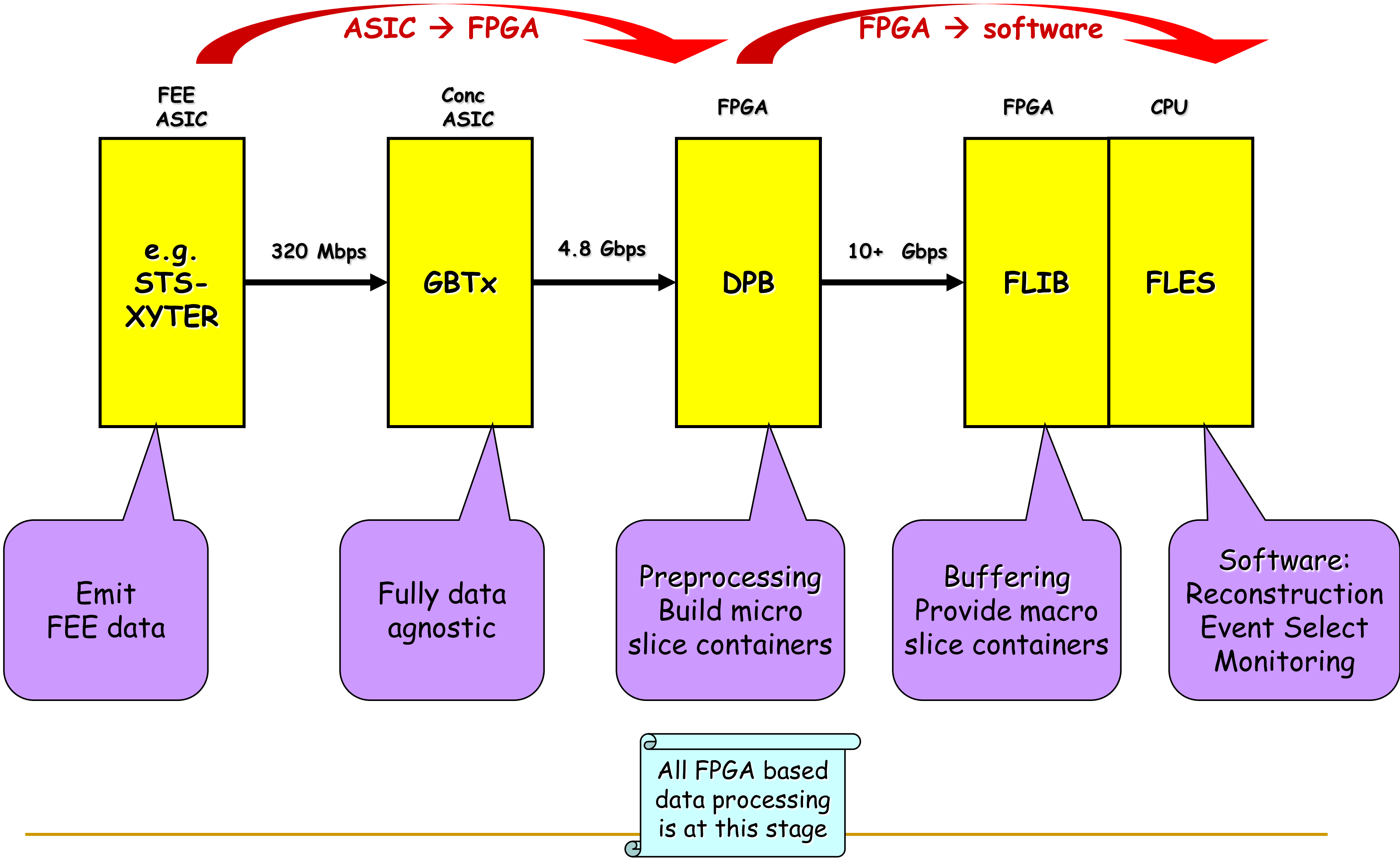
FAIR T0 Centre as CBM FLES Location



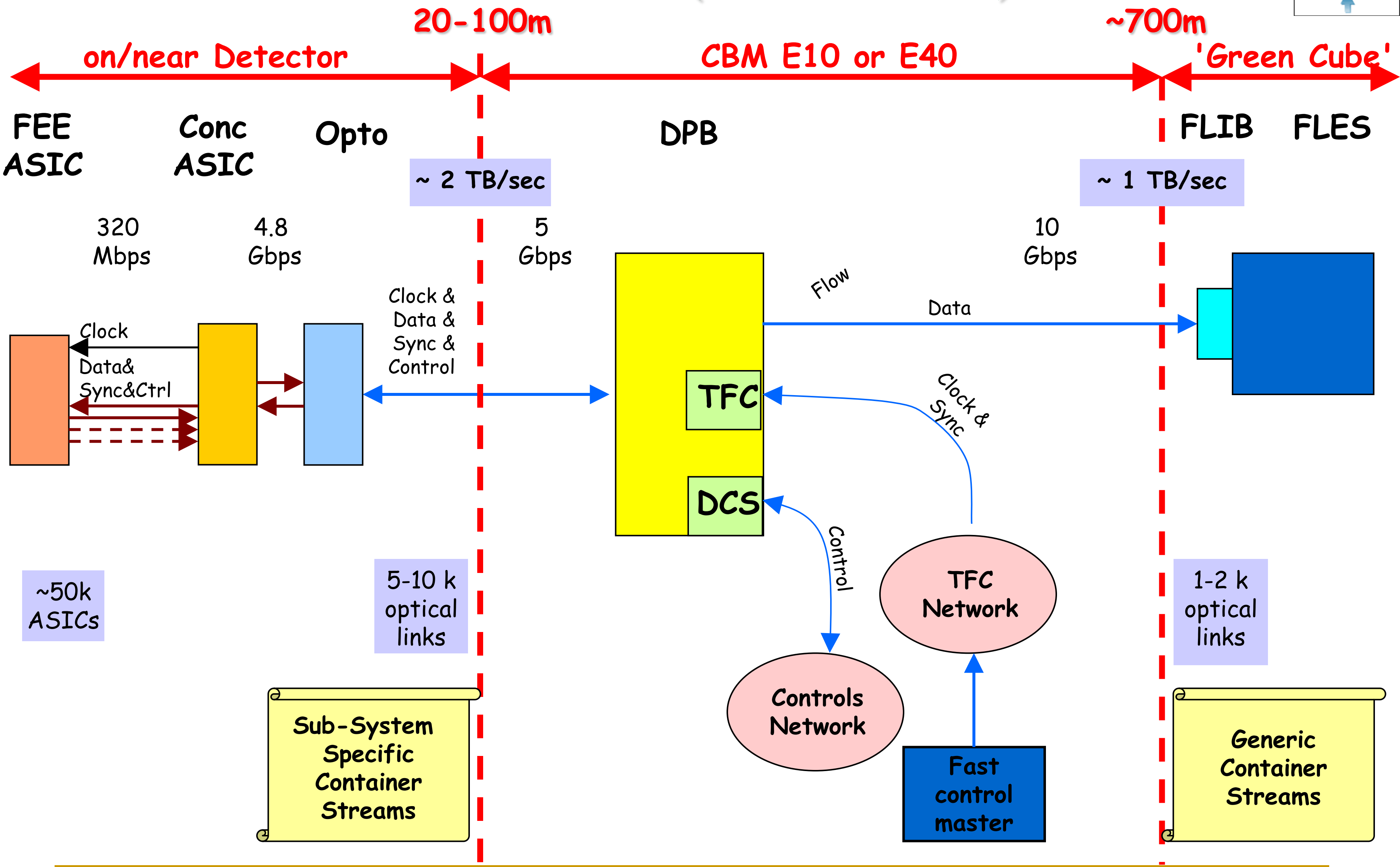
Time Slices

- Time is the only way to organize data at DAQ level
- Events {'one interaction'} are defined during reconstruction
- → Time slice building instead of 'event building'
- Requirements for time slice building
  - collect all data of a time slice in one compute node
  - adjacent time slices must have some small overlap
    {otherwise interactions at the slice boundary can not be reconstructed}
- Efficient solution
  - define a micro slice, length few μsec
  - macro slice is build from micro slices
    {e.g. 100 mirco slices with 1 micro slice overlap}

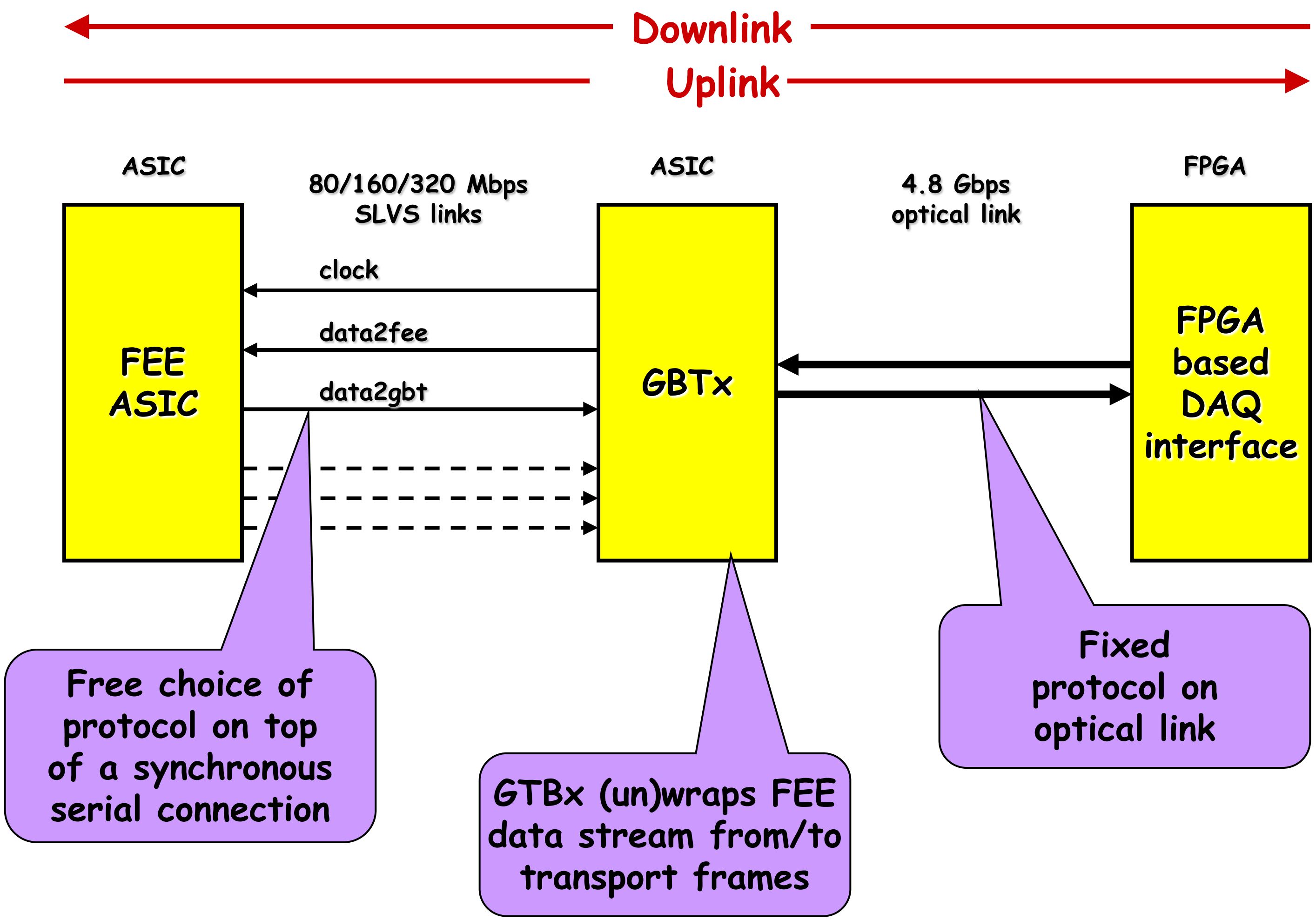
CBM Readout Chain



CBM Readout chain (ASIC case)

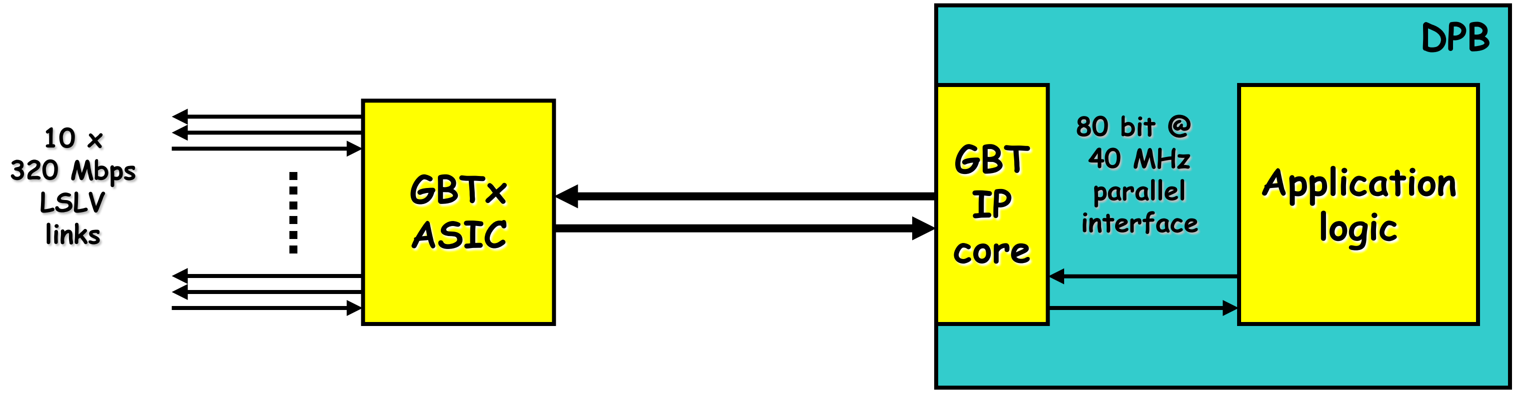


GBTx Based Readout Chain



GBTx in a Nutshell

- GBTx provides essentially a 'remote SPI' interface



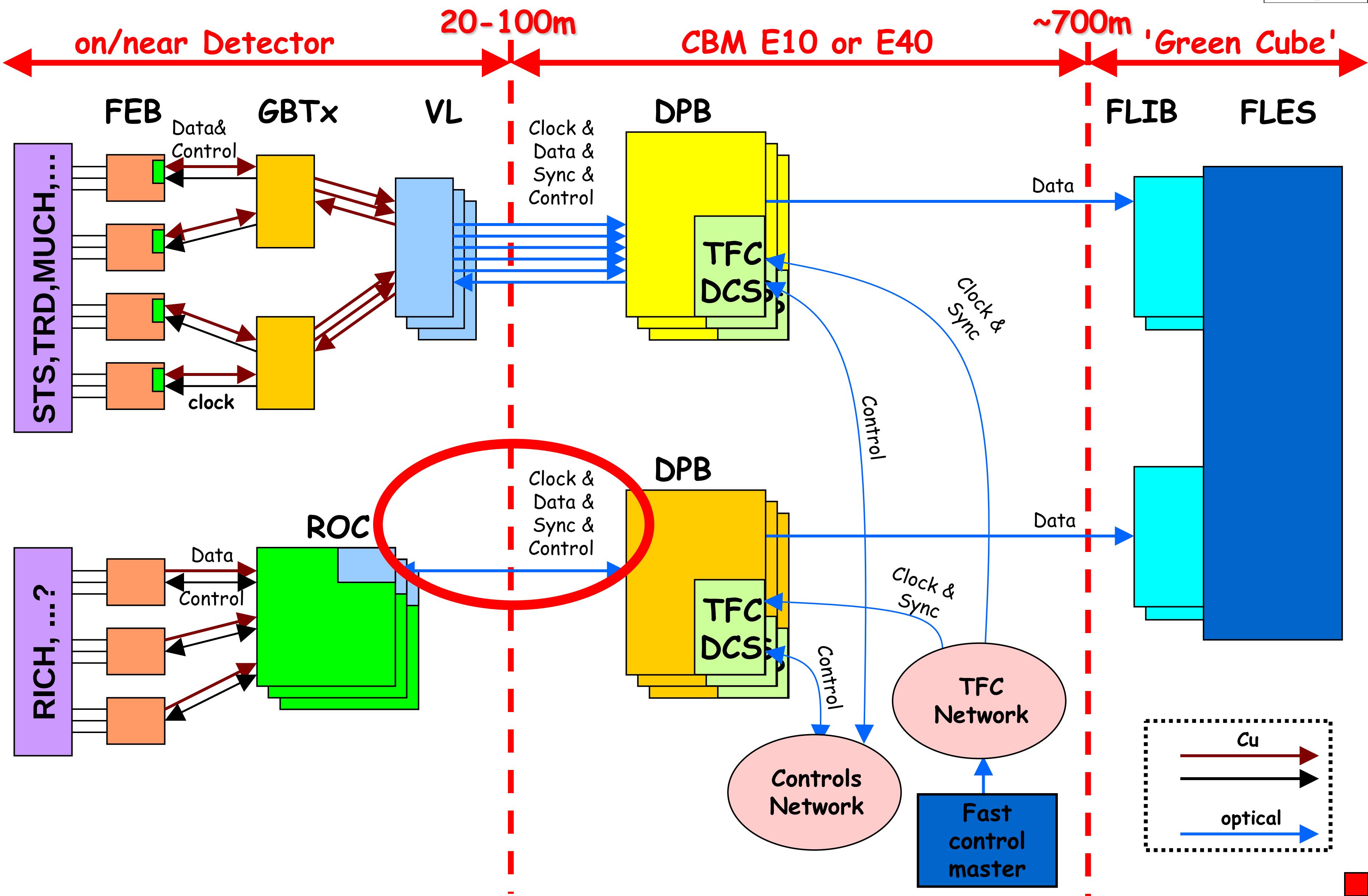
DPB Mission Statement

- Traffic class Mux/Demux
  - Towards FEE: combined clock & sync & control & data
  - Towards backend separate
    - Fast control: clock & sync (e.g. via White Rabbit)
    - Slow control: e.g. via controls Ethernet
    - Data links to FLIB
- Provide generic DAQ and Control Interface
  - Generic data container stream to FLIB/FLES
  - Generic fast/slow controls interface
  - Encapsulate Sub-System specific formats/protocols
- Data Preprocessing
  - Feature extraction (in case of SPADIC)
  - Cluster finding ect.

CBM DAQ: Beyond GBTx

- Some CBM sub-systems have
  - modest data densities
  - low particle fluxes at FEE location
- They can and will use FPGA-based FEE
  - RICH
  - PSD (when FEE separated)
  - ECAL (t.b.d.)
- The readout chain for FPGA-based sub-systems must
  - be compatible with common DPB layer
  - be compatible with common TFC (Timing & Fast Control)
  - be compatible with common controls system
- More in "CBM FPGA-based sub-systems"
  → *next talk by Christian Pauly*

CBM Data Flow – Full Picture

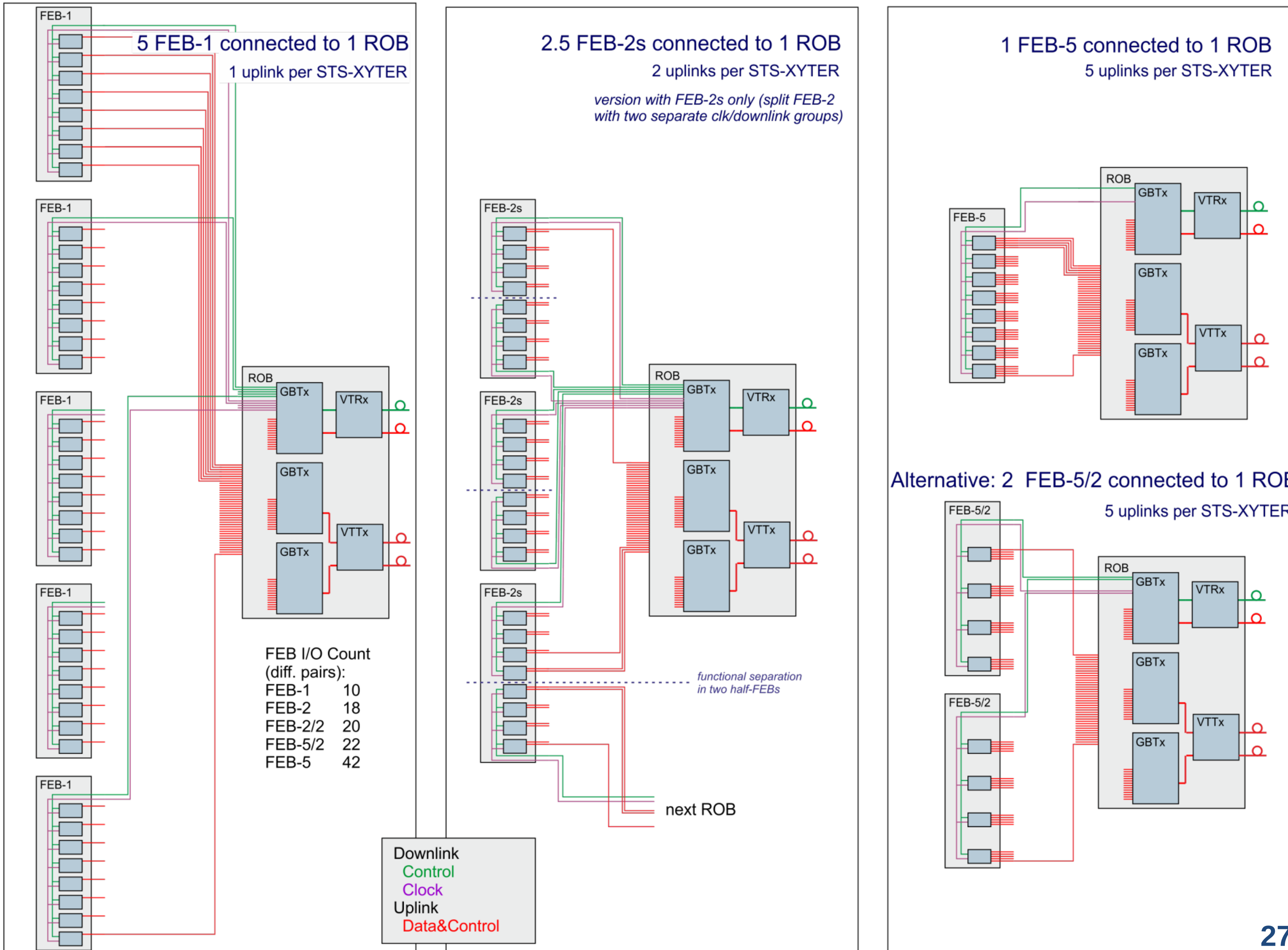


The End

Thanks for your attention

Backup Slides

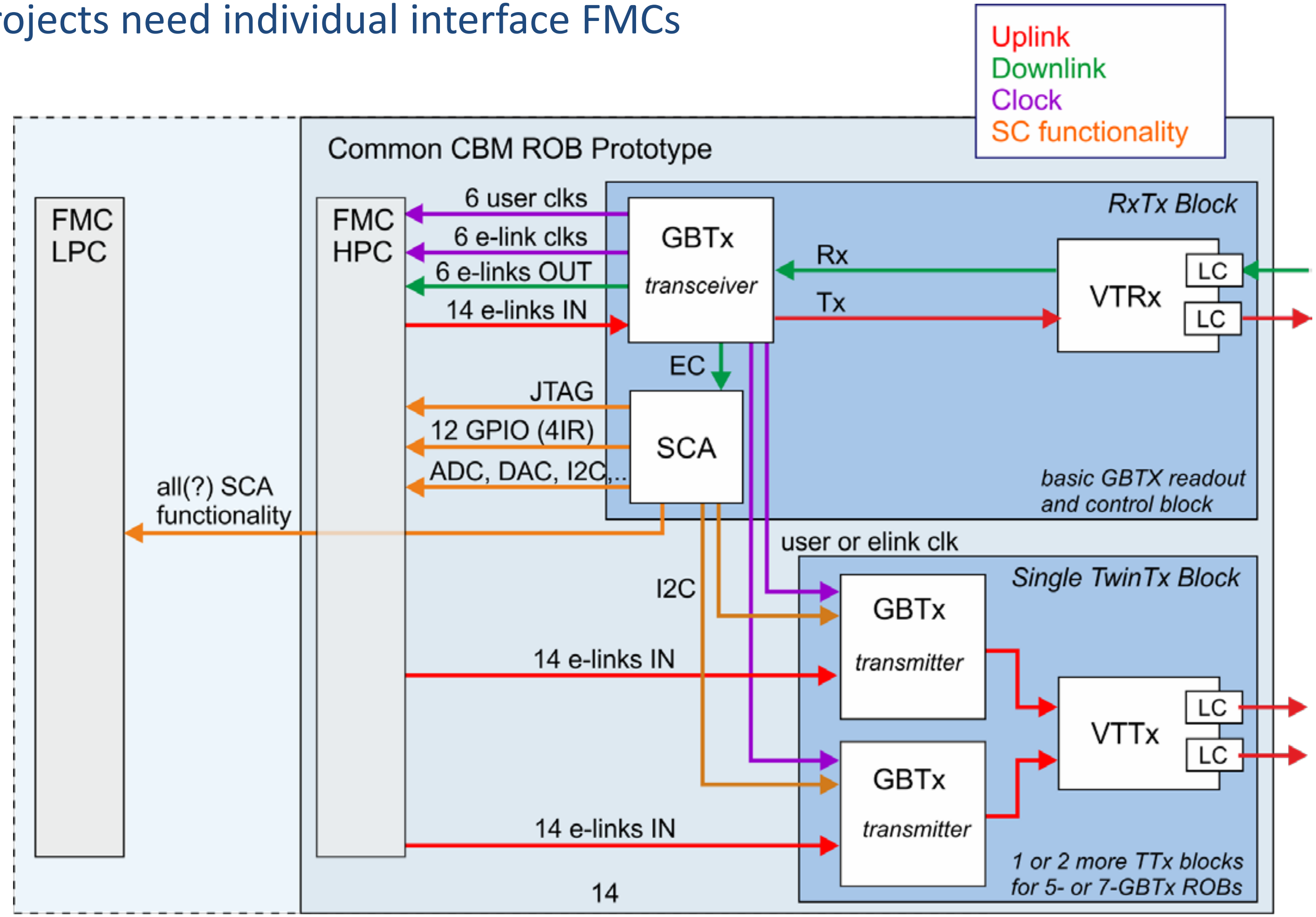
FEB Types and ROB Connectivity



Common CBM ROB Prototype

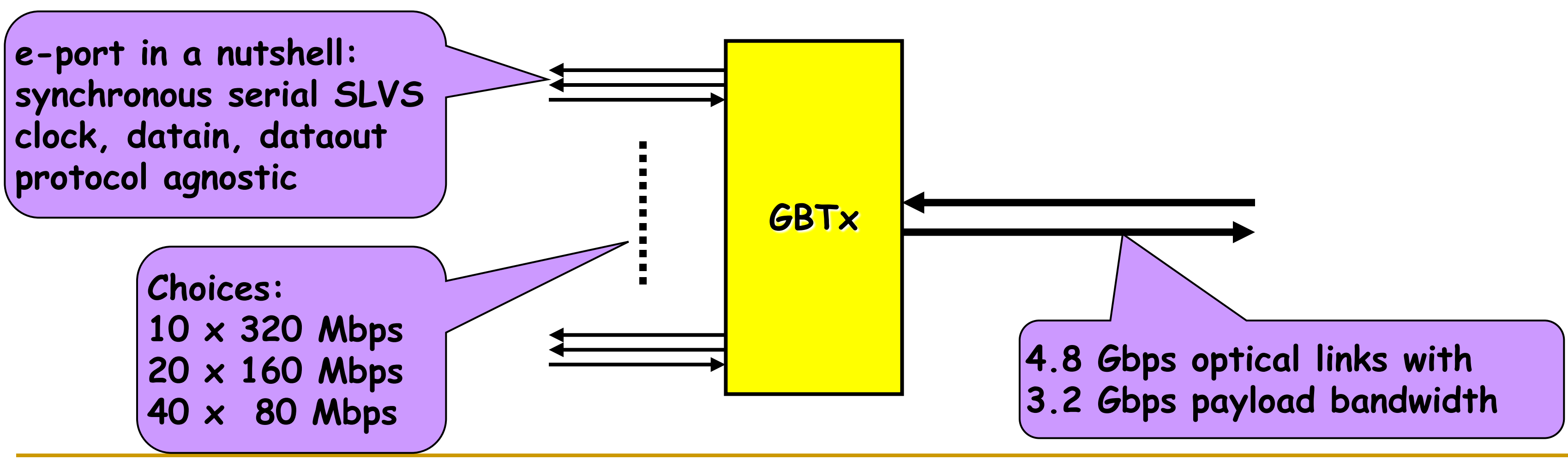
Alternative approach: **common CBM GBT prototype board**

- **Full GBTx/VL functionality** for all readout chains (STS-XYTER, GET4, SPADIC2,..)
- **frontend connectivity** (GBTx E-Links, SCA) routed to **FMC connector**
  → projects need individual interface FMCs



GBTx in a Nutshell 1

- GBTx
  - provides a **bi-directional synchronous bit stream** with **constant latency** between backend and FEE ASIC
  - can be operated in several modes
  - here only one mode is discussed:
    - uplink and downlink uses GBT frames
    - 10 e-ports with 320 Mbps

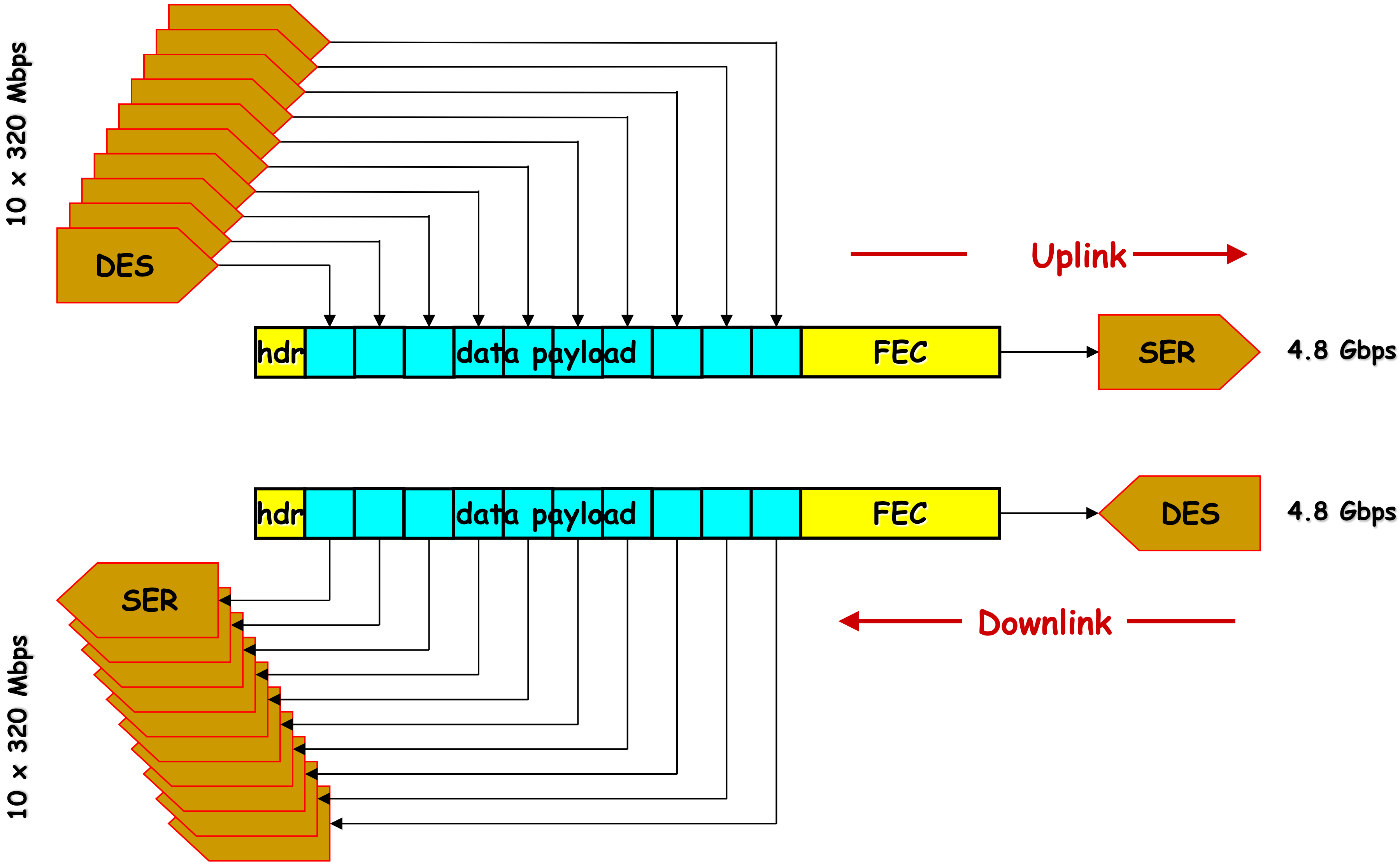


GBTx in a Nutshell 2

- GBTx
  - transports data over optical link in 120 bit frames @ 40 MHz
  - in 'transceiver; GBT frame uplink; 10x320' mode:
    - 80 bit payload data
    - 32 bit FEC
    - 8 bit frame header and slow control
  - action in each 40 MHz cycle (f_{LHC} = 40.0786 MHz)
    - Downlink
      - 80 bit data received from incoming GBT frame
      - split 80 → 10 x 8 bit
      - serialize out 8 bit on each of 10 e-ports
    - Uplink
      - 8 bit received on each of 10 e-ports
      - merge 10 x 8 → 80 bit
      - 80 bit data send with outgoing GBT fame

In short: a synchronous serial interface splitter - merger

GBTx in a Nutshell 3



Current Status DAQ

- FLES (**F**irst **L**evel **E**vent **S**elector) hardware
  - The LOEWE CSC is considered prototype for FLES
    {768 nodes with 2 x 12 cores plus a GPU; InfiniBand interconnect}
- FLIB (**FL**ES **I**nterface **B**oard)
  - Prototype hardware/firmware available from FIAS, Frankfurt
- DPB (**D**ata **P**rocessing **B**oard)
  - Architecture proposal from Warsaw University of Technology
    - µTCA based, many synergies with developments done for White Rabbit switches