BERGISCHE UNIVERSITÄT WUPPERTAL

CBM

FPGA-based subsystems at CBM

Joint CBM / PANDA DAQ workshop
19. / 20.02, 2015

Darmstadt, GSI

ASIC-based CBM readout chain

Optimal for: - high radiation levels
- large channel density
- high data rates

Example : **STS, MUCH-GEM**

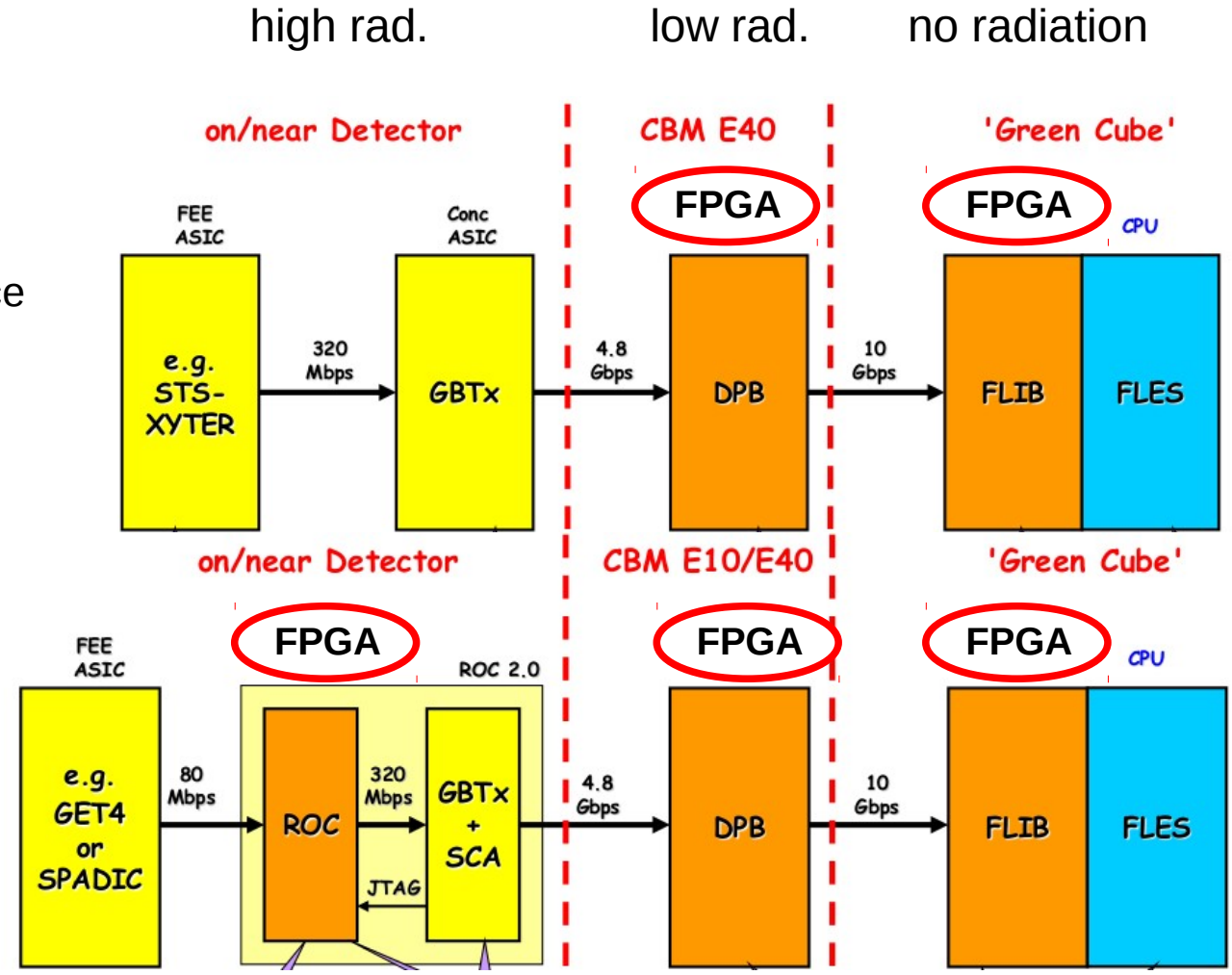
- ASIC-based front end:
  STS-xyter, MUCH-xyter
- GPTx for link aggregation
- ASIC w GPTx compatible interface

- data preprocessing in DPB
  using FPGA

Modification : eg **TOF**, TRD

- ASIC-based front end
  w/o GPTx compatible interface
- SPADIC ASIC, GET4 TDC ASIC

- additional FPGA-based
  Readout Controller in front-end
  - - for data conversion
    - data preprocessing



diagrams: W. Müller

Fully FPGA-based CBM readout chain

"Downstream" detectors: - lower channel density
- lower radiation levels

➡ no need for dedicated front-end ASIC development

Use of FPGAs allows for
- larger **flexibility**
- design iterations / updates
- standard comercial components
  "COME-and-KISS" aproach
- easily scalable solutions

Example: **RICH / PSD / ECAL**
- **fully FPGA-based** frontend:
- implement as much functiona
  On FPGA as possible

- data transport:
  TRBnet-over-GBTx
  (GBTx FPGA-core)

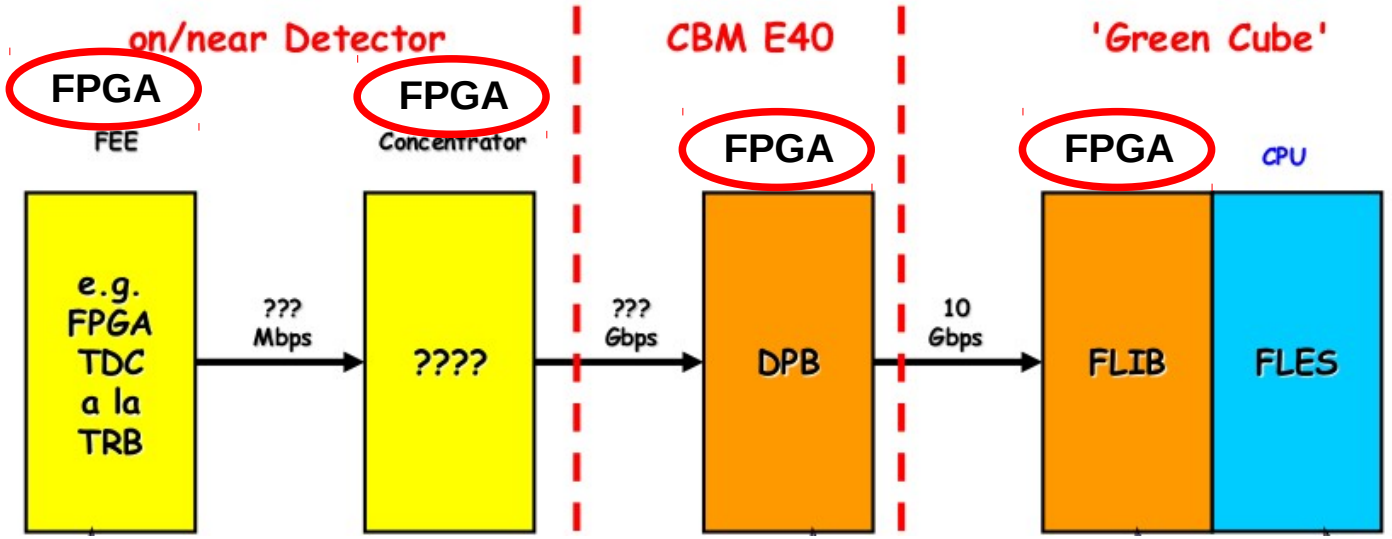
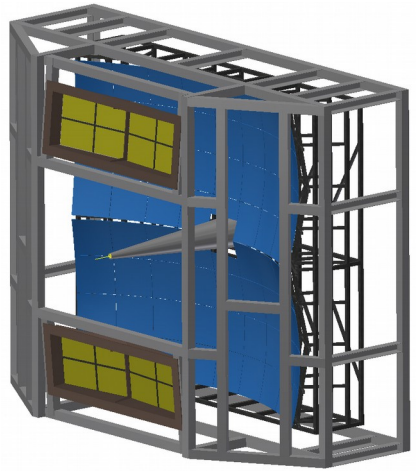


diagram: W. Müller

The RICH readout chain - example of fully FPGA-based FE

- Large CO2 gas RICH detector for e/pi separation
- Multianode Photomultiplier / MCP readout

- **Ca 55k readout channels**
- Time precision better than **500ps**
- Rough amplitude information (threshold adjustment, monitoring)
- Hitrate **up to 700kHz / channel**
- **Moderate radiation environment**
  (far away from target, outside acceptance)



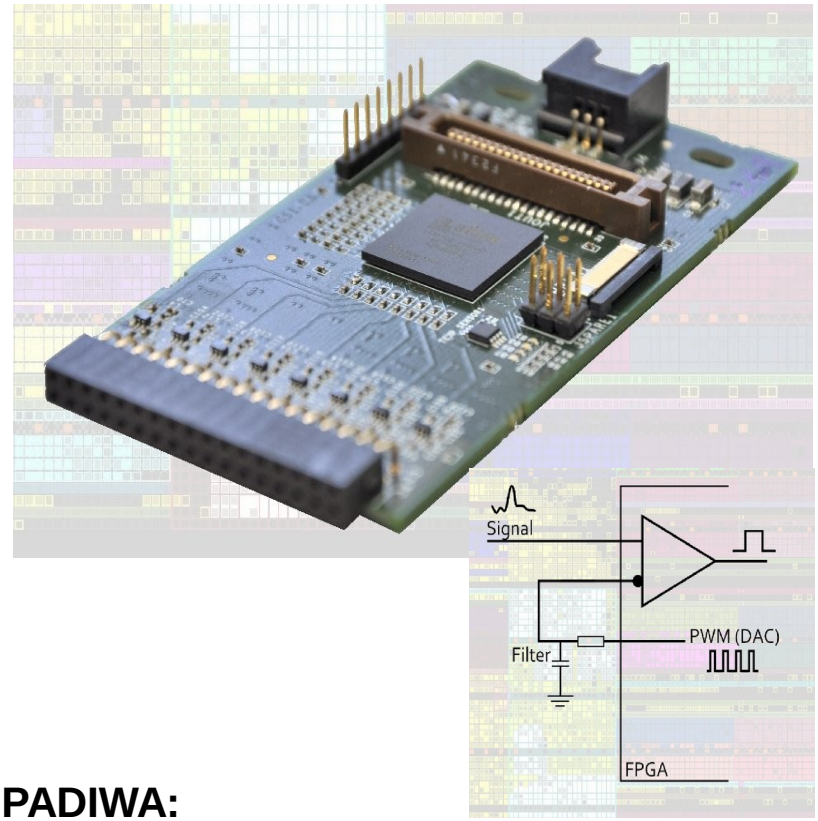
Readout principals:

- Use FPGAs in front-end for
  - **Signal discrimination** (LVDS-buffers)
  - **Time measurement** (FPGA-TDC)
  - **Data handling and control** (GPTx FPGA-core / TRBnet)

- Based on PADIWA / TRB3 development by HADES / PANDA / GSI

PADIWA discriminator + TRB3 FPGA-TDC

discriminator



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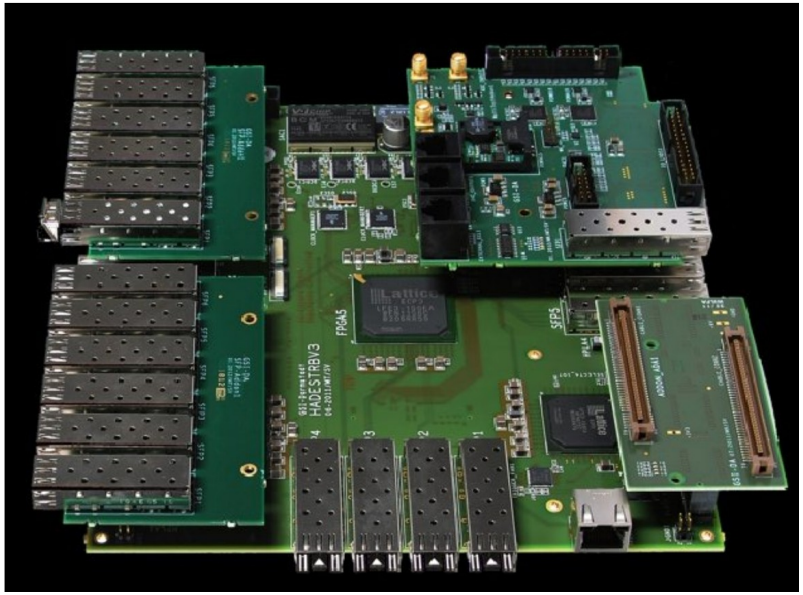
FPGA-TDC



PADIWA:

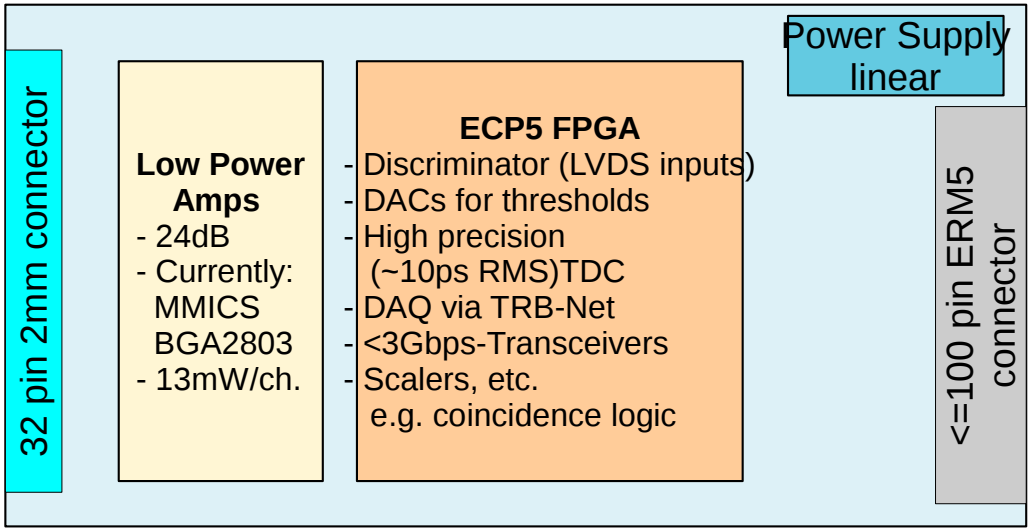
- 16ch discriminator with LVDS output
- Lattice Mach3 FPGA
- Variable broadband amplifiers to match sensor gain
- PMT or MCP readout
- Amplitude via time-over-threshold

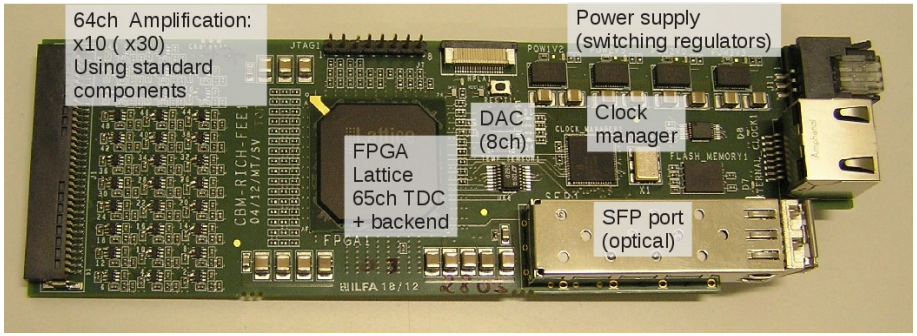
TRB3 FPGA platform:

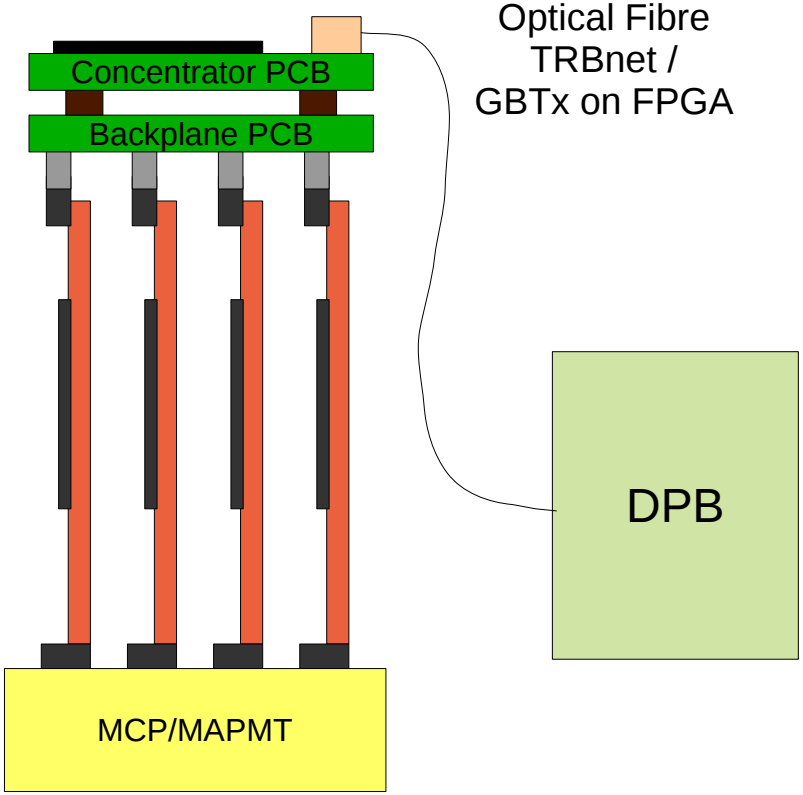
- Versatile platform containing 5 FPGAs
- 256 channel TDC
- Tapped-Delay-Line + Wave Union approach
- 17ps RMS (!) time precision
- Data handling on central FPGA
- TRBnet protocol

DIRICH development - discriminator + TDC on same FPGA

- DIRICH: Dirc / RICH readout board → synergy with PANDA !
- Combine discriminator, TDC, data handling **on same FPGA**
- Additional concentrator FPGA board







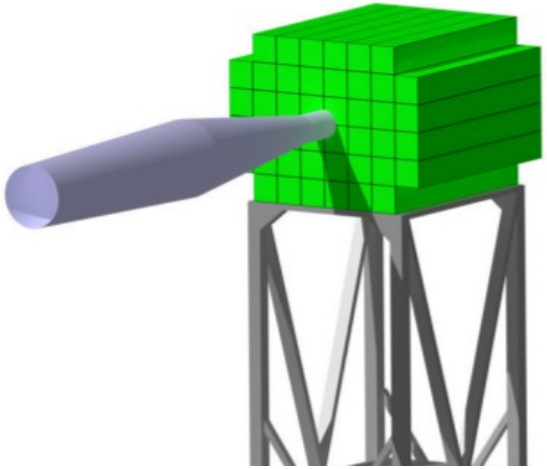
Proof of principal: TRBRICH successfully tested in beam 2012

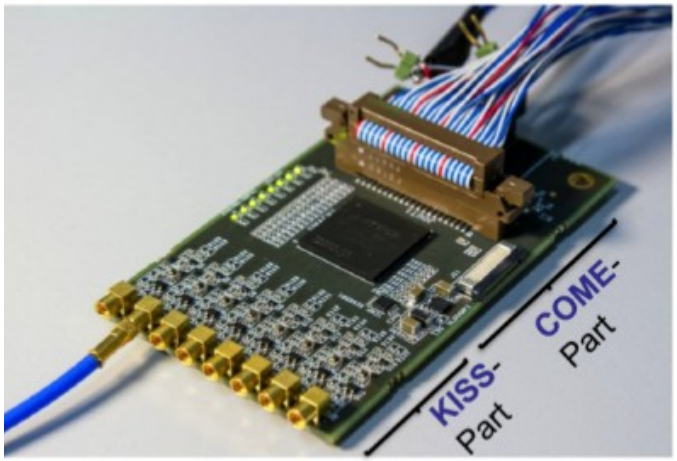
readout chain for PSD (and ECAL?)

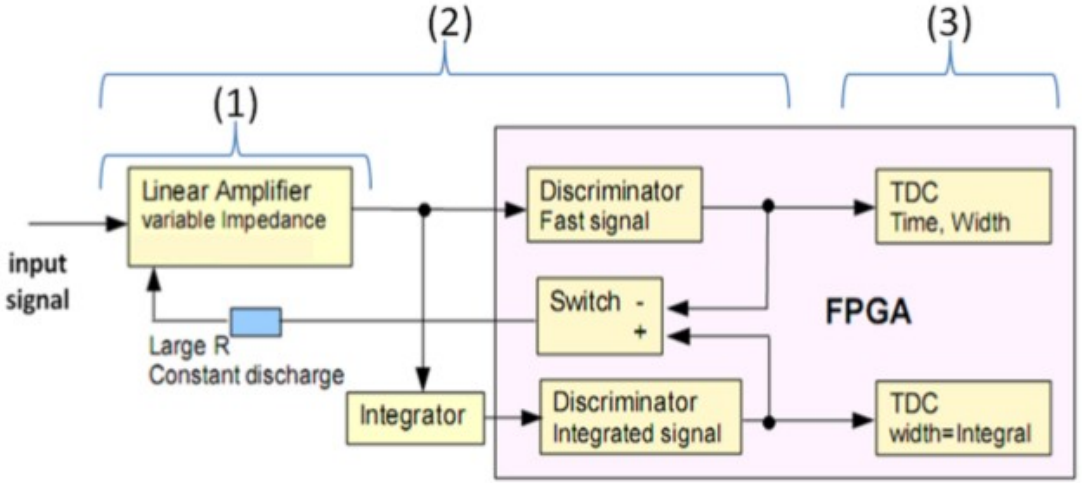
- Lead-scintillator sandwich calorimeter, last detector in setup
- 500 readout channels
- MAPD readout (Micropixel Avalanche Photodiode)

- Readout requirements:
  - **1ns timing precision**
  <1% amplitude resolution (much better than RICH)

- **Very similar aproach as for RICH !**
  - FPGA discrimination (PADIWA-AMPS)
  - FPGA-TDC ala TRB3



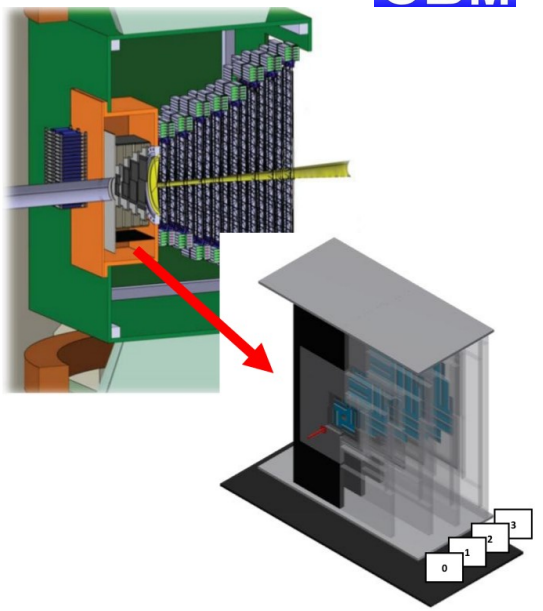




PADIWA-AMPs:

- FPGA-based Wilkinson-ADC
- 8ch input, 32 TDC channels needed
- Time precision <50ps
- Amplitude resolution: <0.5%

MVD – Micro Vertex Detector



- **MAPS** sensors – "**Monolithic active pixel sensors"**
- Closest to vertex – very high radiation dose levels, rate, ...
- **Dedicated sensor development**
- **FEE / discriminators already included** in sensor (~1000ch)

- Data readout/control **using FPGA**
- → **TRB(like) platform** for data transport
  close to MVD, via LVDS cables
  (same FPGA hardware, but no "FPGA-TDC")

- **Common readout concept for RICH / MVD / PSD / …**
  - all FPGA based subsystems

- Based on well developed **TRBnet**
- Many features already existing (used by HADES):
  - slow control, onlie monitoring, data transport, …

- Yet missing:
  - synchronization via optics

summary

- Several CBM subsystems will use **fully FPGA-based frontends**:
  RICH :
  PADIWA discrimination + **TRB3** FPGA-TDC
  to be combined on single FPGA → **DIRICH development**
  strong **synergy between PANDA and CBM** !

  PSD / ECAL:
  PADIWA-AMPs like discrimination / amplitude measurement
  same FPGA-TDC back end as for RICH, same data handling

- Other CBM subsystems **include FPGAs in FE** as readout controller (ROC), or data interface:
  MVD:
  dedicated sensor development with integrated digital FE-interface (MIMOSA)
  FPGA data interface close to detector
  based on TRB3 or derivative
  share same data handling / protocol (TRBnet) as RICH/PSD

- **TOF / MUCHstraws:**
  own FE developments (PADI ASIC + GET4 TDC)
  TRB3 based FPGA-TDC considered as possible alternative
  → then again perfect synergy with RICH / PSD / MVD