HGF-AMC for the Readout of the PANDA MVD
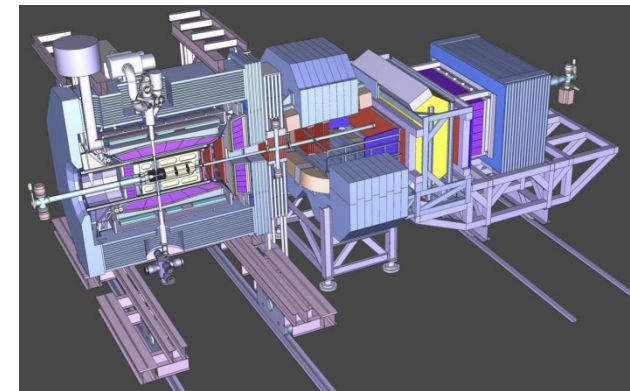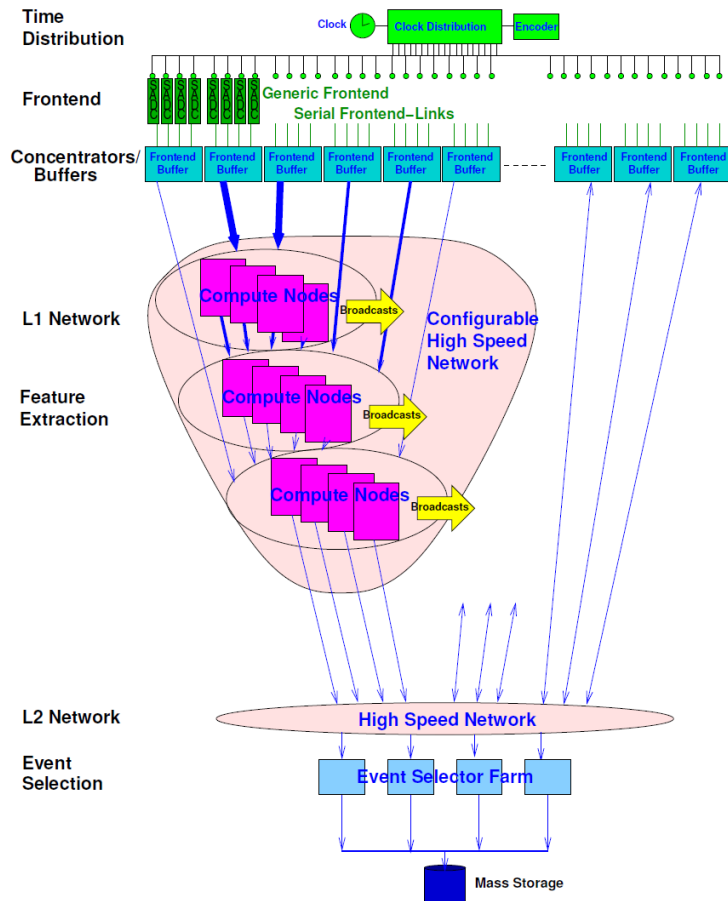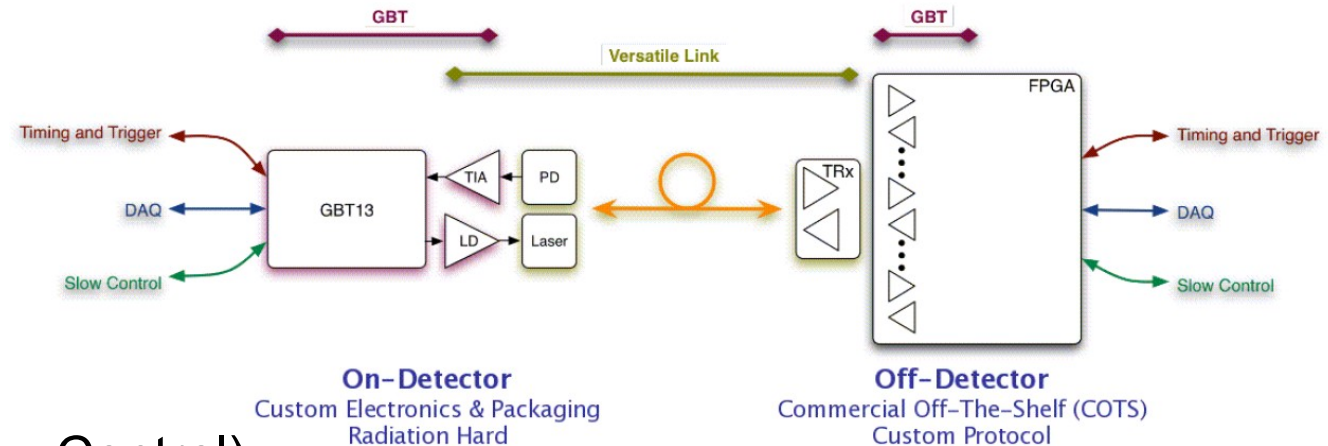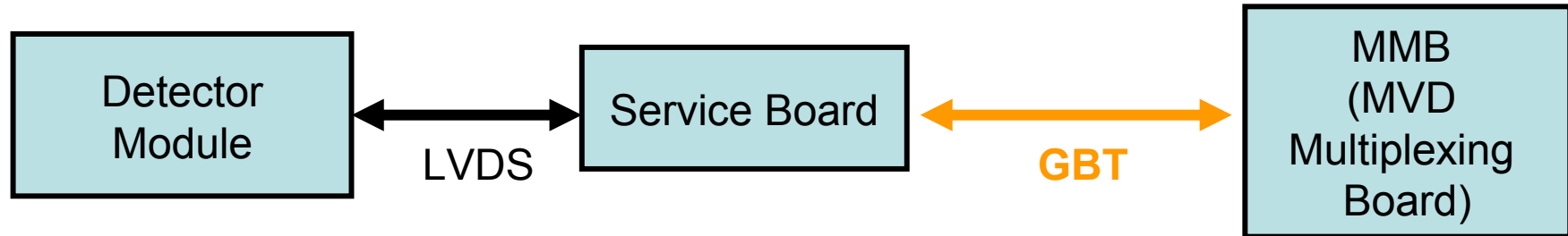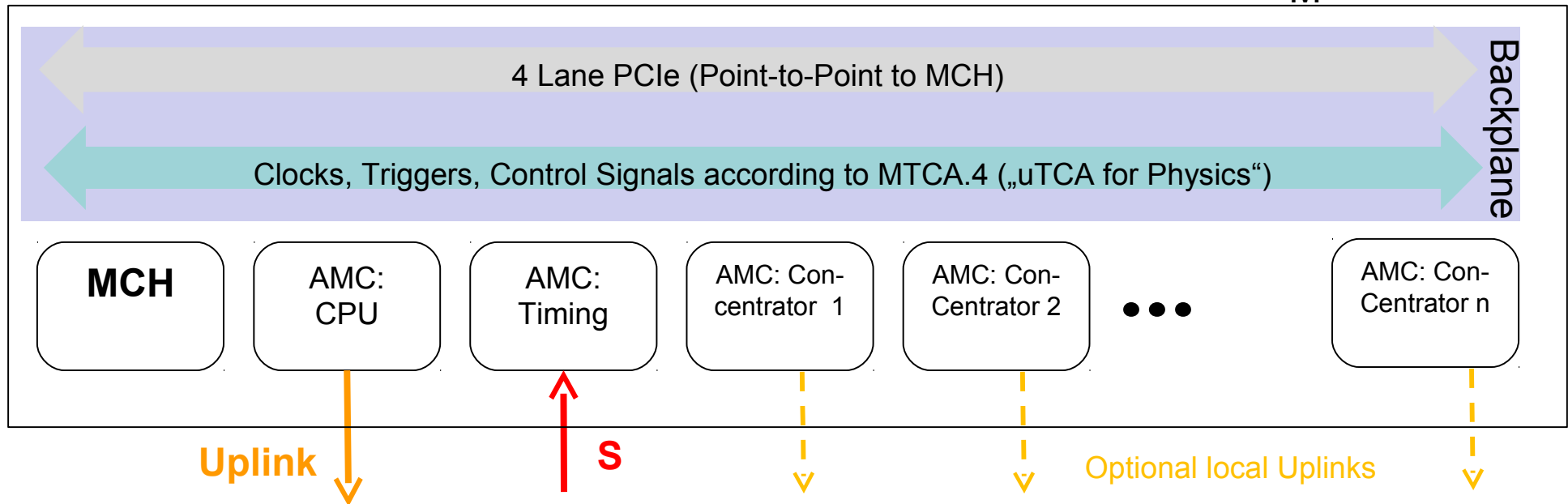
PANDA MVD Readout

- GBT:
  - Serial optical link
  - 3.36 Gb/s (incl. Slow Control)
  - Line Rate 4.8 Gb/s (Reed-Solomon Encoding)
  - Under development at CERN (Set of 4 ASICs)
  - Implementation of GBT protocol on FPGAs: Reference implementation of CERN

MicroTCA at the PANDA Multiplexing Layer

M

4 Lane PCIe (Point-to-Point to MCH)

Clocks, Triggers, Control Signals according to MTCA.4 („uTCA for Physics")

Backplane

| MCH | AMC: CPU | AMC: Timing | AMC: Con-centrator 1 | AMC: Con-Centrator 2 | ● ● ● | AMC: Con-Centrator n |

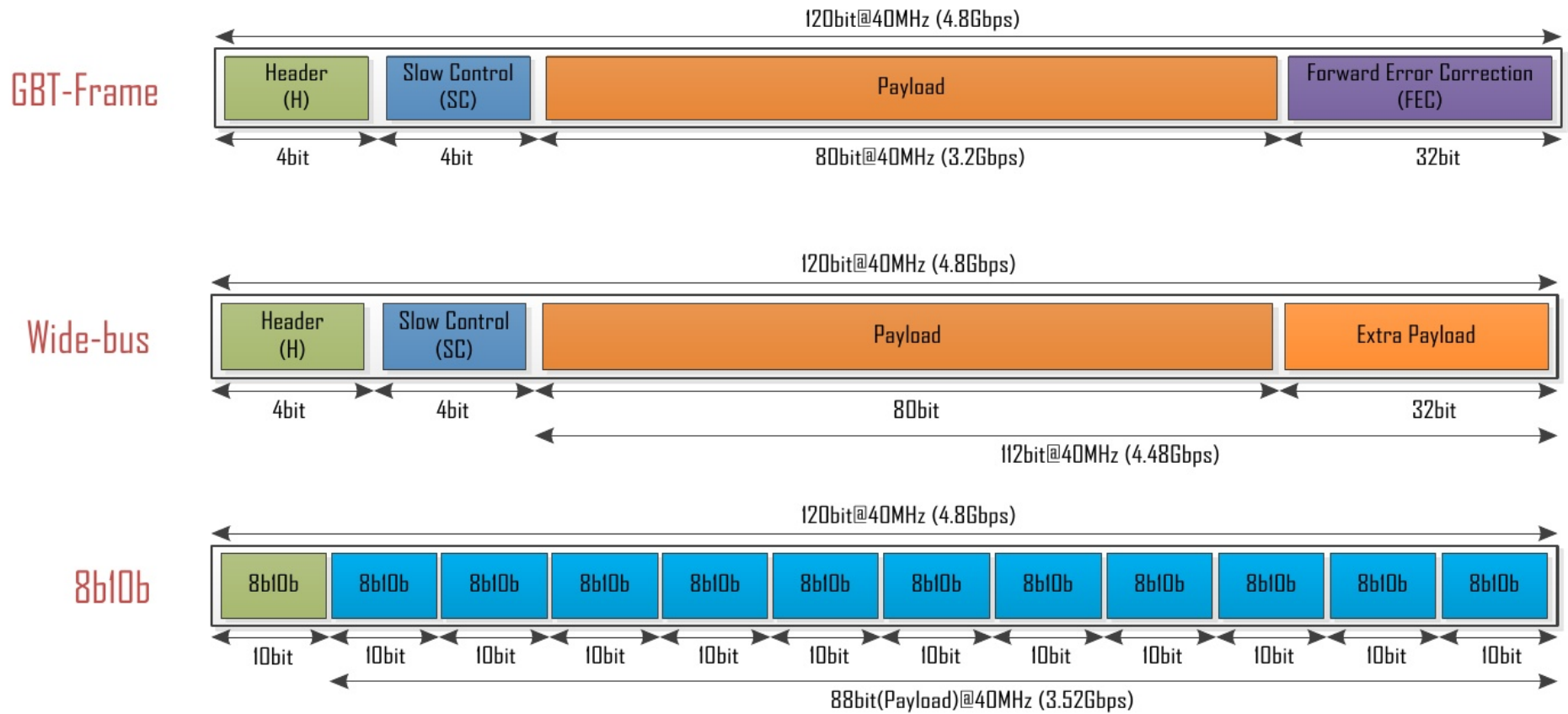**Uplink**   **S**   Optional local Uplinks

- Central input for SODA, local distribution on backplane
  - Radial clocks TCLA, TCLB or bussed clocks? performance?
- Local uplinks on concentrator AMCs for high data rate subsystems
- CPU for management + control system + uplink for low data rate subsystems

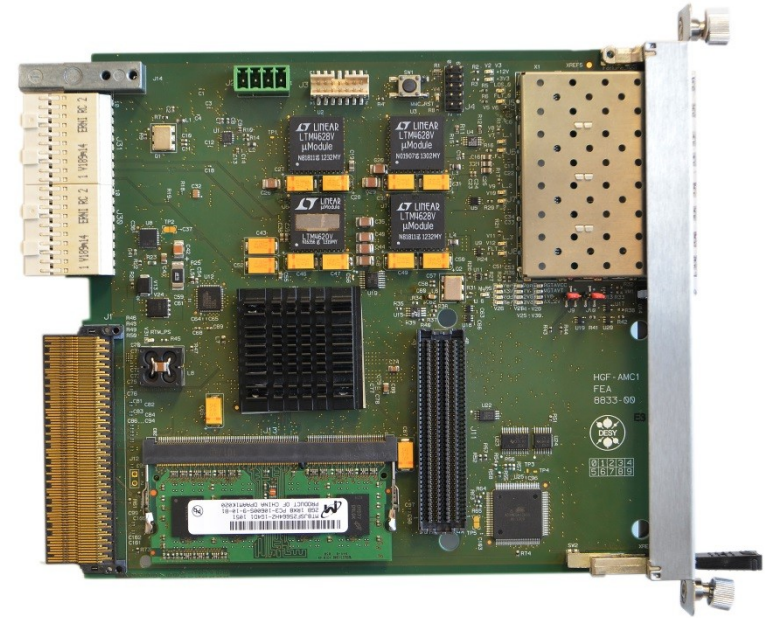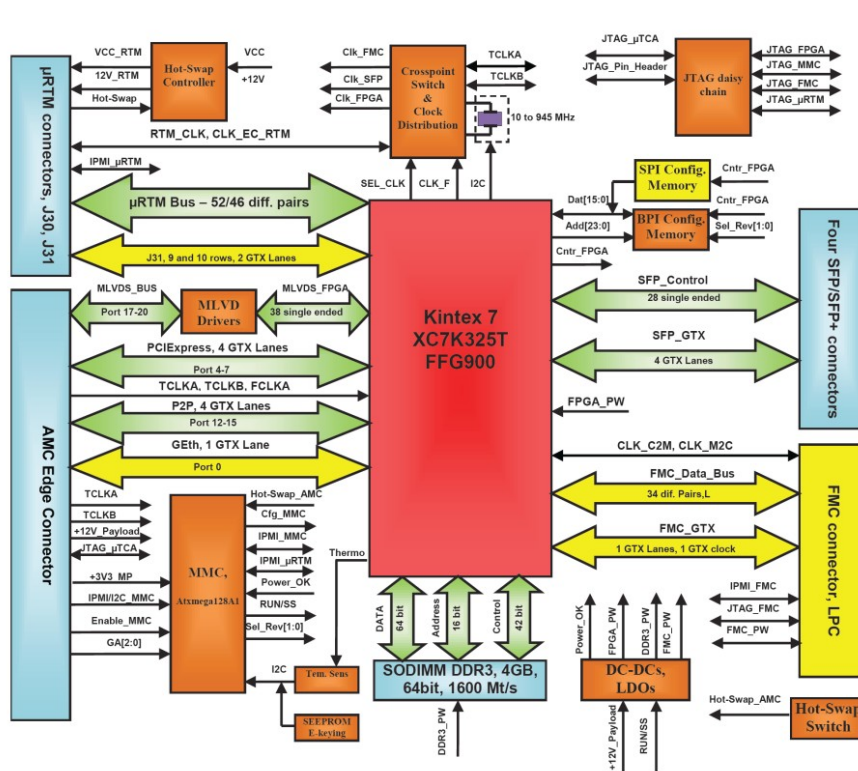# PANDA MVD Multiplexing Board (MMB)
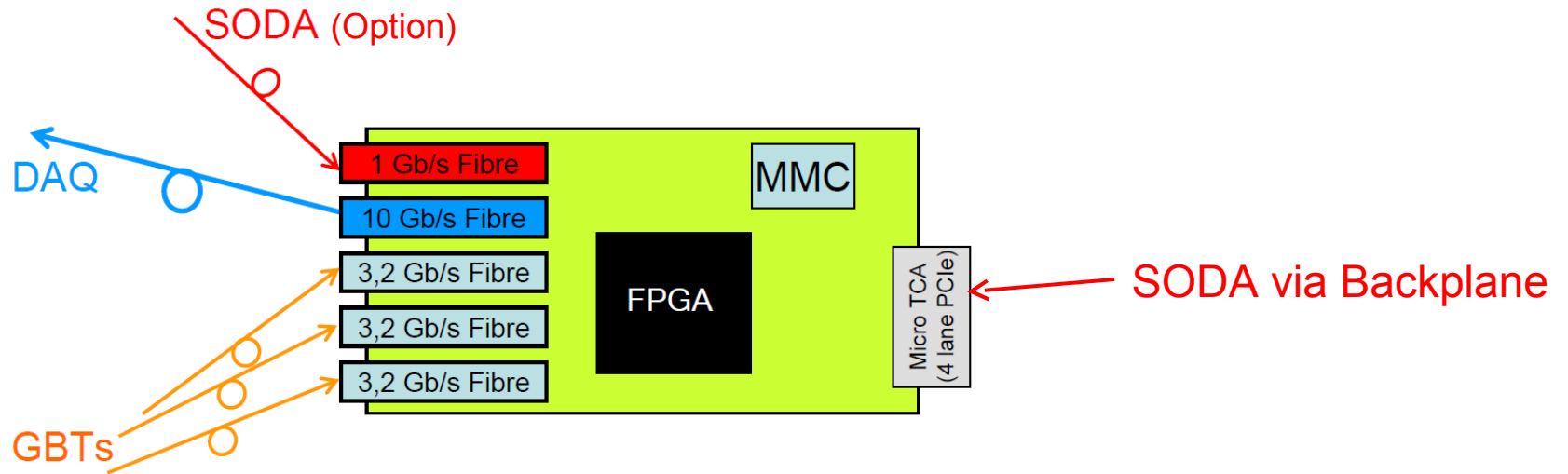
- Technical implementation: HGF-AMC
- FPGA implementation tasks:
  - GBT protocol
  - Uplink protocol
  - Mapping between both
  - SODA
 - PCIe (for control and montioring tasks)

GBT frame types

GBT-Frame

120bit@40MHz (4.8Gbps)

Header (H)	Slow Control (SC)	Payload	Forward Error Correction (FEC)

4bit — 4bit — 80bit@40MHz (3.2Gbps) — 32bit

Wide-bus

120bit@40MHz (4.8Gbps)

Header (H)	Slow Control (SC)	Payload	Extra Payload

4bit — 4bit — 80bit — 32bit

112bit@40MHz (4.48Gbps)

8b10b

120bit@40MHz (4.8Gbps)

8b10b	8b10b	8b10b	8b10b	8b10b	8b10b	8b10b	8b10b	8b10b	8b10b	8b10b	8b10b

10bit — 10bit — 10bit — 10bit — 10bit — 10bit — 10bit — 10bit — 10bit — 10bit — 10bit — 10bit

88bit(Payload)@40MHz (3.52Gbps)

Preparations for the Preassembly Phase: Phase 2
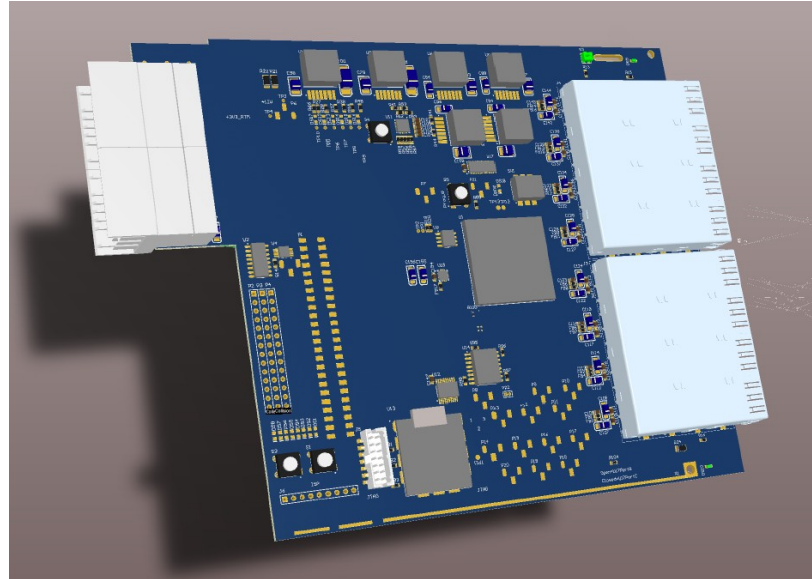

HGF-AMC
(DESY/KIT)

- MicroTCA.4 board developed in HGF Portfolio "Detector Technologies"

- Based on Kintex 7 (4 GTX lanes to Front Panel)

- Directly usable as MVD Multiplexing Board

- FPGA code from Phase 1 can be reused
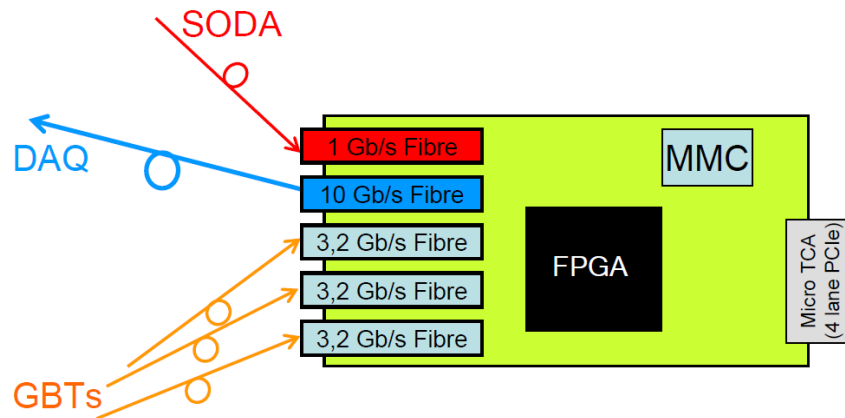
HGF-AMC (MTCA.4)
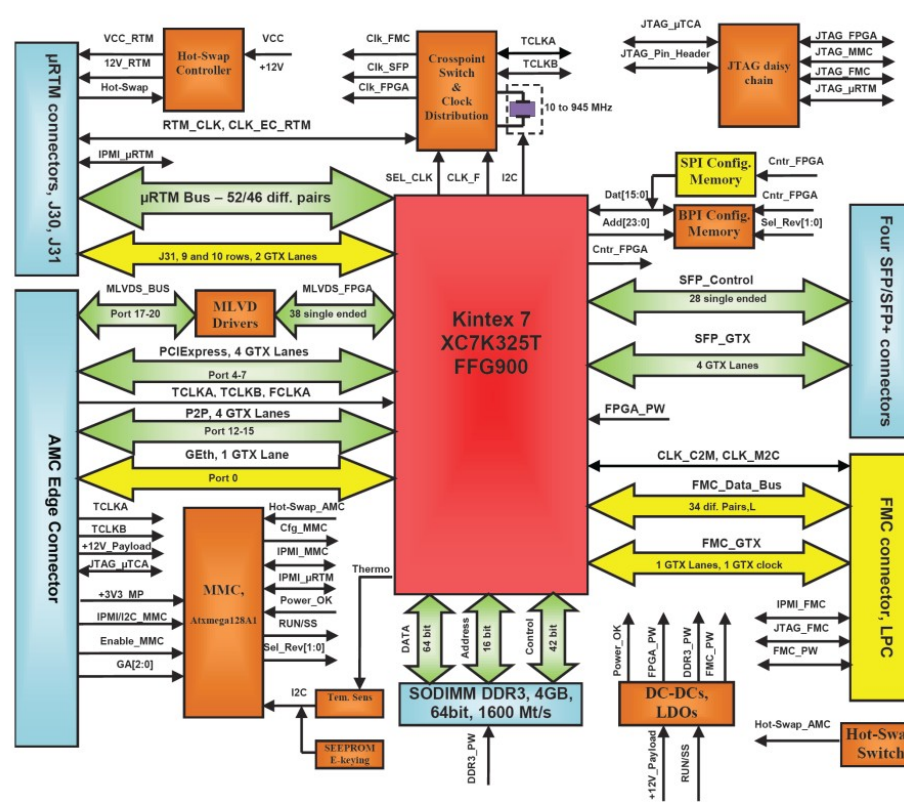
Entwicklung von DESY / Kit

Rear IO Module for the HGF-AMC

- Increase of multiplexing level
- 8 GTP Transceivers
- Based on Artix7 for the mapping to the parallel interface to the HGF-AMC
- Status: Layout
- First prototype expected in January

Preparations for the Preassembly Phase: Phase 1

SODA

DAQ

GBTs

1 Gb/s Fibre

10 Gb/s Fibre

3,2 Gb/s Fibre

3,2 Gb/s Fibre
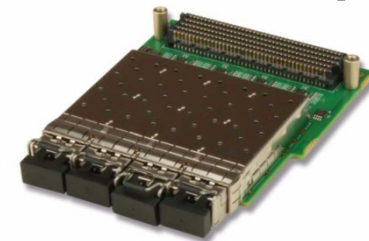
3,2 Gb/s Fibre

MMC

FPGA

Micro TCA (4 lane PCIe)
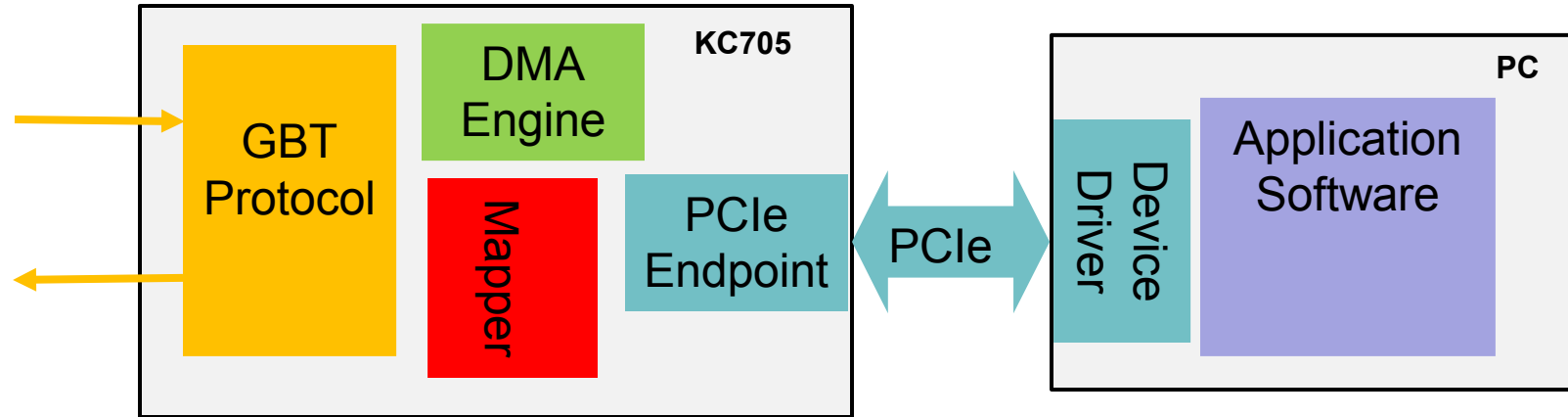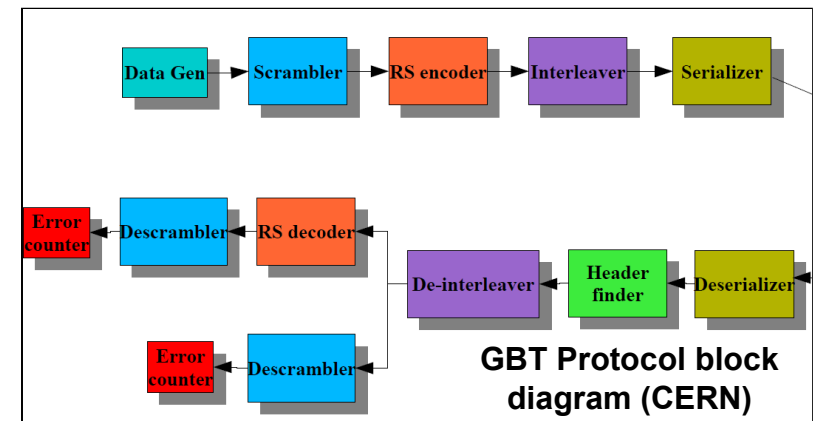
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Xilinx KC705

+

Vadatech FMC105 Quad SFP+

- Implement MVD Multiplexing Board with KC705
- Focus: FPGA Code
- Uplink Protocol has to be defined!

Development Tasks for GBT protocol on KC705

- Major Effort: FPGA code
  - PCIe
  - DMA-Engine: Commercial core?
  - Mapping????

GBT Protocol block diagram (CERN)

- GBT protocol should be straight forward, based on a reference implementation from CERN