Current STS Readout Concept

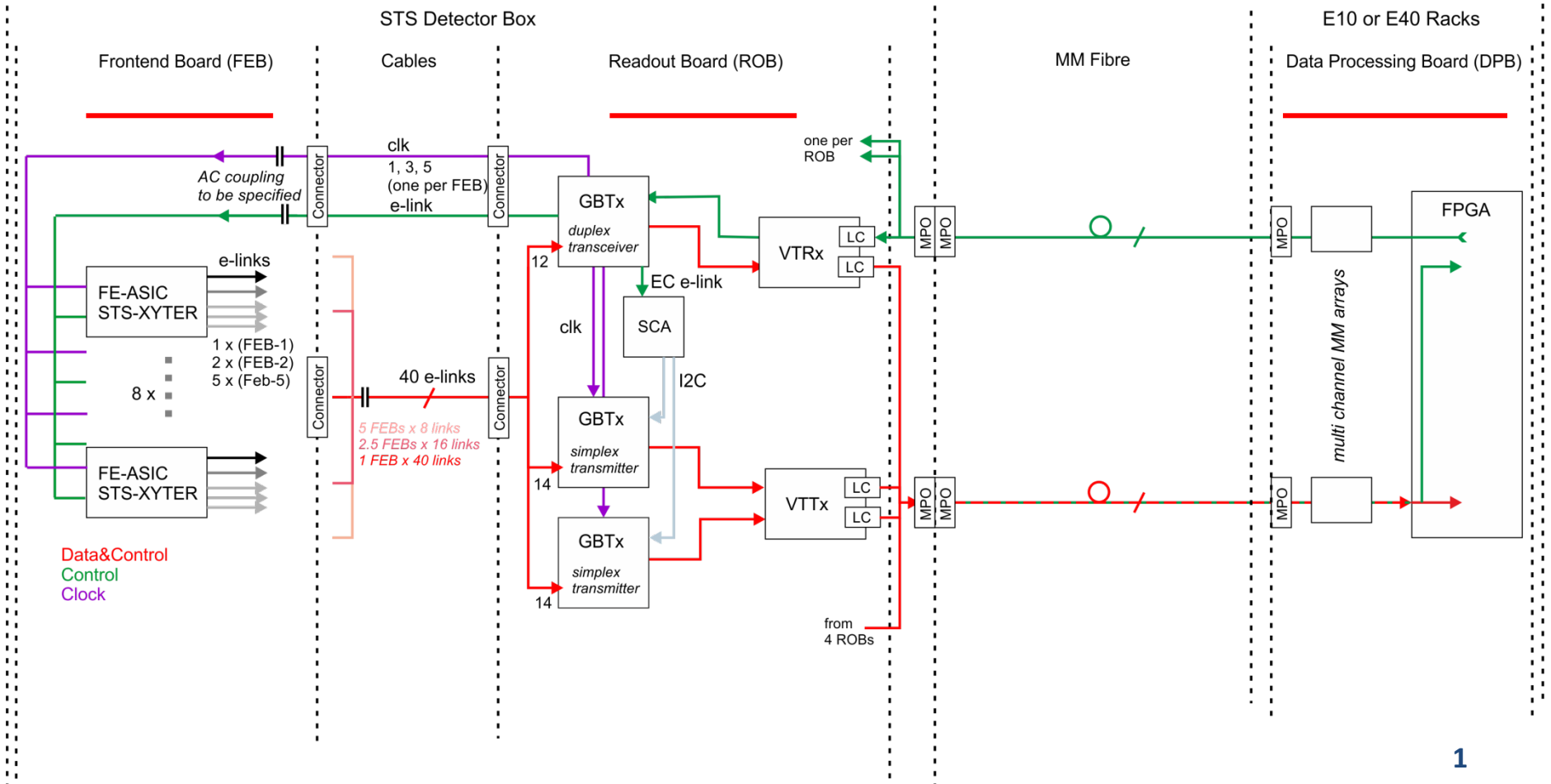
FEB
8 STS-XYTER

Electrical Interface
SLVS/LVDS
10-42 pairs/FEB

ROB
GBTx / VL

Optical Interface
4 MM fibers /ROB

DPB



STS Readout Board (ROB)

1 master GBTx connected to 1 VTRx transceiver
- Slow control, clock distribution
- Data readout

2 slave GBTx connected to 1 VTTx (twin transmitter)
- Data readout, control responses

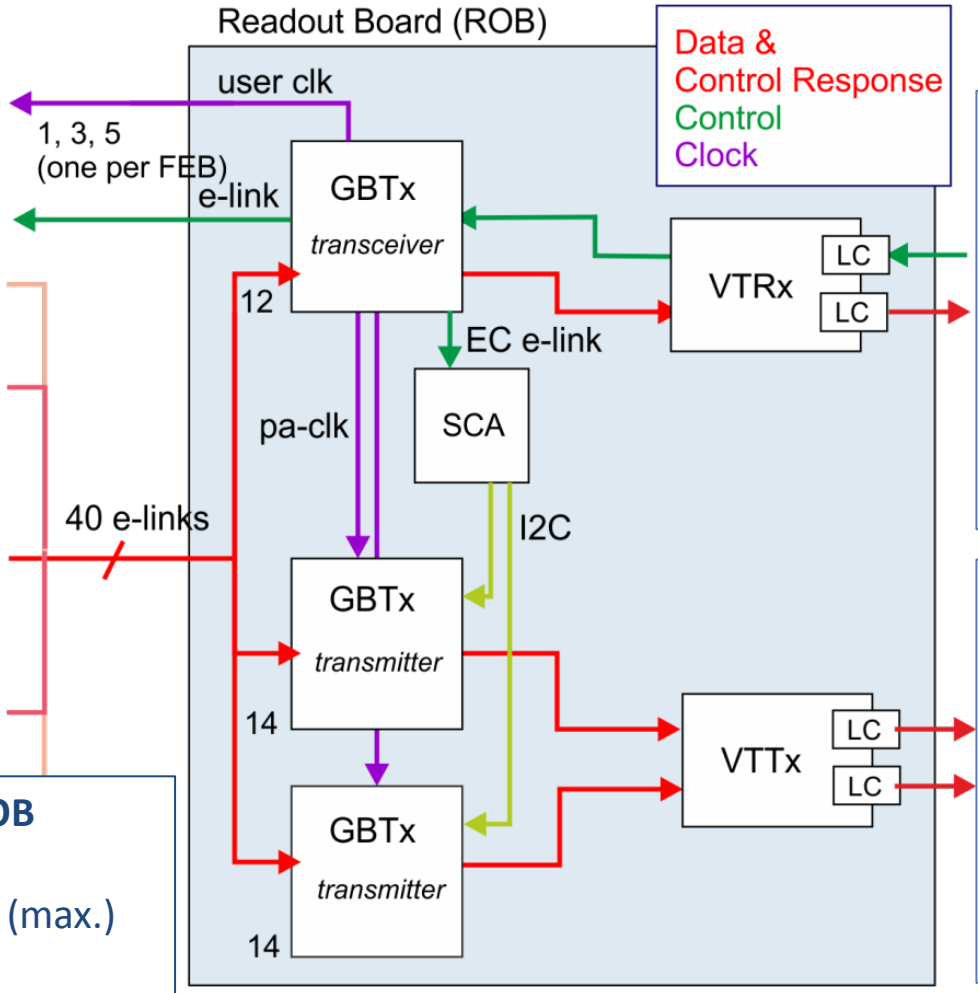
1 SCA as slow control interface from master to slaves

Frontend Side

Clock and Slow Control:
- single clock and slow control downlink to each FEB
- multidrop to 8 ASICs

Input from FEBs:
- 3x14 = **42 e-links@320Mbps**
- GBTx wide bus mode
- input bandwidth 13.44 Gbps

Minimized number of FEB-ROB connections:
on FEB side from 8+2 to 40+2 (max.) differential pairs

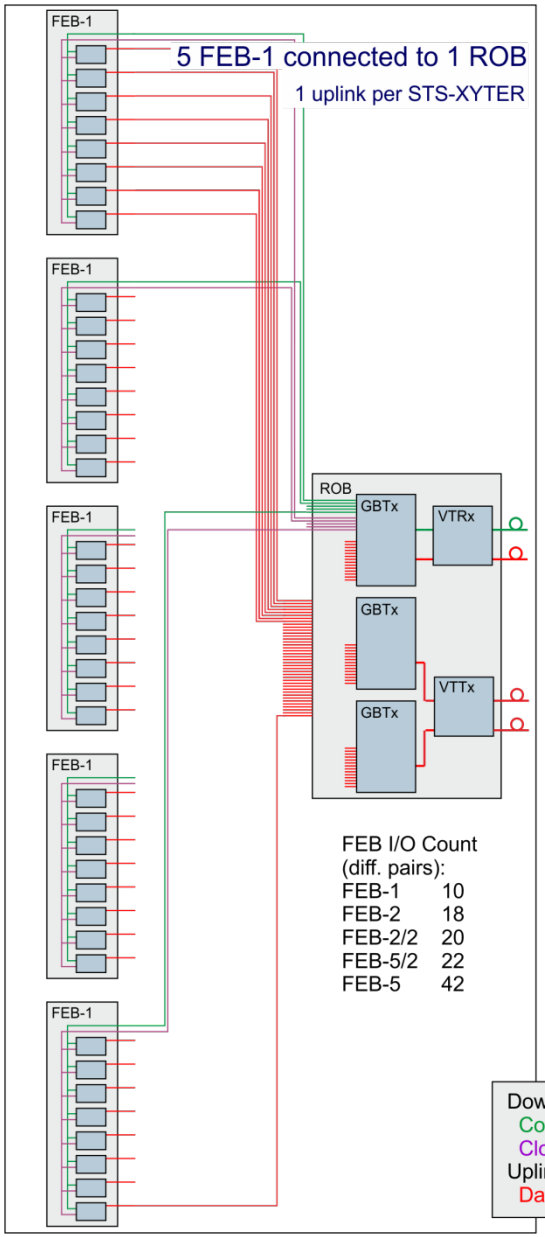


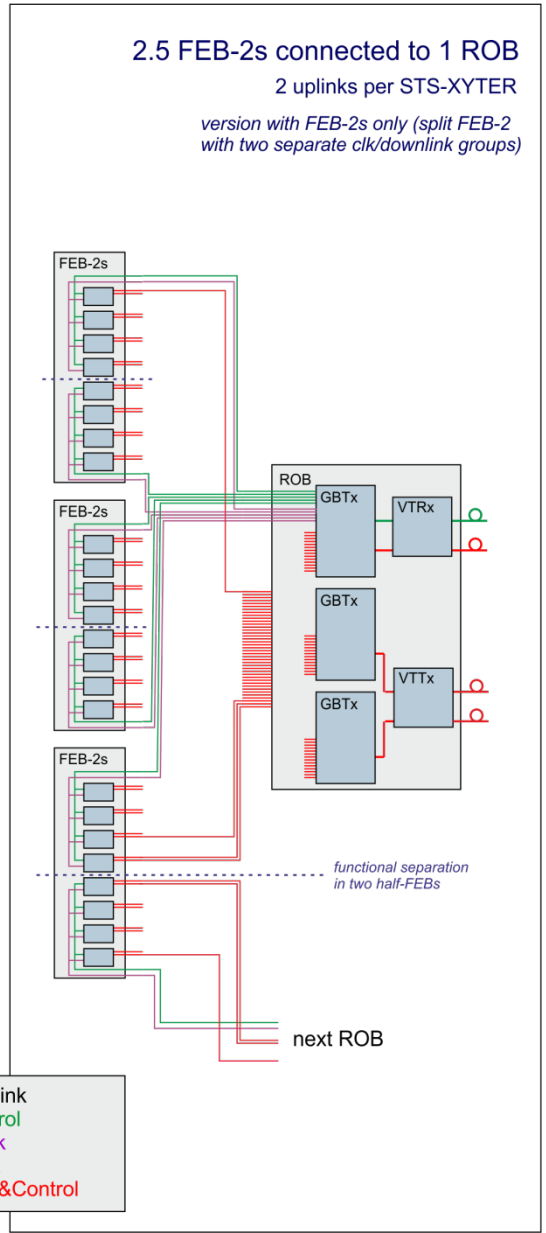
Backend Side

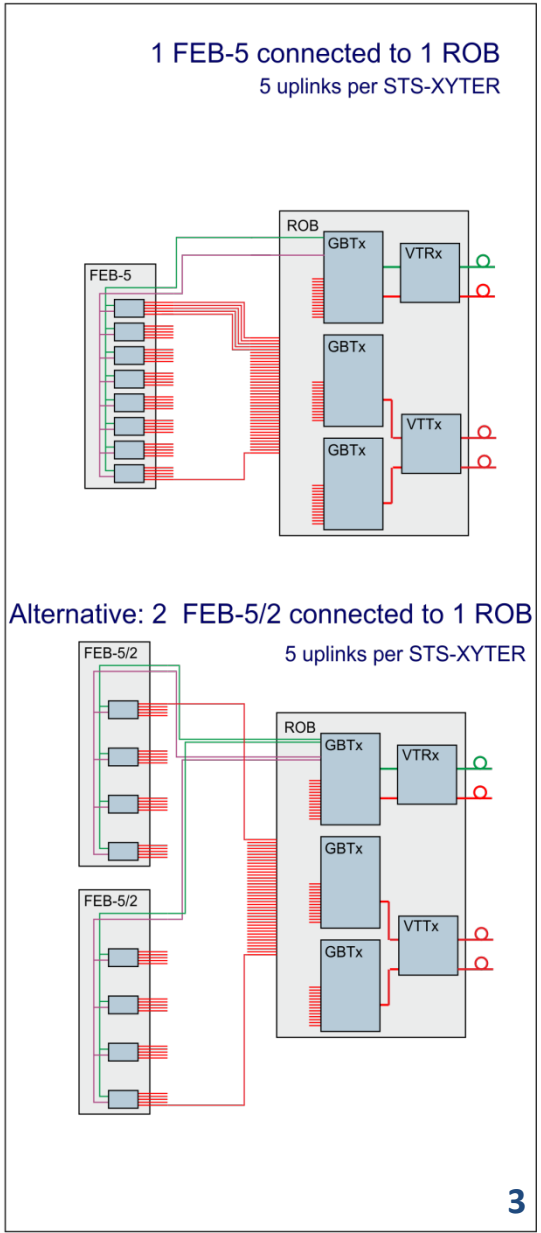
Output to DPBs:
- 1 VTRx, 1 VTTx
- **1 downlink**
- **3 uplinks**
- user bandwidth 3x4.48 = **13.44 Gbps**

SCA:
- I2C masters for slave GBTx control
- Use additional slow control features?

FEB Types and ROB Connectivity







Common CBM ROB Prototype

Alternative approach: **common CBM GBT prototype board**

- **Full GBTx/VL functionality** for all readout chains (STS-XYTER, GET4, SPADIC2,..)
- **frontend connectivity** (GBTx E-Links, SCA) routed to **FMC connector**

  → projects need individual interface FMCs