

#### **Prometeusz Jasinski**

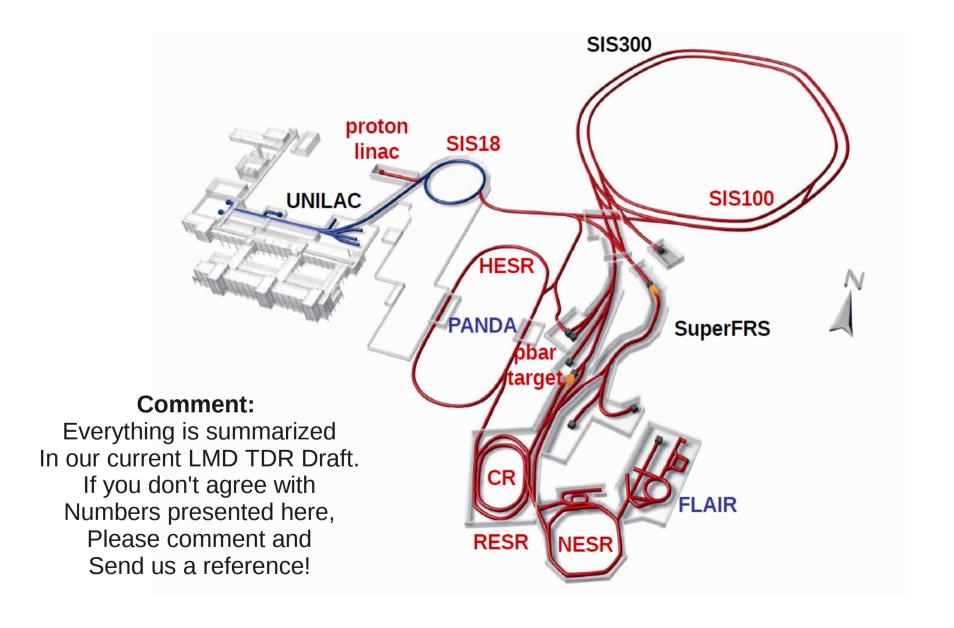
For the PANDA luminosity detector group 09.12.2014
Collaboration meeting: DCS



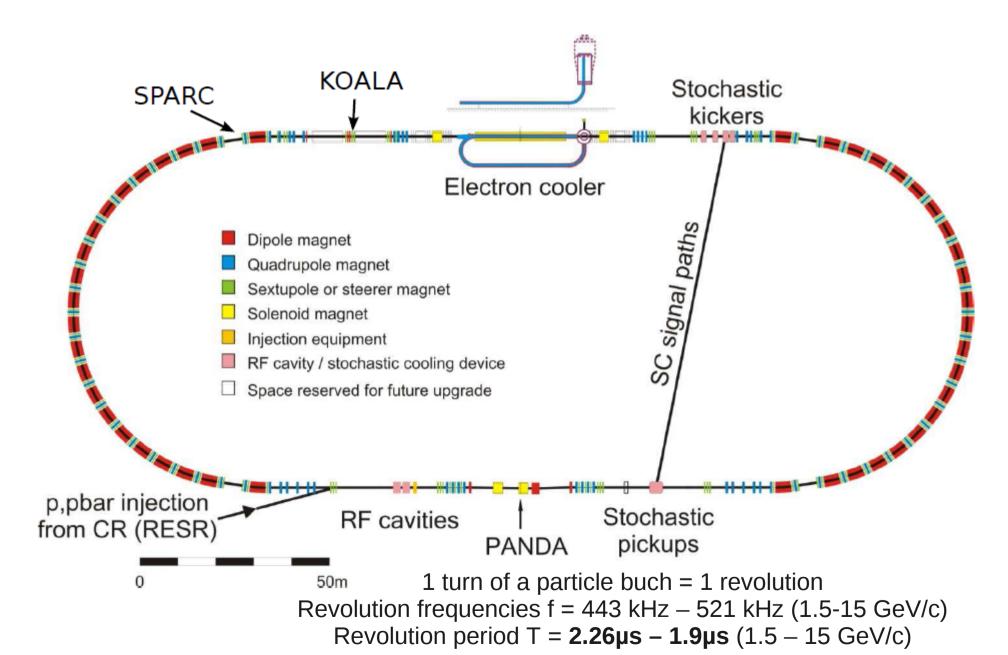


Helmholtz-Institut Mainz

## Some "facts" on HESR

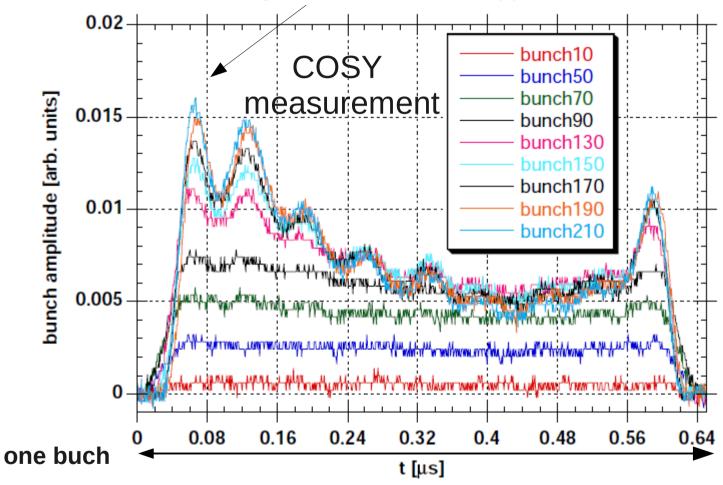


## Some "facts" on HESR



### Bunch Structure in Barrier Bucket Mode (Physics at PANDA)





MOPD068

Proceedings of IPAC'10, Kyoto, Japan

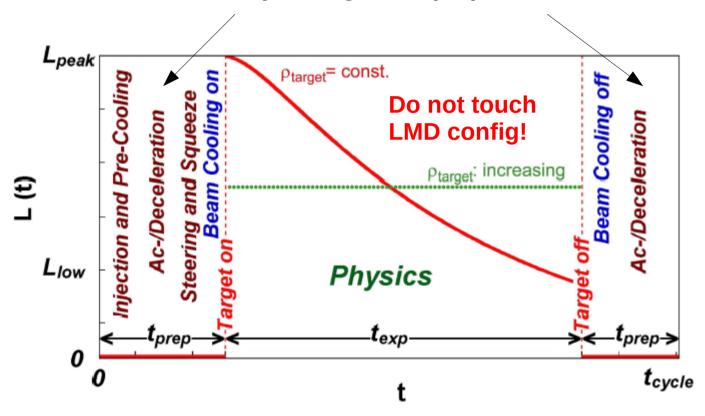
STOCHASTIC MOMENTUM COOLING EXPERIMENTS WITH A BARRIER BUCKET CAVITY AND INTERNAL TARGETS AT COSY-JUELICH IN PREPARATION FOR HESR AT FAIR

PANDA future conditions: DC beam with a fill factor of 80%

H. Stockhorst, R. Maier, D. Prasuhn and R. Stassen, Forschungszentrum Jülich GmbH, Germany T. Katayama, Tokyo

# The Luminsity Profile

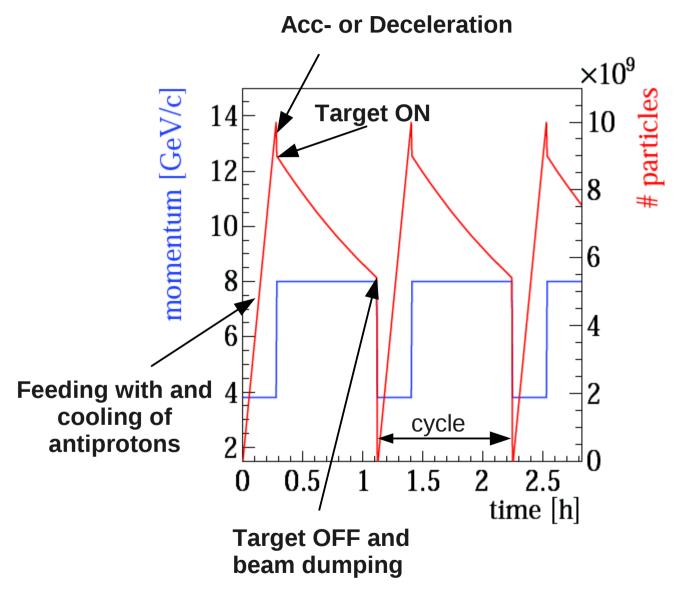
# LMD Configuration only during beam preparation!



 $t_{exp} = 9.5 \text{ min} - 32 \text{ min}$ ;  $t_{prep} = 2 \text{ min} - 5 \text{ min}$ 

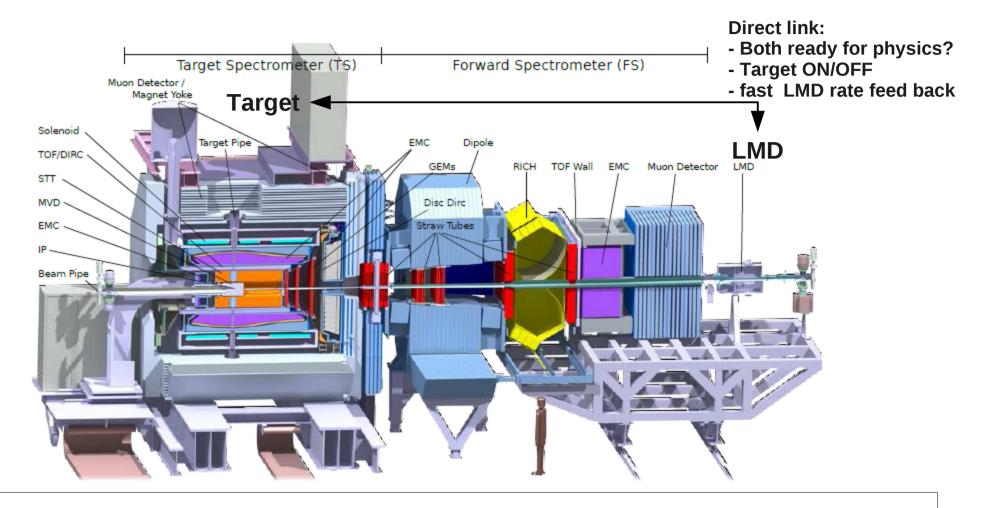
Well, this is the operation WITH the RESR. But we won't have the RESR for quite a long time.

# **HESR** cycles without RESR



 $t_{exp} = 26 \text{ min} - 65 \text{ min}$ ;  $t_{prep} = 19 \text{ min} - 22 \text{ min}$ 

## The Luminosity Detector and PANDA@HESR

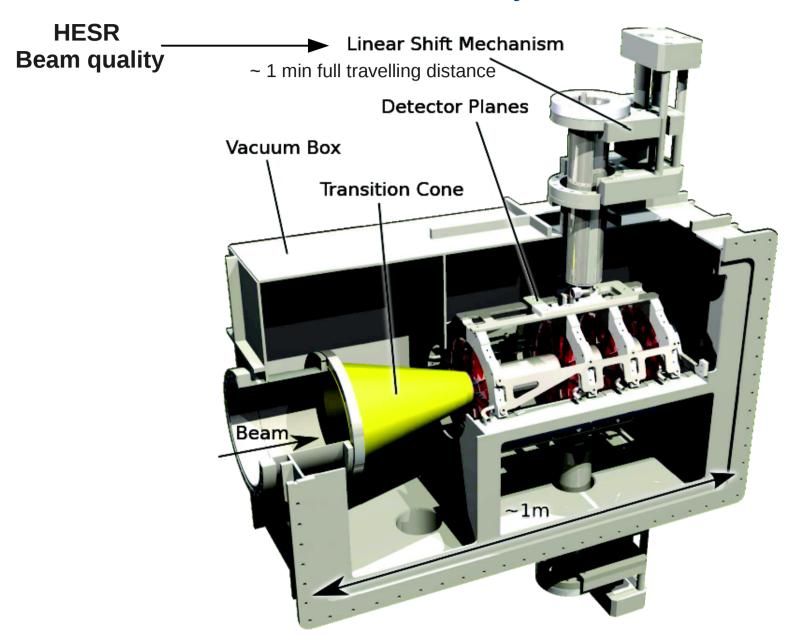


Below 3.8 GeV/c Solenoid field must be reduced down to 1T for 1.5 GeV/c Dipole field is ramped by HESR according to the beam momentum

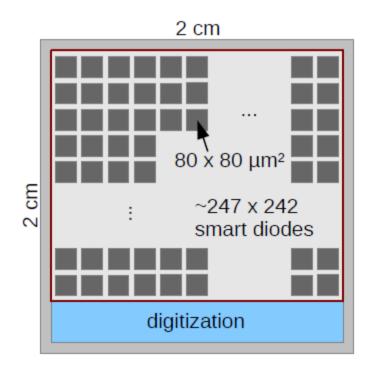
→ Offline access to the dipole field strength at ANY physics data taking time required!

→ PANDA Hall probe → DCS?

# The Luminosity Detector



### **LMD Sensors**



type	pads	traces on	description
		module flex cable	
data	6	4	data output (LVDS @ 800 Mbps)
clock	2	2	system clock (LVDS @ 40 MHz)
SPI	4	4	Slow control
ground	10	6	GND
low voltage (LV)	5	1	high current 1.8 V
LV sense	1	1	sense line low voltage
VSSA	1	1	analog voltage 1.5 V
HV	2	2	60 V
Temperatur	2	2	NTC on chip
Fast reset	2	2	synchronized reset (LVDS)
Test pulse	2	2	test pulse
Reset	2	2	asynchronous reset
Monitor	2	2	discriminator output
Total	41	31	

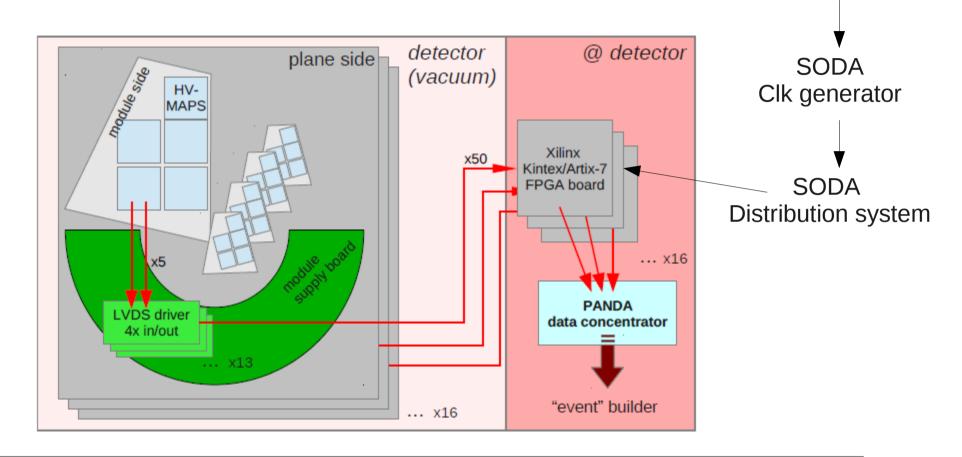
Table 3.1: Overview of number and usage of PADs on the HV-MAPS.

Figure 3.4: Simplified layout of the final HV-MAPS design (Not to scale)

In total 400 HV-MAPS in the LMD Send time information of hits encoded with a gray counter at 40MHz (25ns)

## DAQ of HV-MAPS

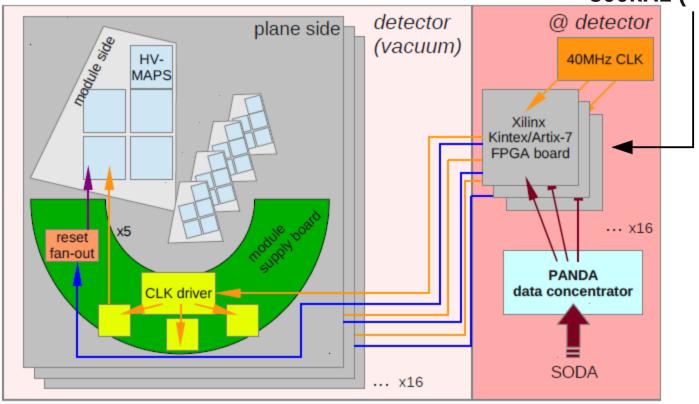
# **HESR** burst number or revolution signal?



Delay between LMD hits → FPGA board ~ 1µs Delay between HESR signal → FPGA board = ? → **Specifications needed here!** 

### DCS of HV-MAPS

HESR burst signal ~ 500kHz (= rev frequ)



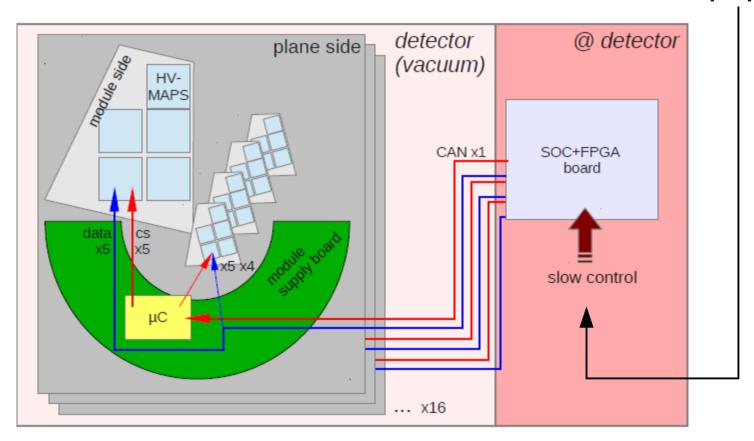
40 MHz clk signal (most probably) directly coupled to SODA 160MHz clk Synchronous Reset of gray counters on the HV-MAPS:

Fast resets within one ~ 400 ns long burst gap!

→ Direct link to HESR monitoring equipment with low jitter and well known timing specifications needed! (analogue signal of beam current pickup?)

#### DCS of HV-MAPS

#### **HESR** preparation



~ **15 MB** of sensor settings via SOC+FPGA board configuration during preparation time in an HESR cycle In the worst case **only 2 min** available for configuration and we are not the only ones in PANDA!

 $\rightarrow$  HESR information of middle priority

# Prior to Specifications / DB design : Requirements

See the table...