

# Structure of ADC-based DAQ-system

PANDA Collaboration Meeting Dec 2014

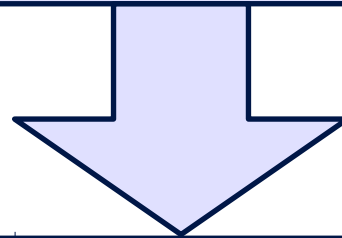
A. Erven

# Background

- Existing Hardware:  
ADC-Modules with 16  
channels and proprietary  
crate system

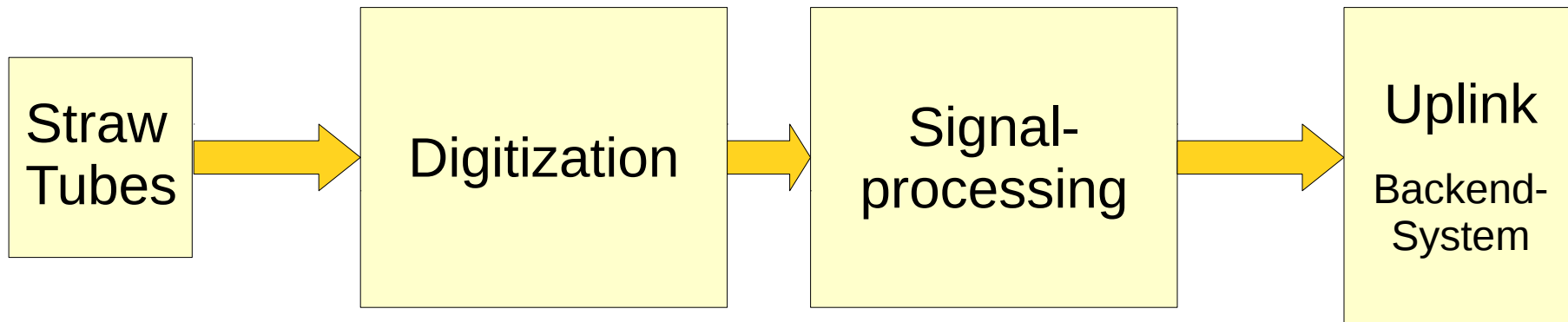


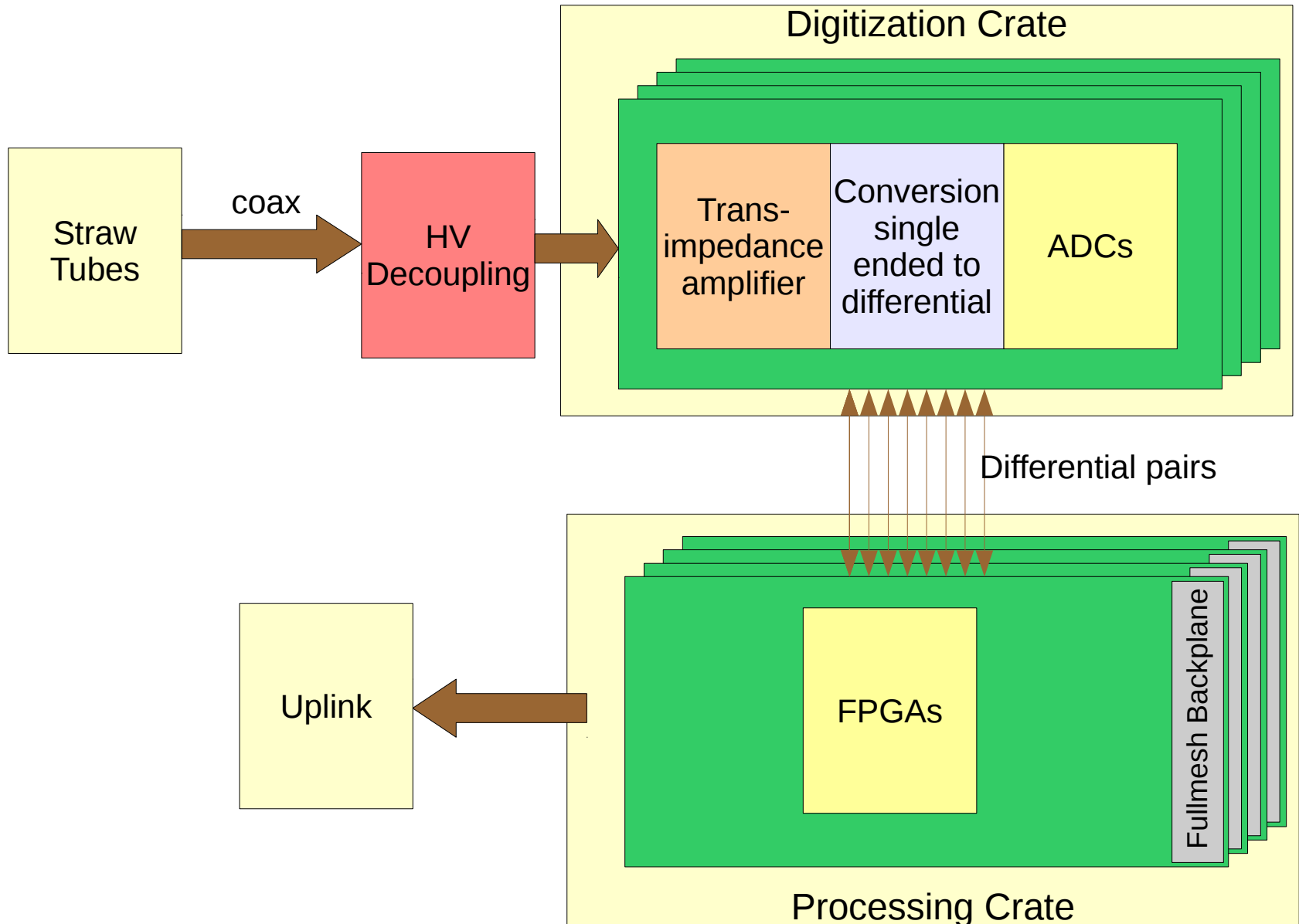
- For 4636 channels of PANDA STT, ~ 20 Crates and ~ 300 Modules would be needed
- Performance of Processing- and Datatransfer not feasible

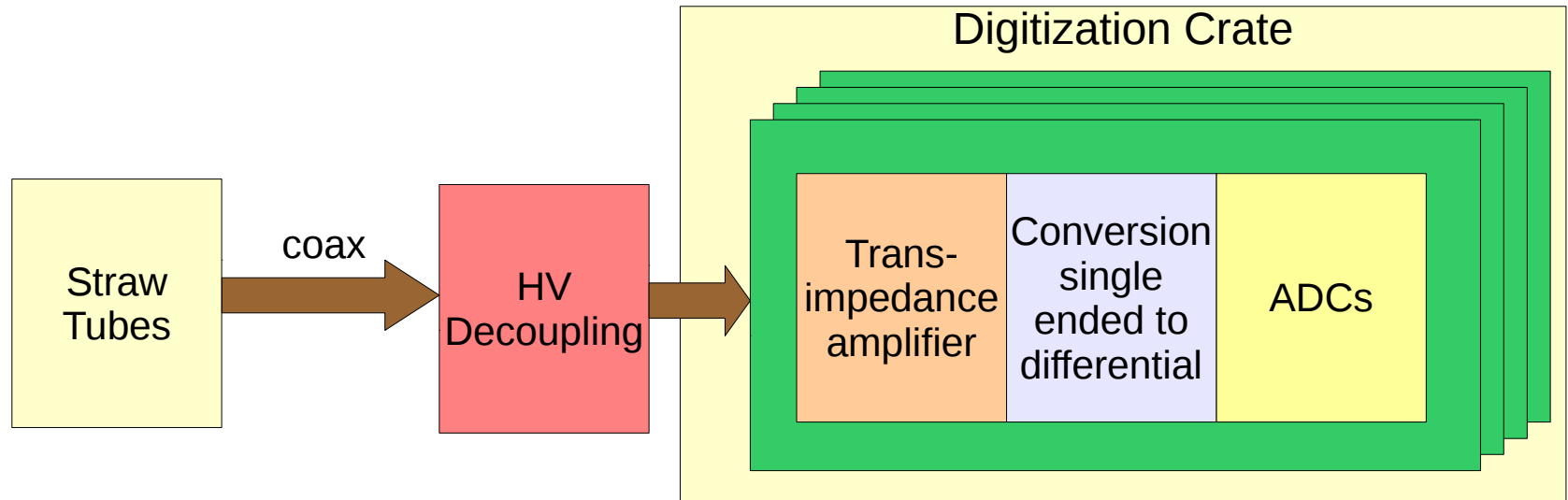


- High integration
- Move Processing from Backend to Firmware

- Division of Digitization and Signal-processing into 2 Crates

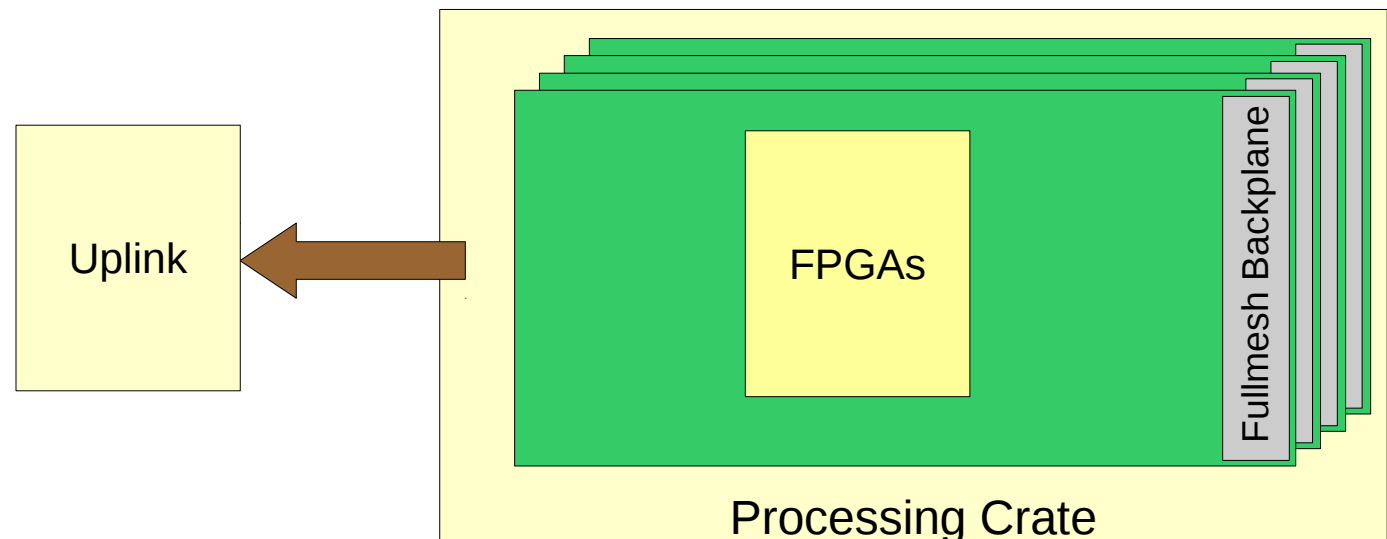




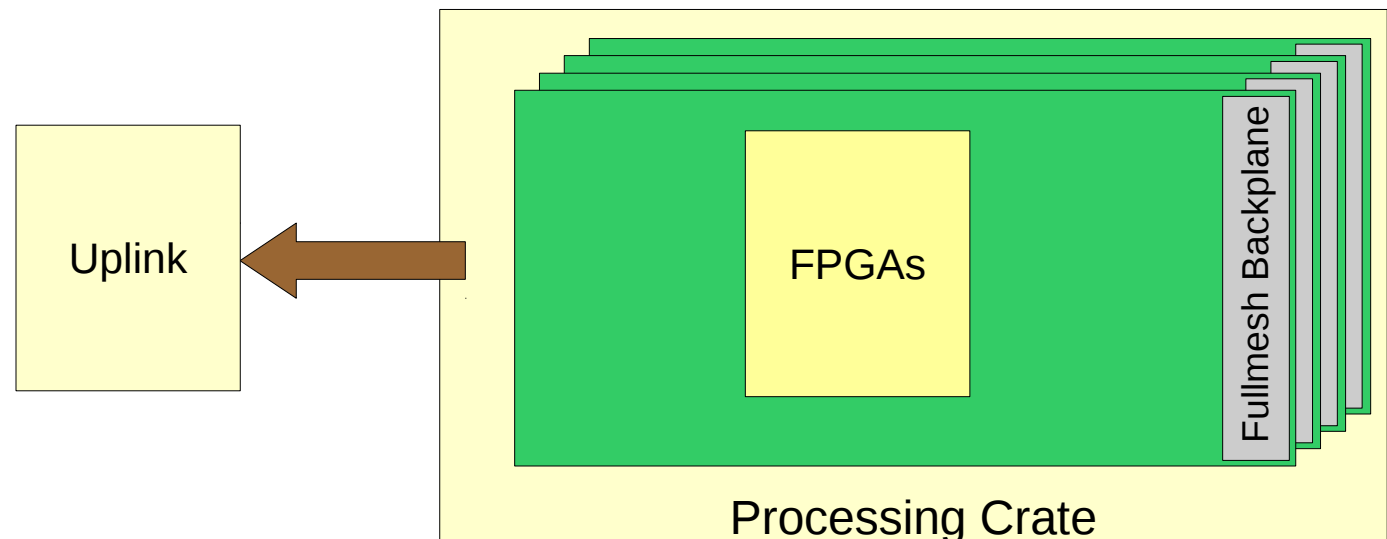


- Goal:  
200 channels on one Digitization-Module
- ADC: 8channel, serial output over 2 lanes per channel at 750 MHz  
→ 25 ADCs per board
- HV-Decoupling may be done in connector or on Digitization-Board

- System requirements:
- High number of channels should be processed on the same FPGA
- High number of FPGA should be integrated on the same FPGA-board
- Connections between FPGAs off one board
- Large FPGA-board dimensions are of choice
- Point-to-Point connections between boards are needed
- Using one of hardware standards is preferred

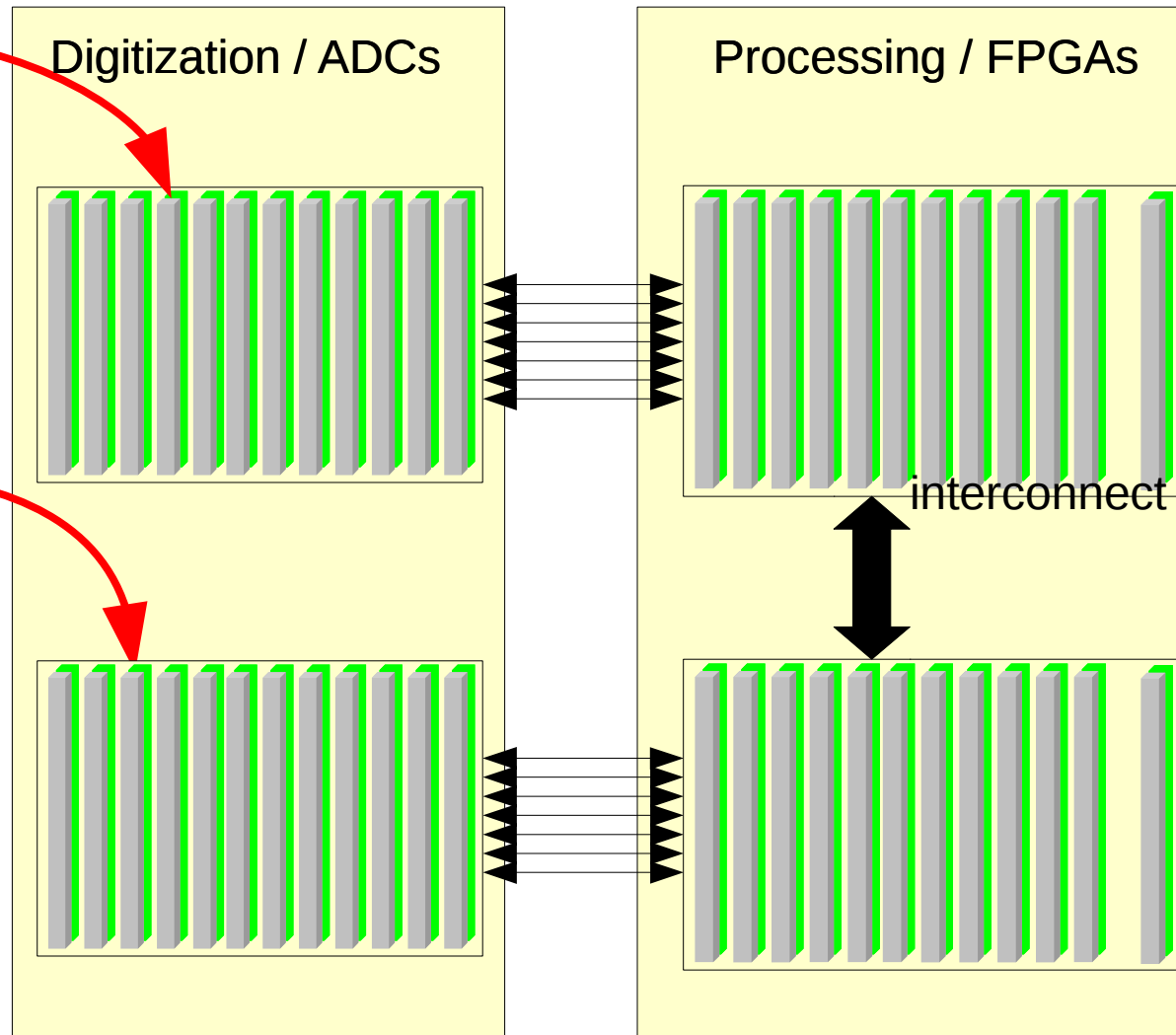
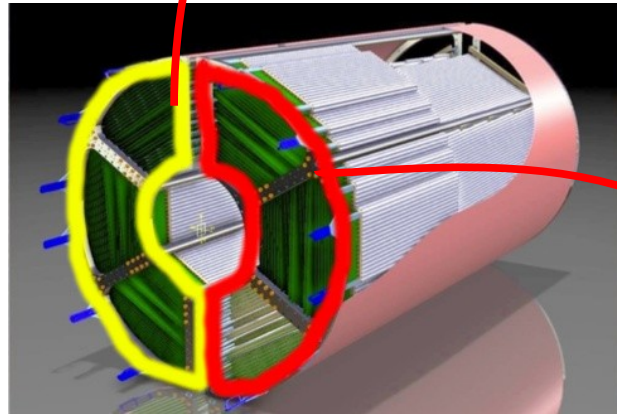


- Connection of one Digitization-Module to one Processing-Module  
→ 400 differential pairs for data stream + 125 lanes for control
- Deserializing of data stream with SERDES on Xilinx FPGA
- 200 channels, processing of 40 channels per FPGA  
→ 5 processing FPGA + 1 controlling FPGA per Board
- One communication board per crate needed

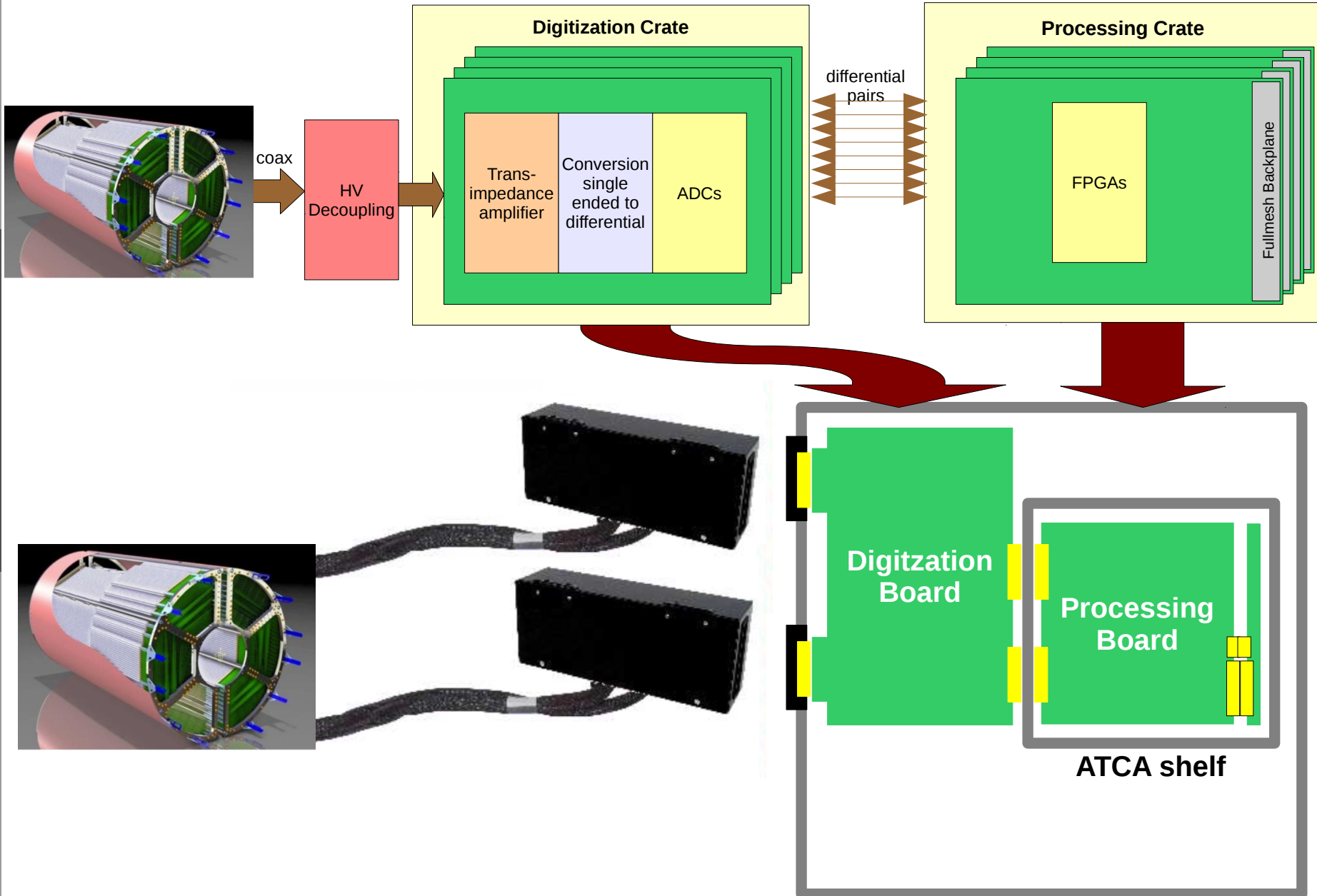


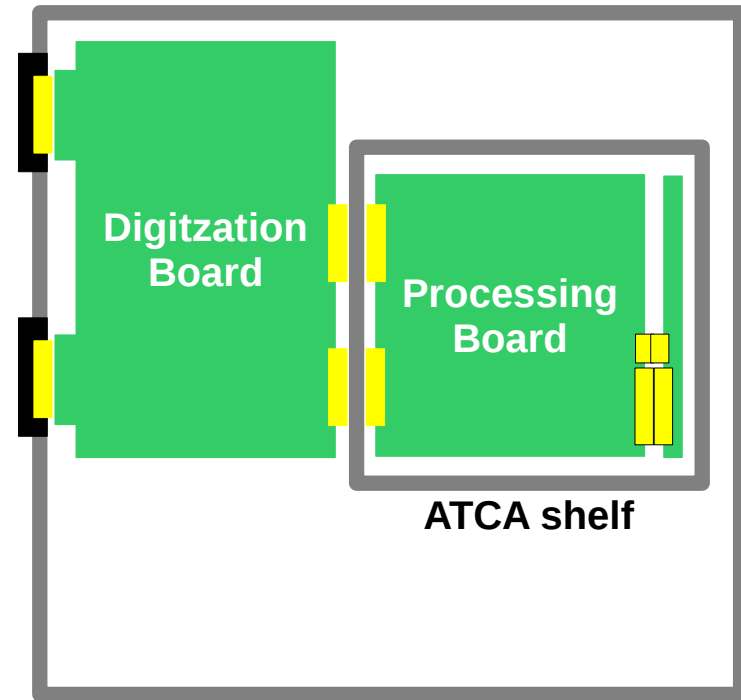
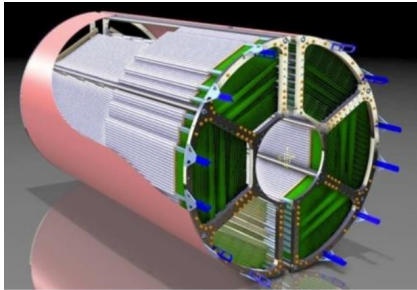
- **200 channels / board**
  - **19" ATCA crate: 14 slots**
  - **12 processing boards + 1 communication board + 1 spare**
  - **12 boards \* 200 channels = 2400 channels**
- **Need 2 sets of Digitization- and Processing-Crate for 4636 straw tubes**





# Connections and Rack design





- Connector:
  - Trade-off between modularity and high integration
    - possibility to easy assemble / disassemble groups of straw tubes (whole connector) or single straw tube (single cable at connector)
- Suitable connector under investigation with focus on:
  - HV-Decoupling
  - Shielding

- Conclusion:
  - Starting point: existing ADC-Modules
  - Development of higher integrated system
    - Division of tasks Digitization and Processing
    - Rack design to combine both units
    - Connectors with focus on integration level, HV and shielding
- Next steps
  - Tests with new ADC until next beam time in 2015
    - Data transfer, Combination with pre-amplifier
  - Concretize Rack design and choice of connector
  - Tests of algorithms with existing ADC-Module in parallel

**Thank you!**