

Status of ASIC and TRB readout

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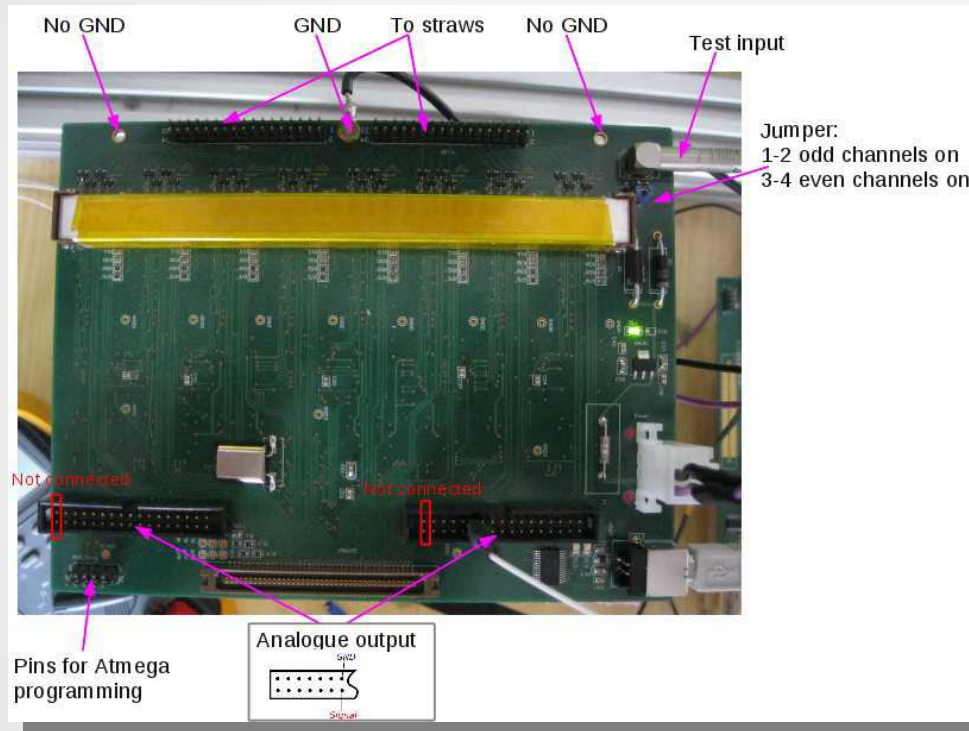


Jagiellonian University

Krakow

9 December 2014

Remainder

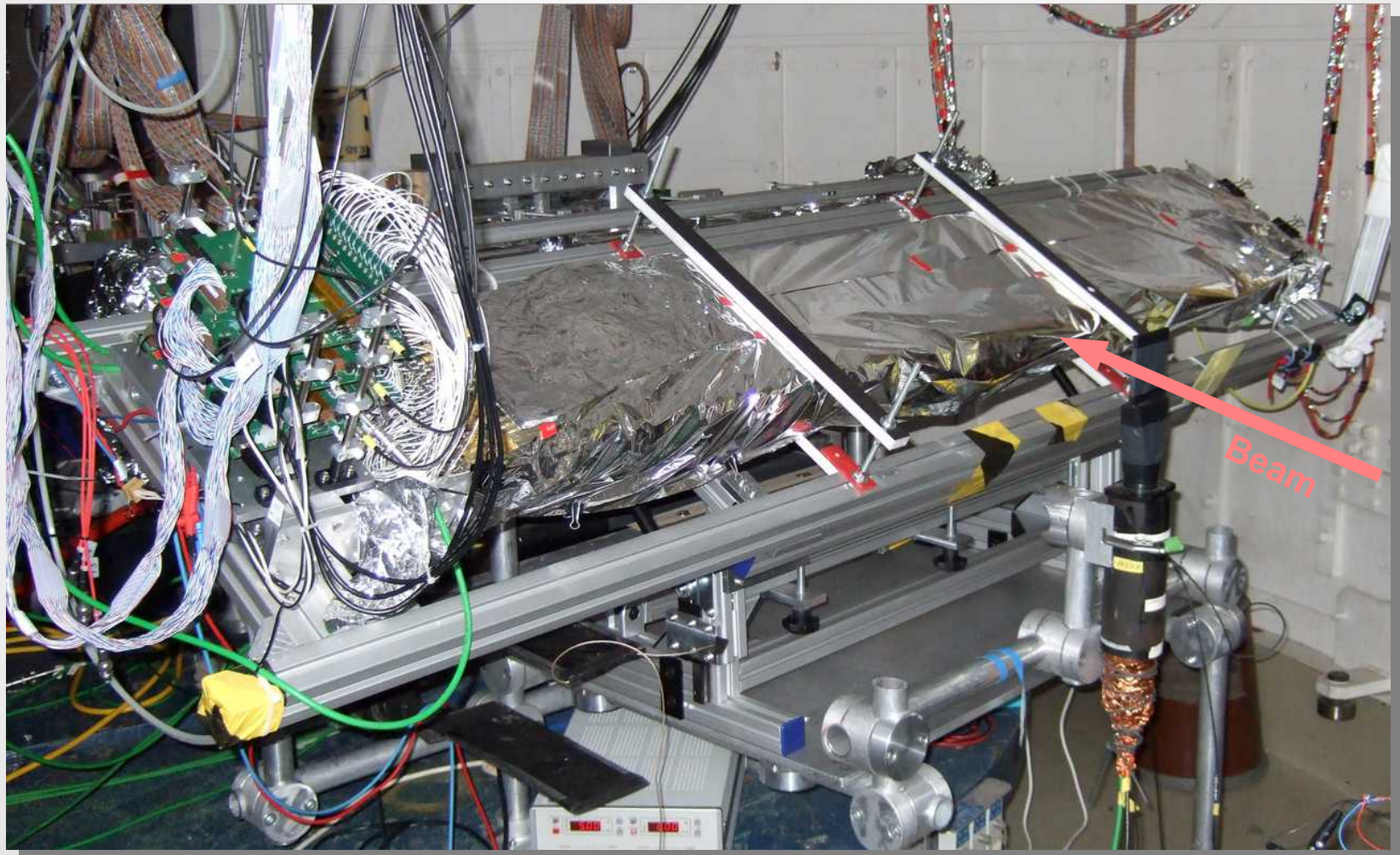


Parameter	Range/Value
Charge gain [mV/fC]	3 – 20
Peaking time (for delta) [ns]	15–40
Power consumption [mW]	≈ 16
ENC [fC]	< 0.4
1 st TC time constant [ns]	20 – 500
2 nd TC time constant [ns]	3 – 40
Input transistor parameters	
Dimensions W/L	2000μ/0.35μ
Transconductance [mS]	≈ 26
Drain current [mA]	2

Currently used chip parameters

Boards with 8 chips (32 channels)

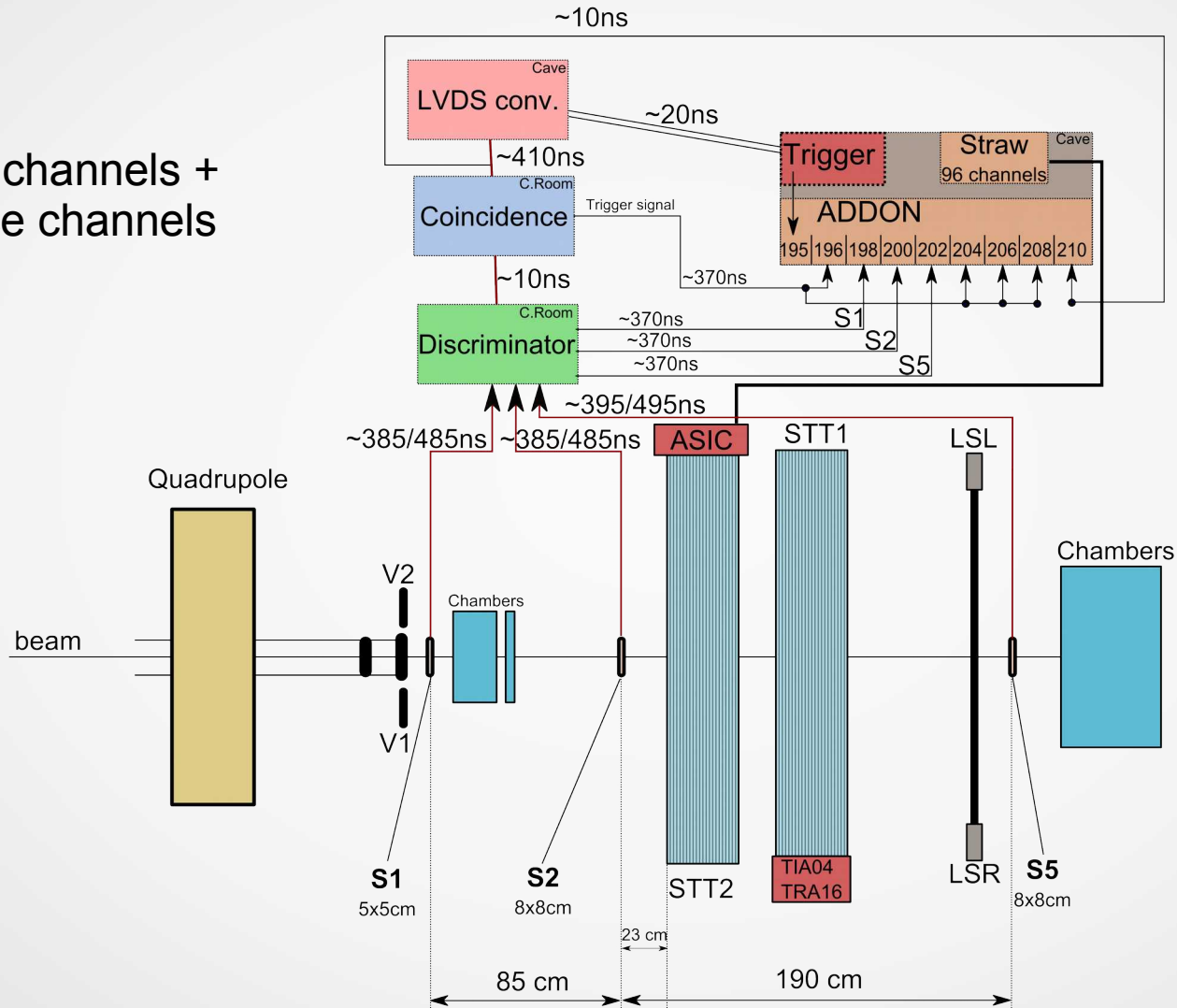
Setup at Juelich



ASIC/TRB status

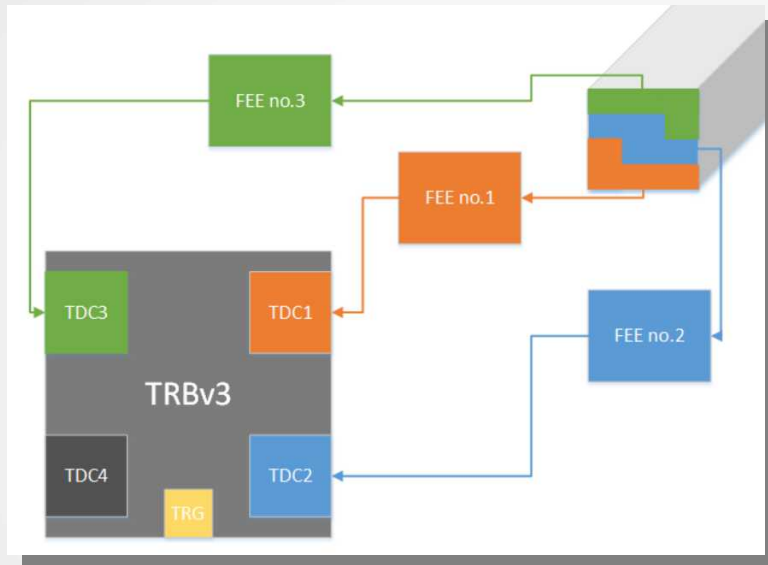
Beam set up

96 straws channels +
8 reference channels



ASIC/TRB status

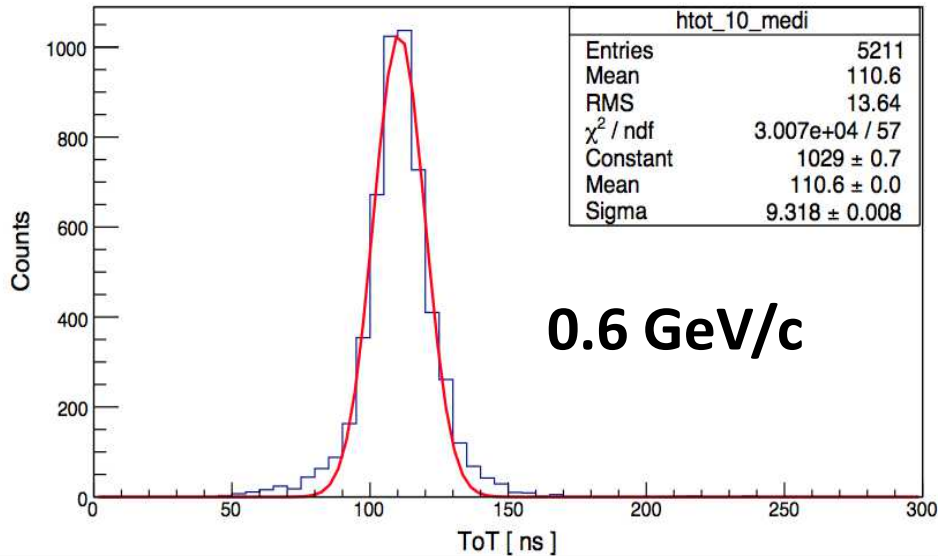
Read out



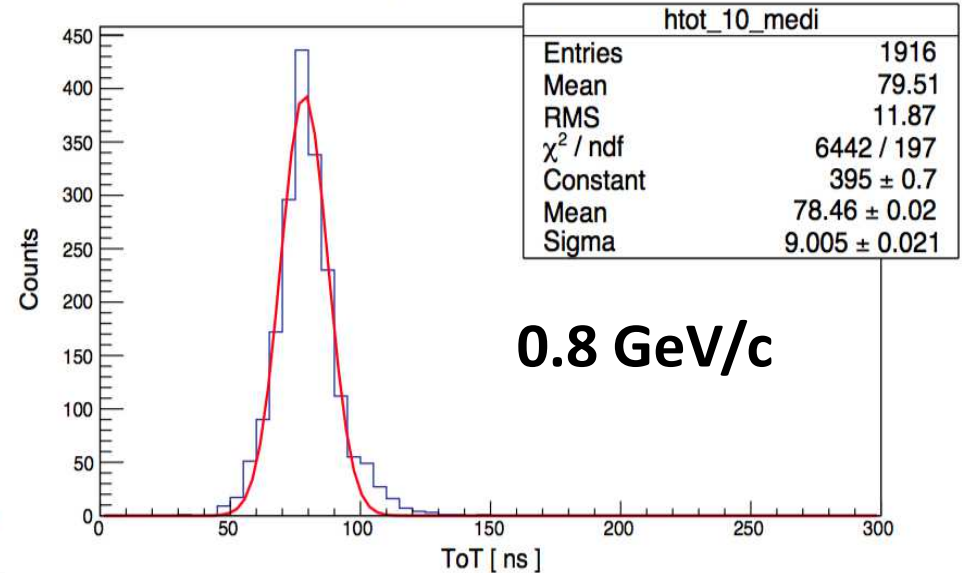
Read out is done with one TRB3. Each FEB is plugged to one TDC. Reference time (scintillators coincidence) is measured with Gpaddon.

ToT momentum scan

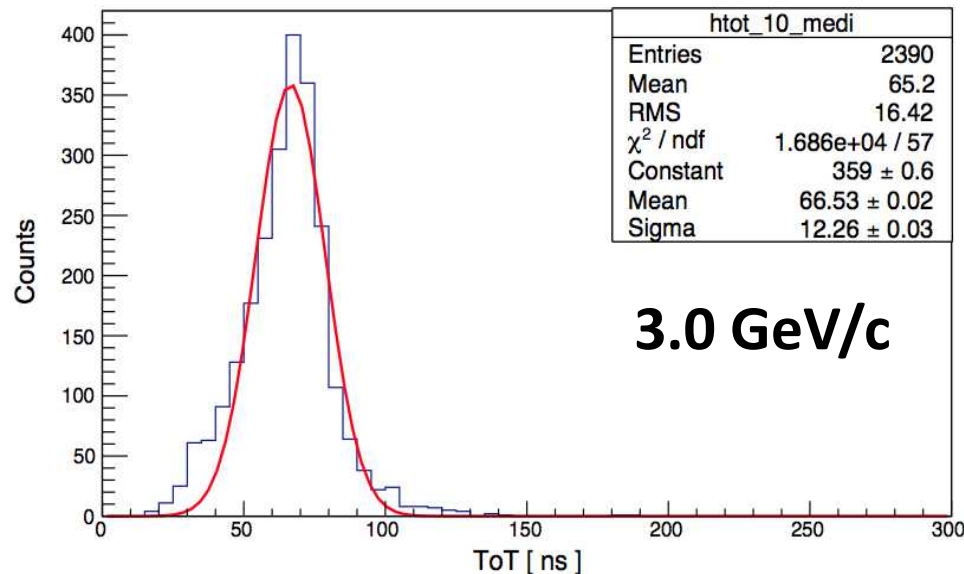
ToT for 10 straws / nt



ToT for 10 straws / nt

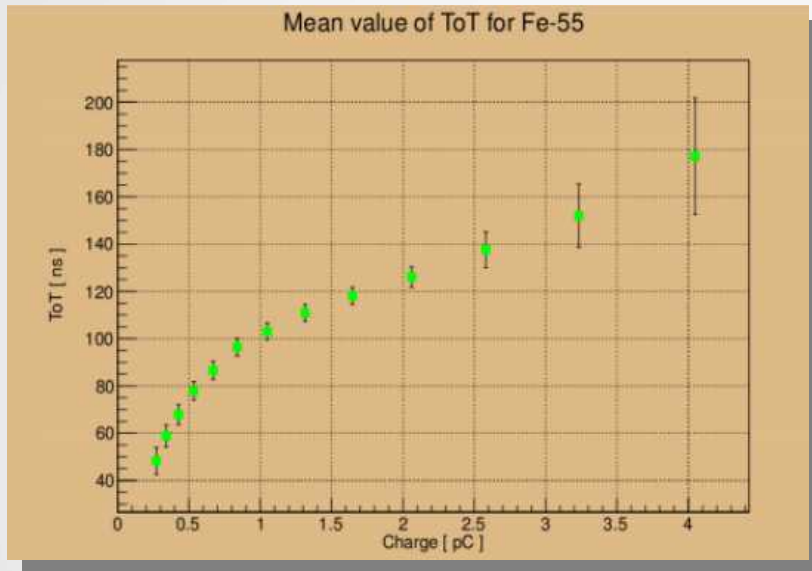


ToT for 10 straws / nt

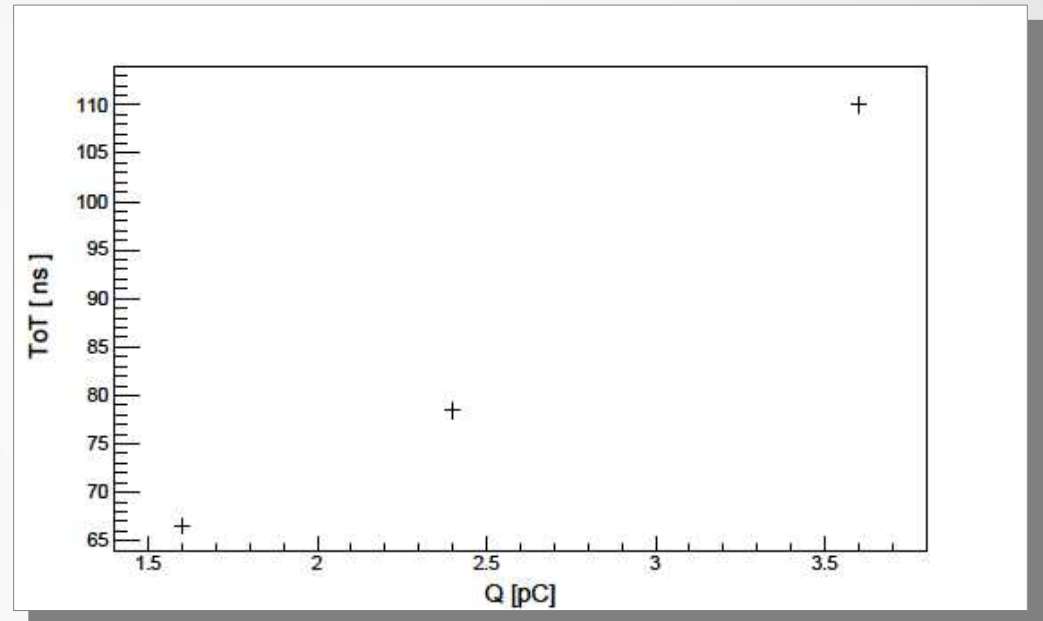


Data analysis done by
Jacek Biernat

ToT vs charge



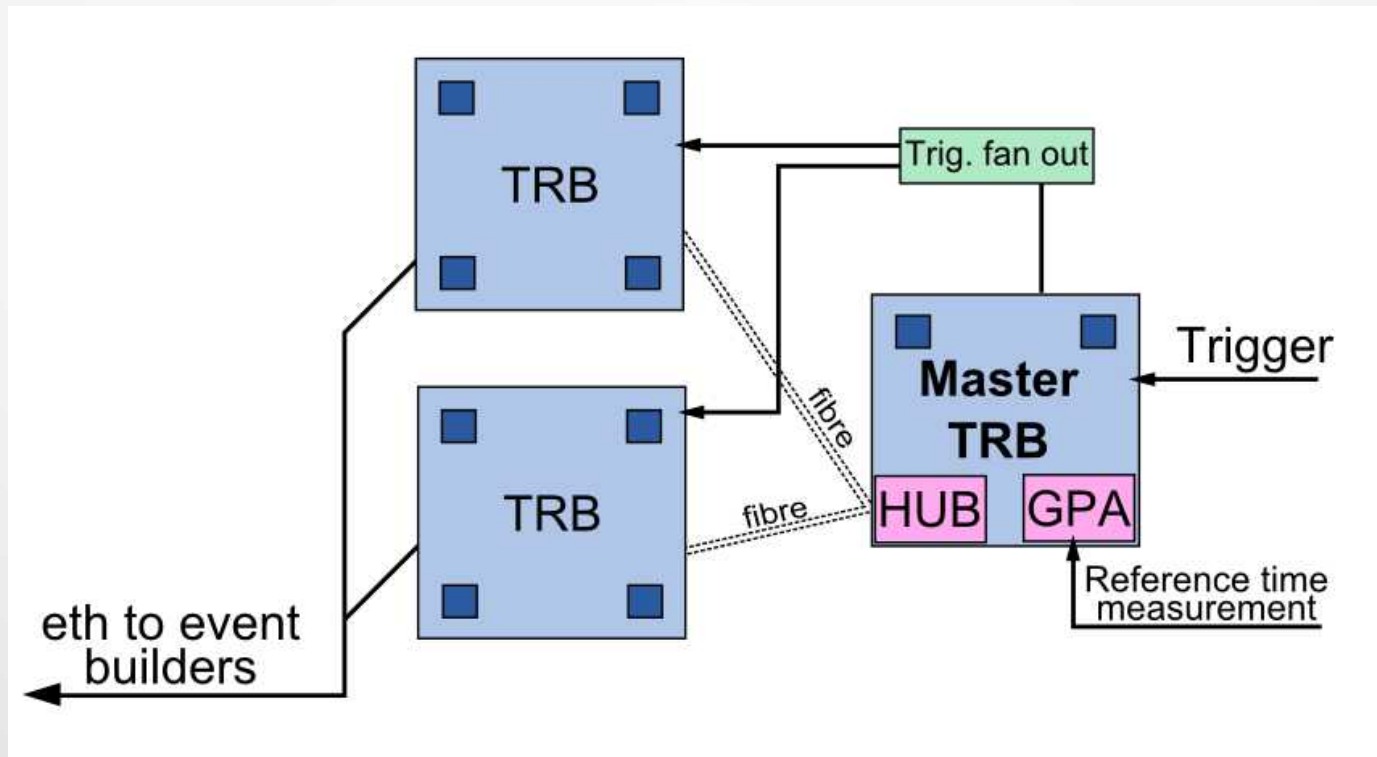
Fe-55 source



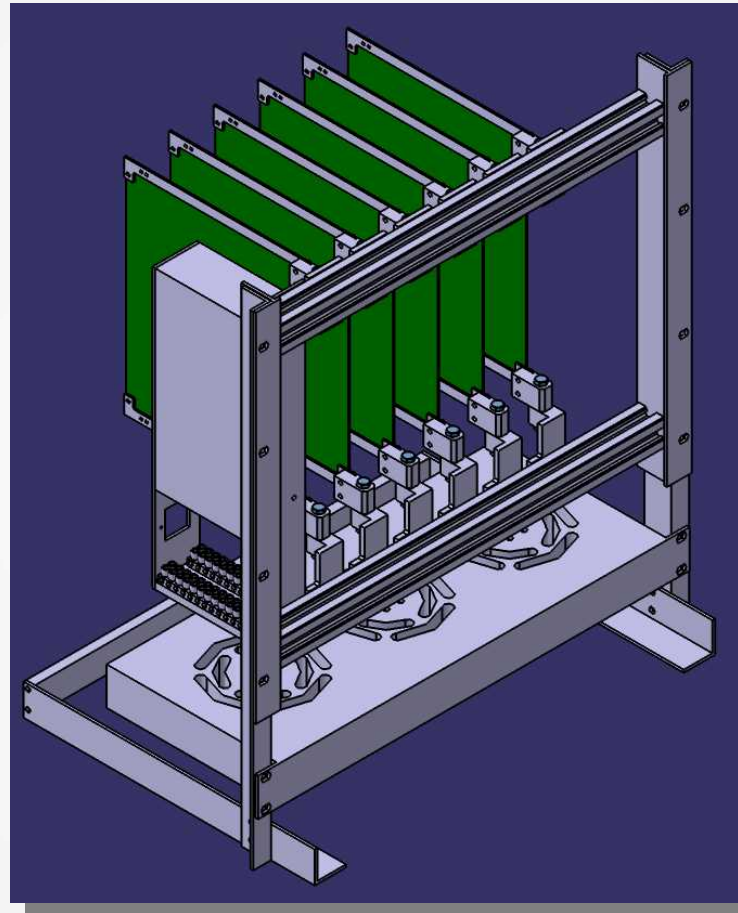
July 14 proton run

Read out upgrade

- TDC version 2.0 – 48 channels per one TDC + 1 reference signal channel, rising and falling edge detection.
- Multi TRB set-up to enable reading more than 196 channels.



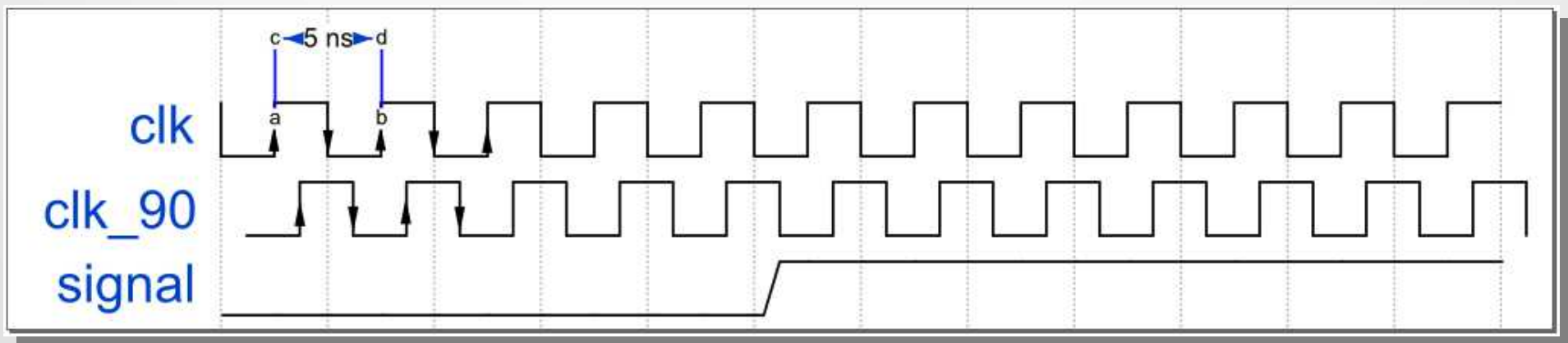
Readout upgrade



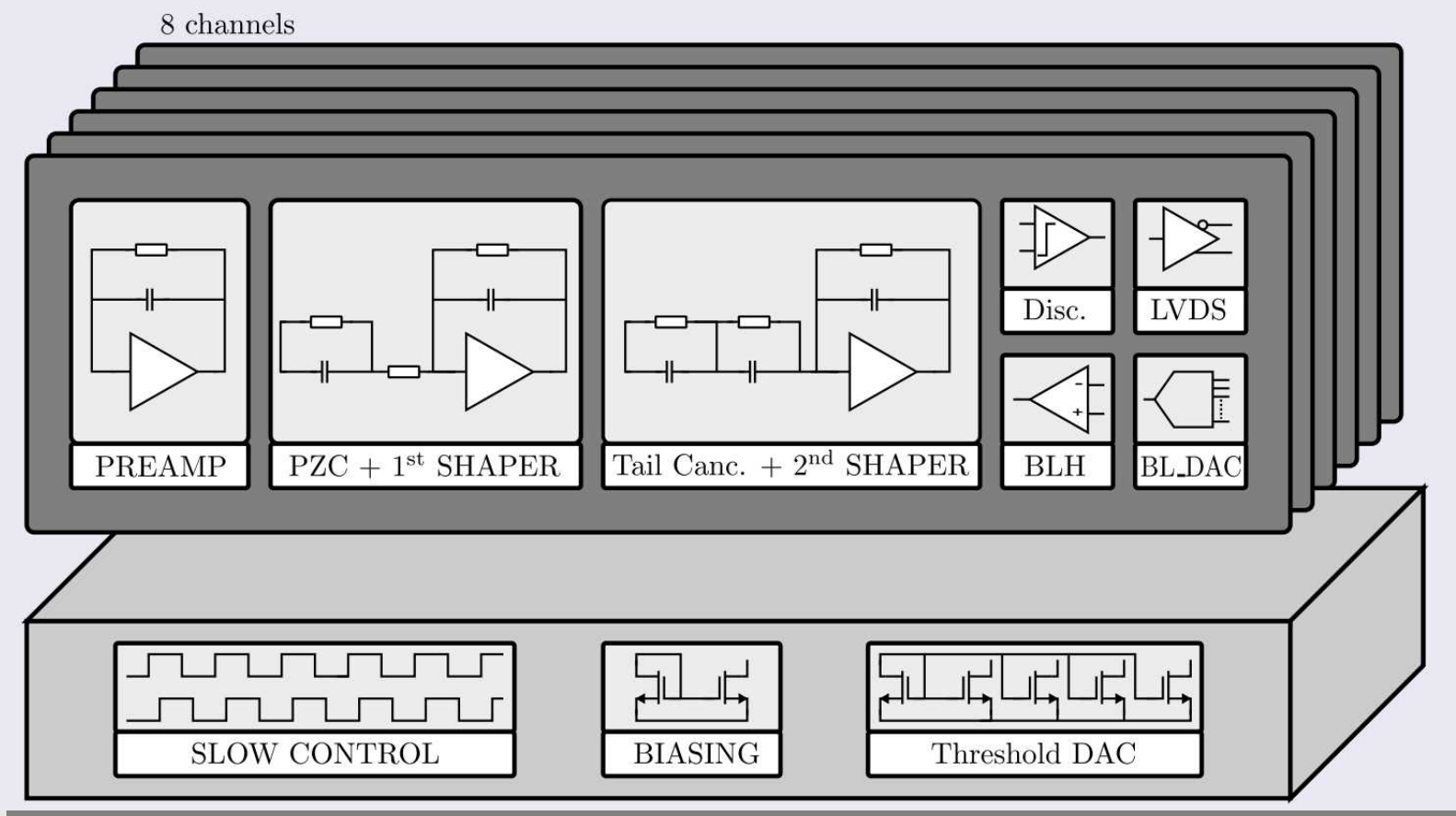
TRB crate – installable in a rack.

Low resolution TDC

- New concept of implementing TDC with resolution reaching 0.5-1ns.
- Incoming signal sampling takes place at rising and falling edge of 200 MHz clock as well as the same clock but phase shifted by 90 degree.
- Less complex logic equals higher channel density.



New ASIC – block diagram



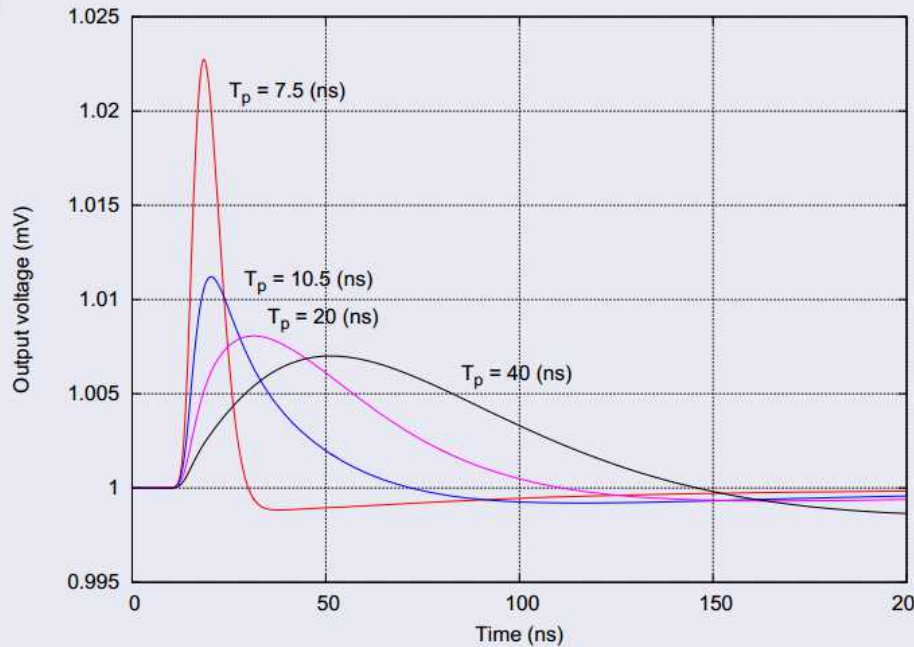
Schematic view of new ASIC. On chip has 8 channels.

New ASIC – properties

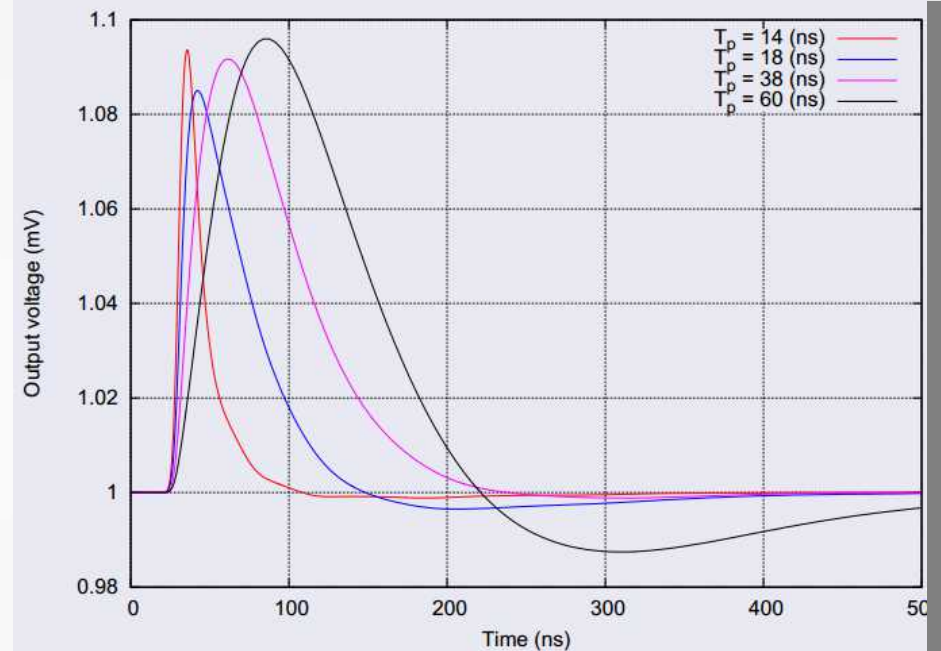
Properties and new features

- 8 channels, analog and digital (LVDS) outputs
- Variable preamp gain: 0.7; 1; 2 & 4 mV/fC
- Variable peaking time: 14, 18, 24, 38 ns – faster than previous chip
- Variable tail cancellation
- 5 bits DACs for baseline level trimming (one per channel)
- 7 bits DAC for thresholds settings (global) – till now external DAC used
- Improved baseline holder stability

ASIC simulation



Response for 1fC delta pulses

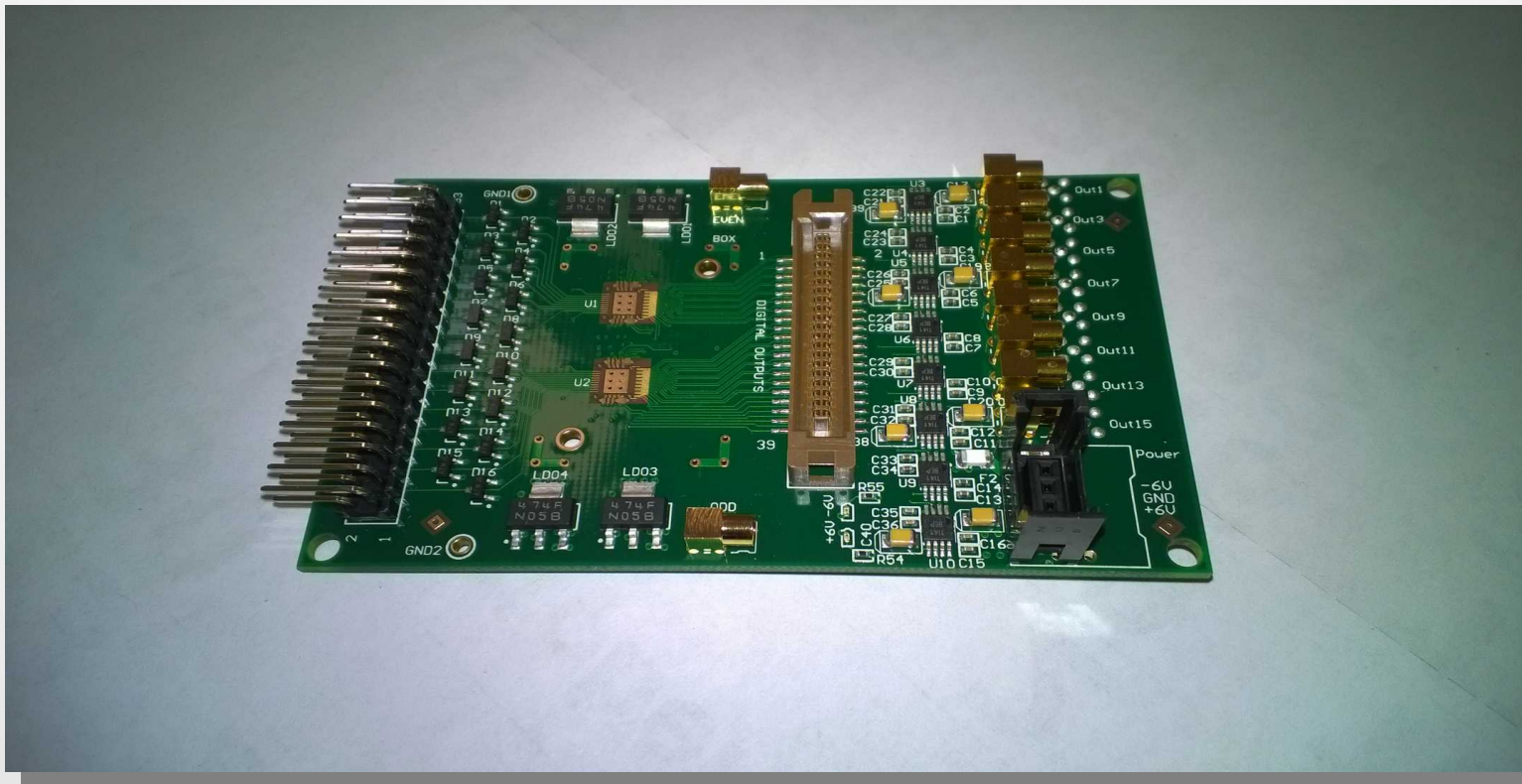


Response for pions

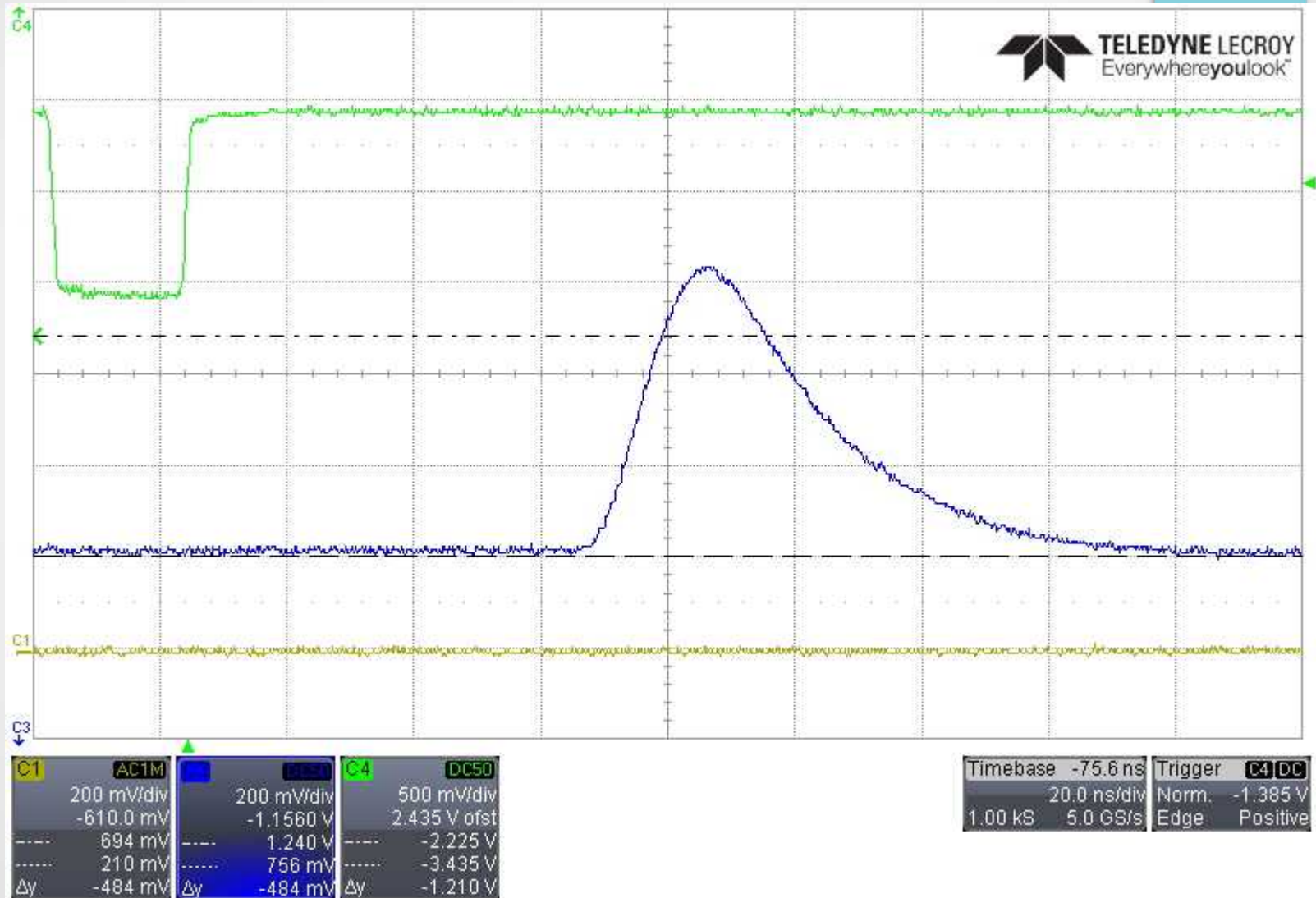
Simulations done by Dominik Przyborowski – chip author.

Current status

- FEB has been produced and initial test were done
- New firmware – slow control almost ready



Preliminary tests



ASIC/TRB status

Slow control

- Slow control integrated with TRB system.
- Possibility to change individual ASIC settings, baseline for each channel and global threshold.
- Read/write ASIC registers

The screenshot displays the 'Threshold Settings' configuration window. At the top, the 'Configuration' section shows 'Board: e002' and 'Iosc plyt: 1' with a 'create' button. Below this, the 'Plyta-1' section includes checkboxes for 'Cable conn-1' through 'Cable conn-4' and 'Asic-1' through 'Asic-2'. The main area is divided into two columns for 'Plyta-1 Cable-1 Asic-1' and 'Plyta-1 Cable-1 Asic-2'. Each column contains a table of parameters with dropdown menus for their values:

Parameter	Value
Amplification [mV/C]	4
Peaking time [ns]	35
TC1C ₂₀ [pF]	18.5
TC1R ₂₀ [kΩ]	31
TC2C ₂₀ [pF]	1.65
TC2R ₂₀ [kΩ]	28

Below the parameter tables, there are two 'Threshold (Baseline divide Baseline + 256 mV)' sections, each with a slider and a 'create' button. Underneath, there are eight 'Base line channel' rows (1-8) for each ASIC, each with a slider and a 'create' button.

Outlook

- FEB test in Krakow
- Building new set up for beam test in 2015

Thank you for your attention!

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Acknowledgments:

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