PANDA LI Collaboration Meeting

Status of ASIC and TRB readout

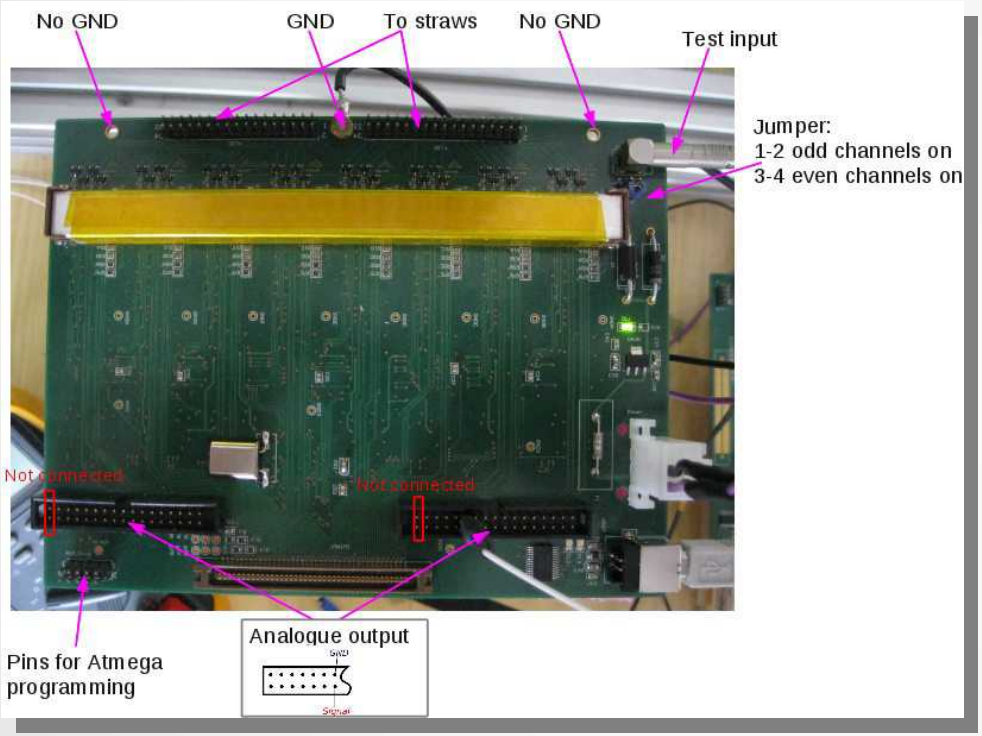
Paweł Strzempek, Grzegorz Korcyl

Jagiellonian University

Krakow

9 December 2014

Remainder

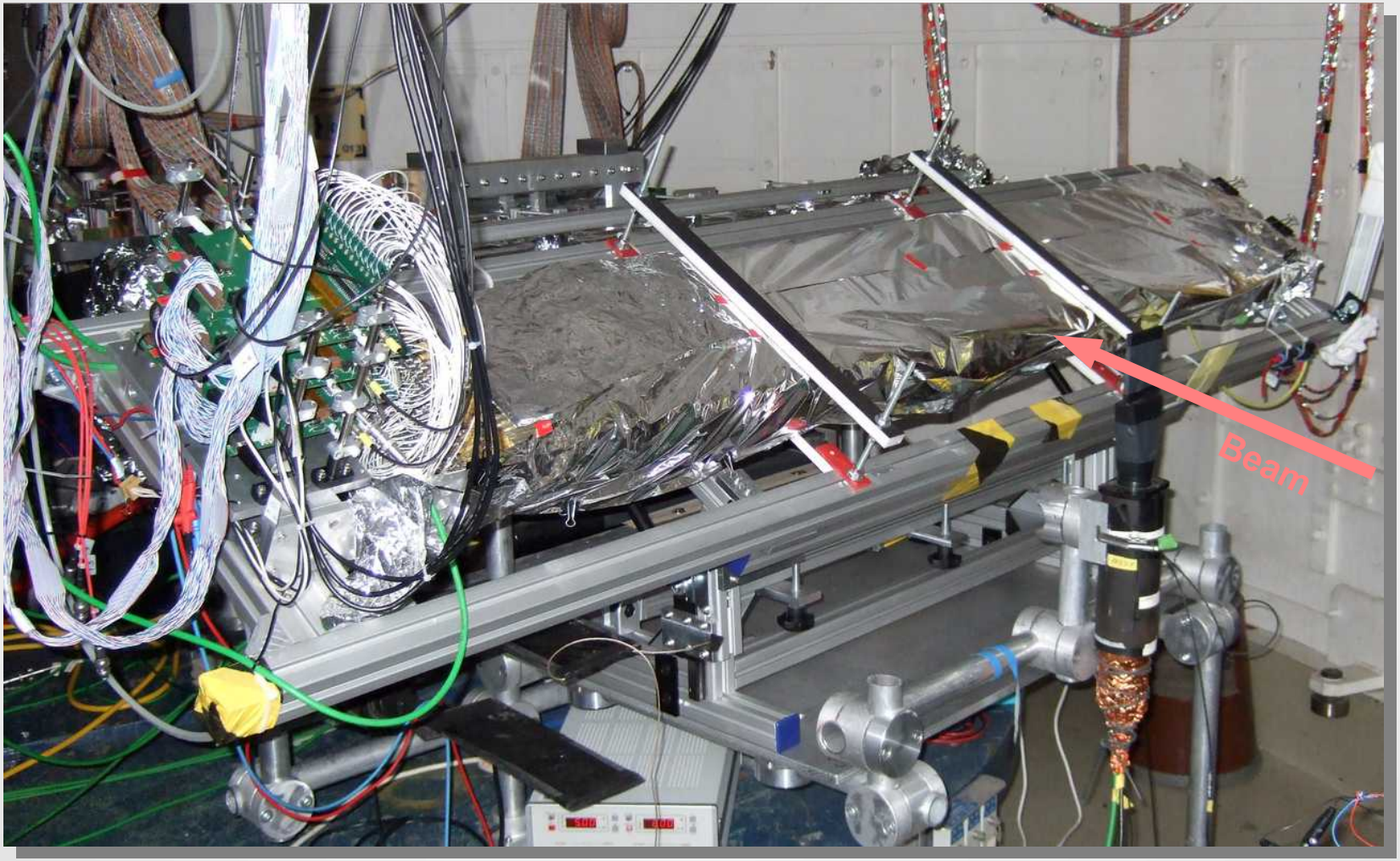


Boards with 8 chips (32 channels)

Parameter	Range/Value
Charge gain [mV/fC]	3 – 20
Peaking time (for delta) [ns]	15–40
Power consumption [mW]	$\approx$ 16
ENC [fC]	$<$ 0.4
1^{st} TC time constant [ns]	20 – 500
2^{nd} TC time constant [ns]	3 – 40
Input transistor parameters	
Dimensions W/L	$2000\mu/0.35\mu$
Transconductance [mS]	$\approx$ 26
Drain current [mA]	2

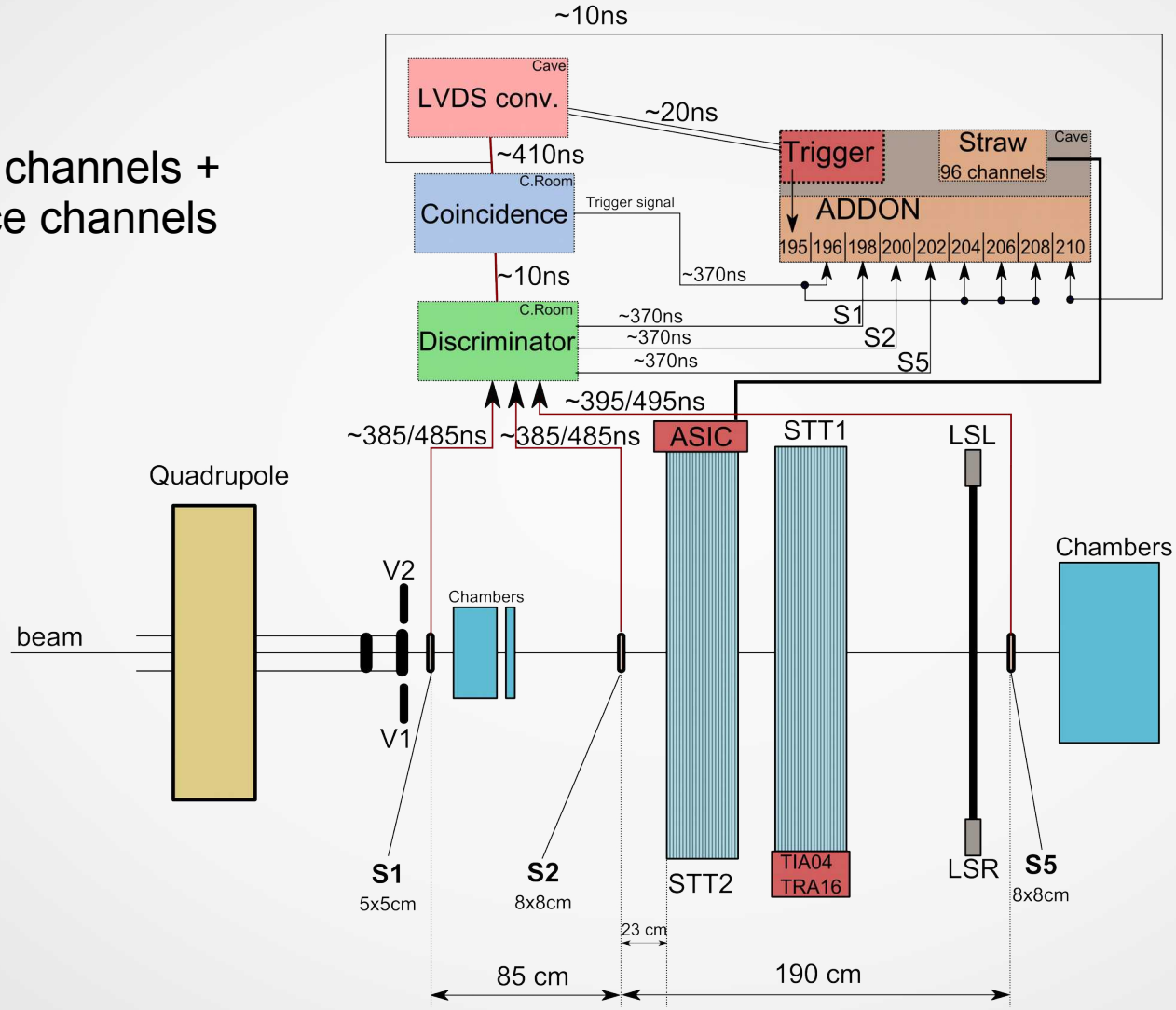
Currently used chip parameters

Setup at Juelich

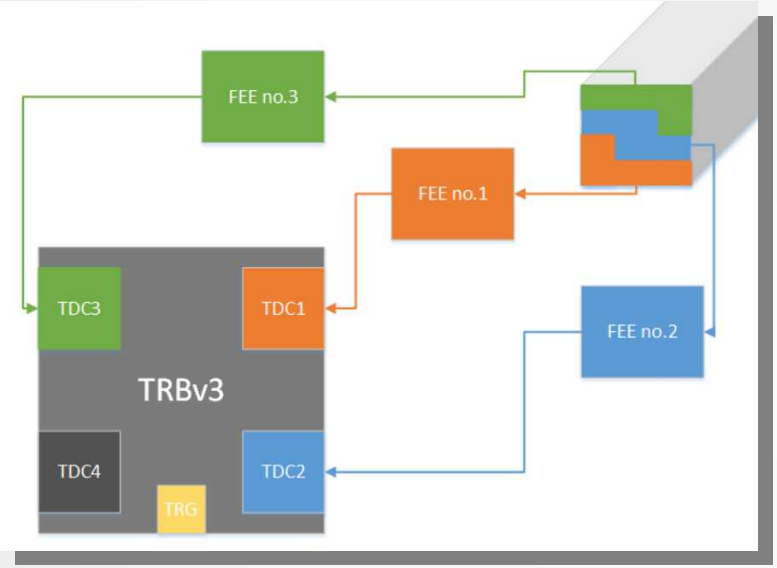


Beam set up

96 straws channels +
8 reference channels

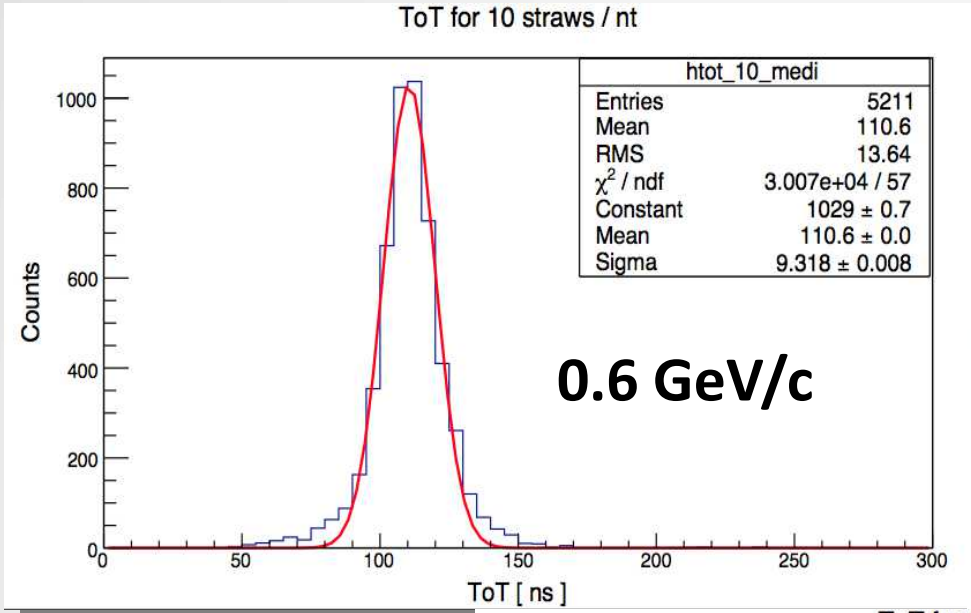


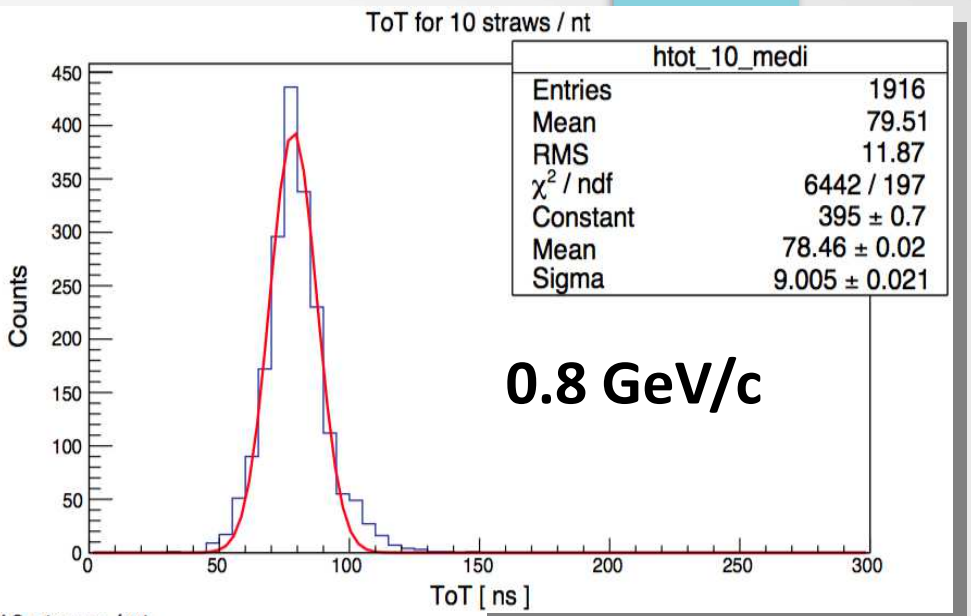
Read out

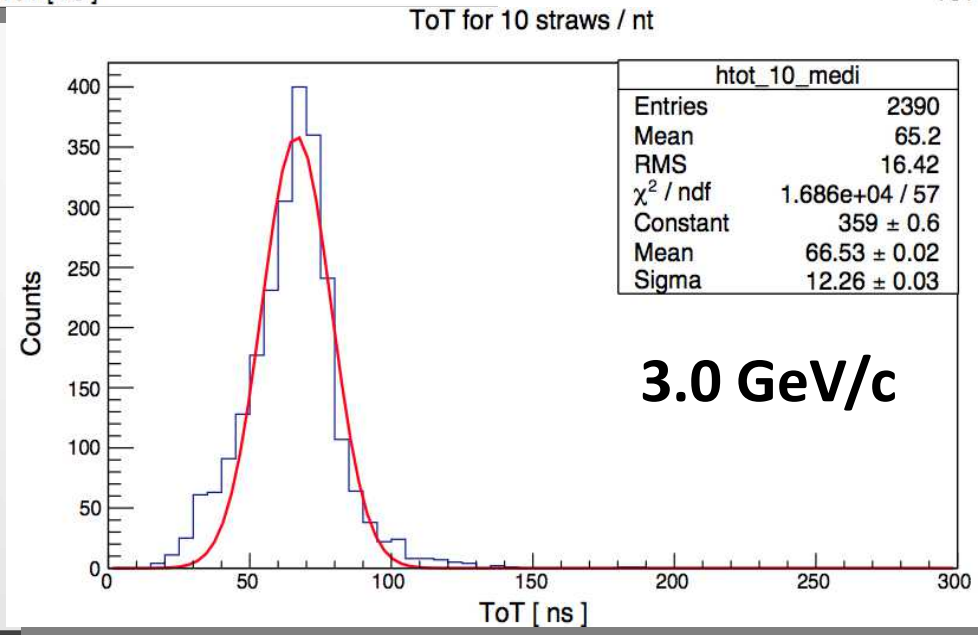


Read out is done with one TRB3. Each FEB is plugged to one TDC. Reference time (scintillators coincidence) is measured with Gpaddon.

ToT momentum scan

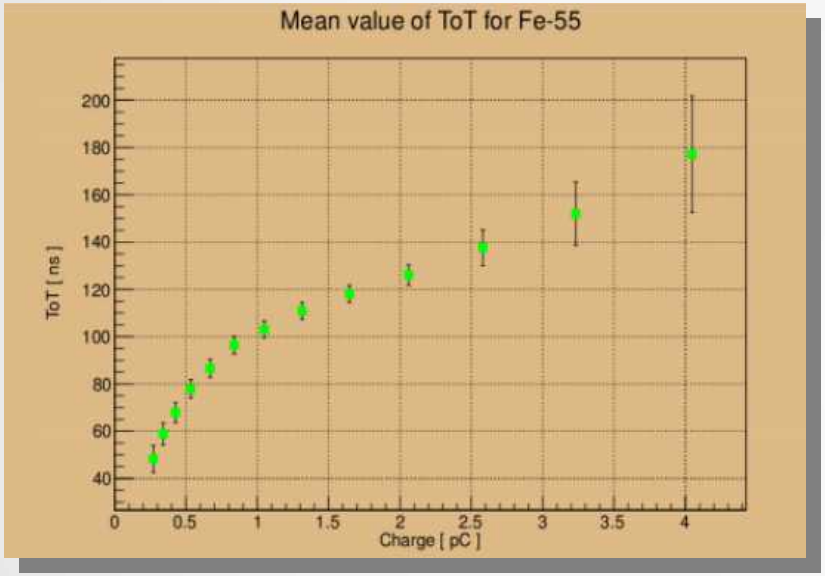




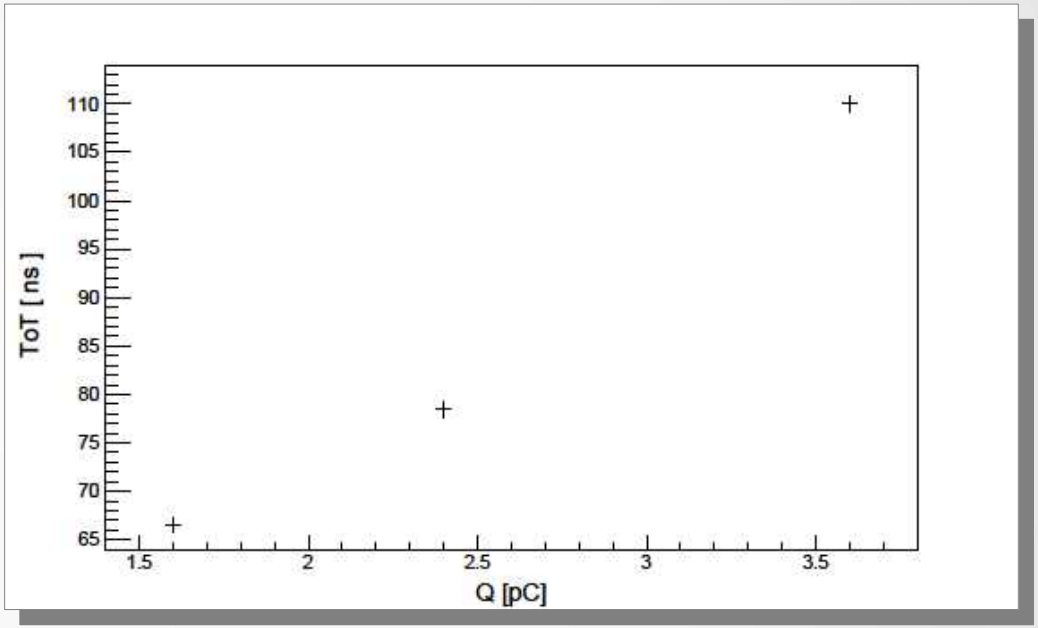


Data analysis done by Jacek Biernat

ToT vs charge



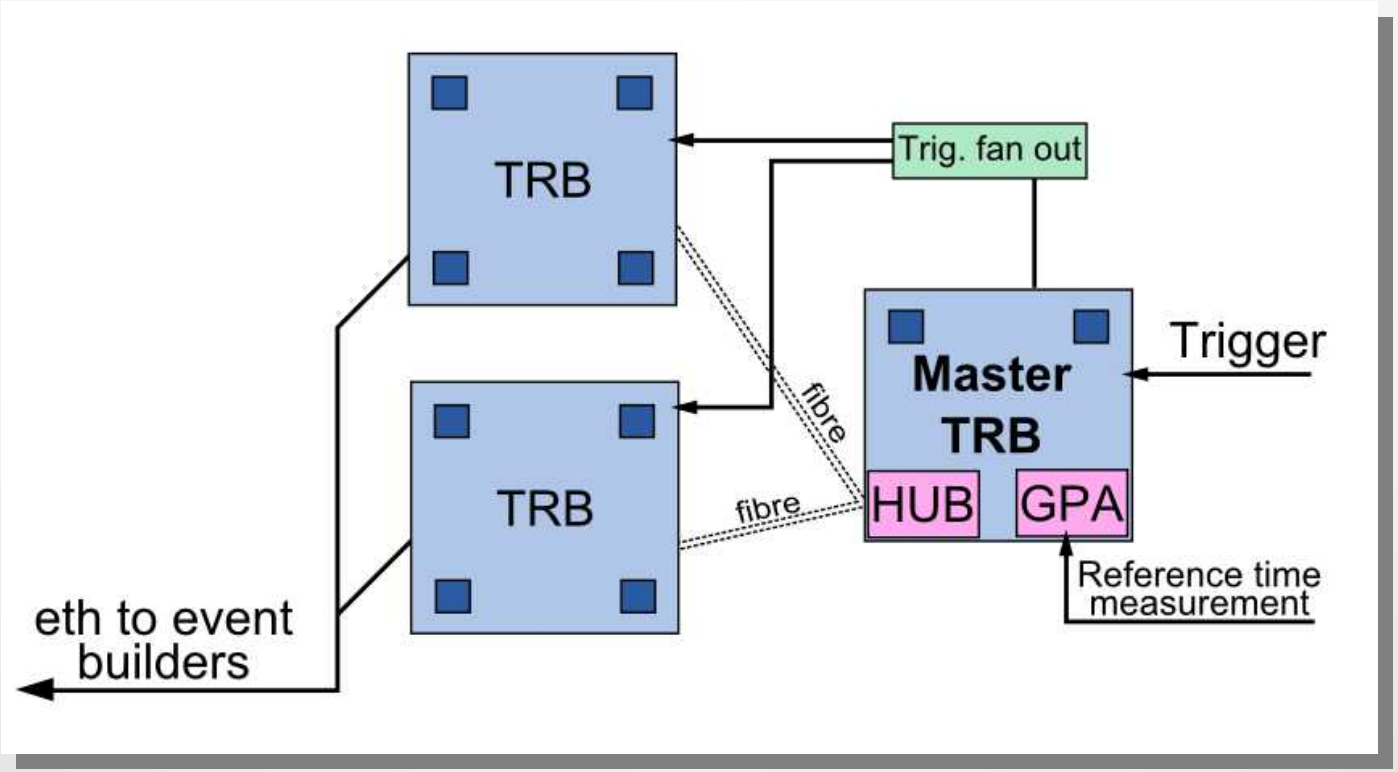
Fe-55 source



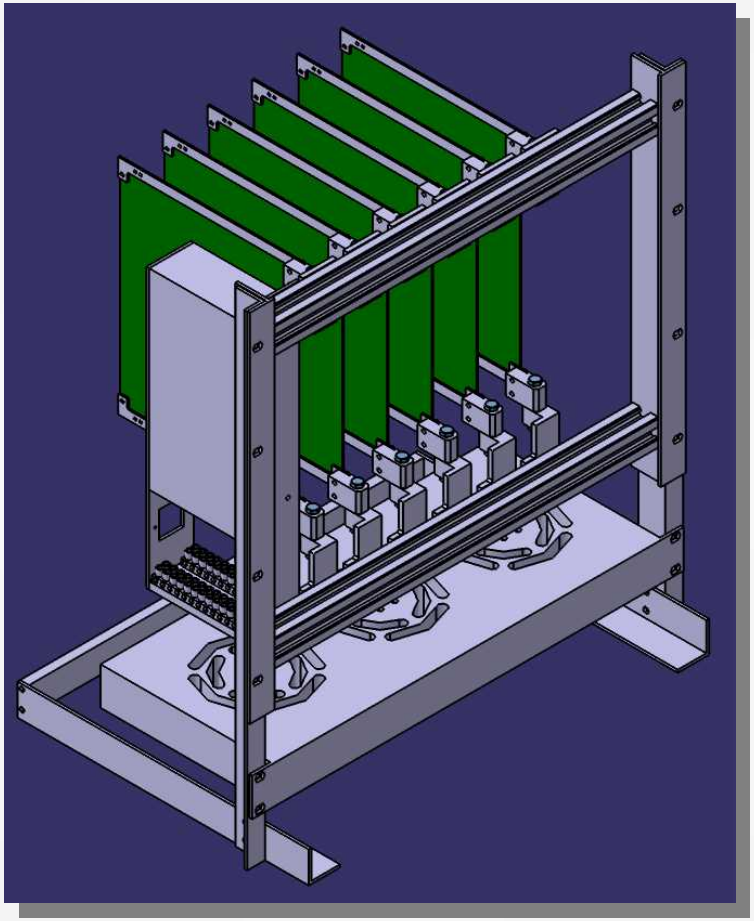
July 14 proton run

Read out upgrade

- TDC version 2.0 – 48 channels per one TDC + 1 reference signal channel, rising and falling edge detection.
- Multi TRB set-up to enable reading more than 196 channels.



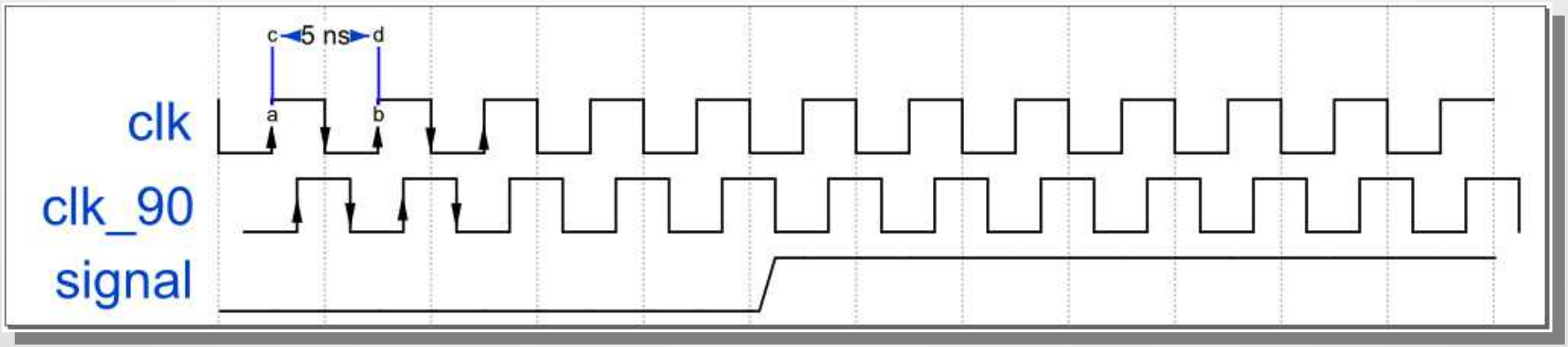
Readout upgrade



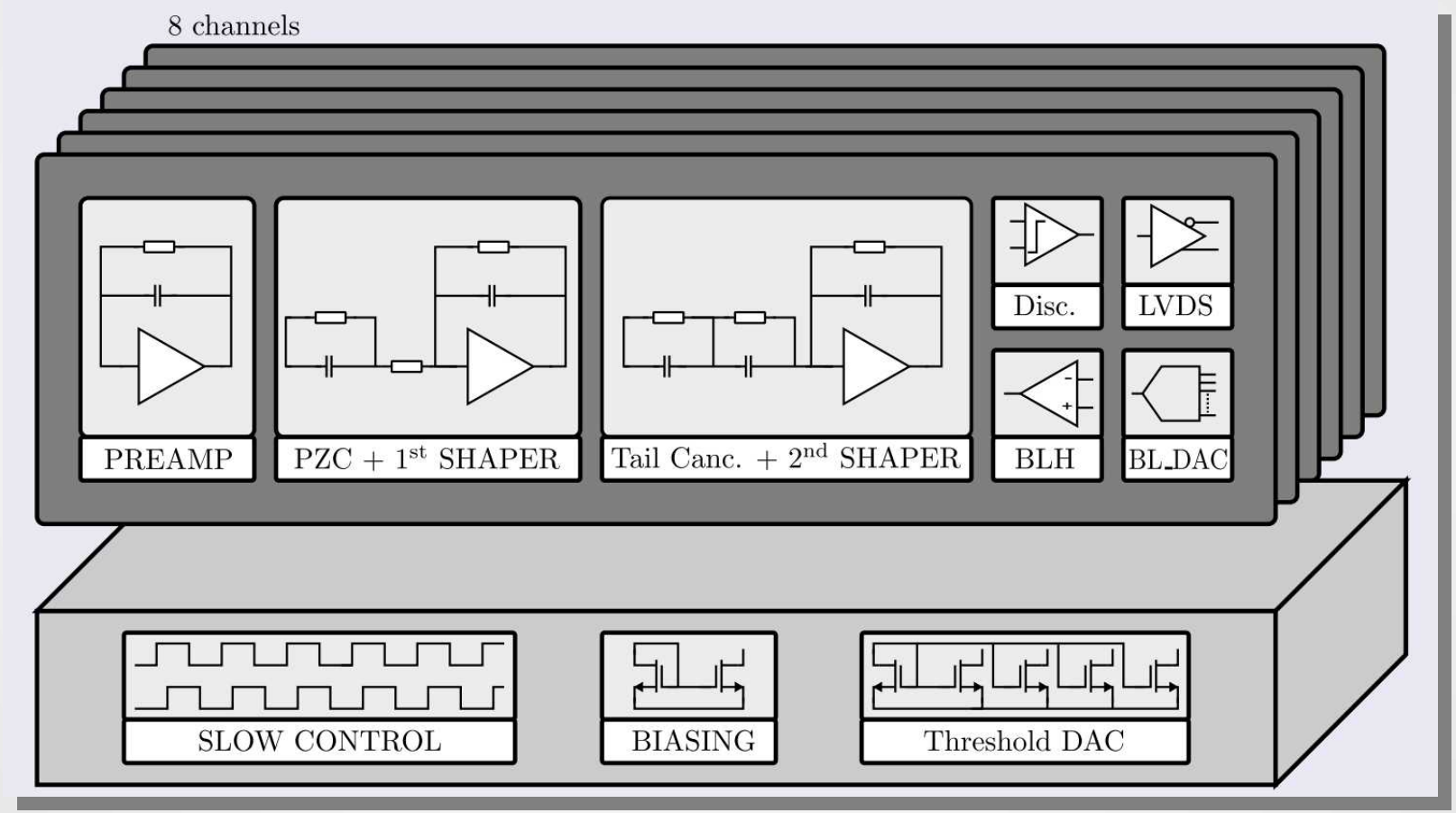
TRB crate – installable in a rack.

Low resolution TDC

- New concept of implementing TDC with resolution reaching 0.5-1ns.
- Incoming signal sampling takes place at rising and falling edge of 200 MHz clock as well as the same clock but phase shifted by 90 degree.
- Less complex logic equals higher channel density.



New ASIC – block diagram



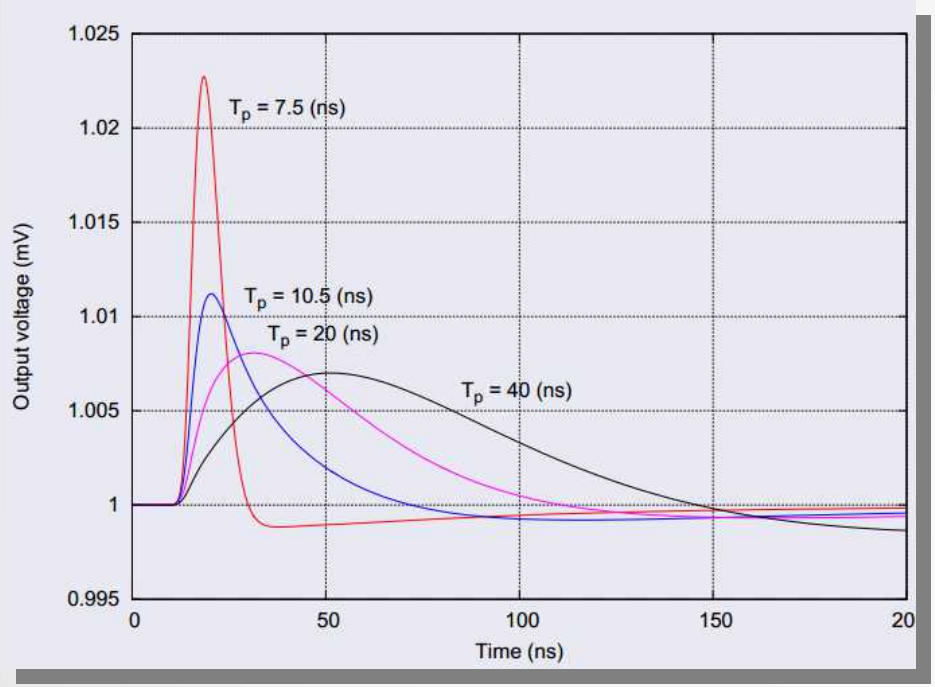
Schematic view of new ASIC. On chip has 8 channels.

New ASIC – properties

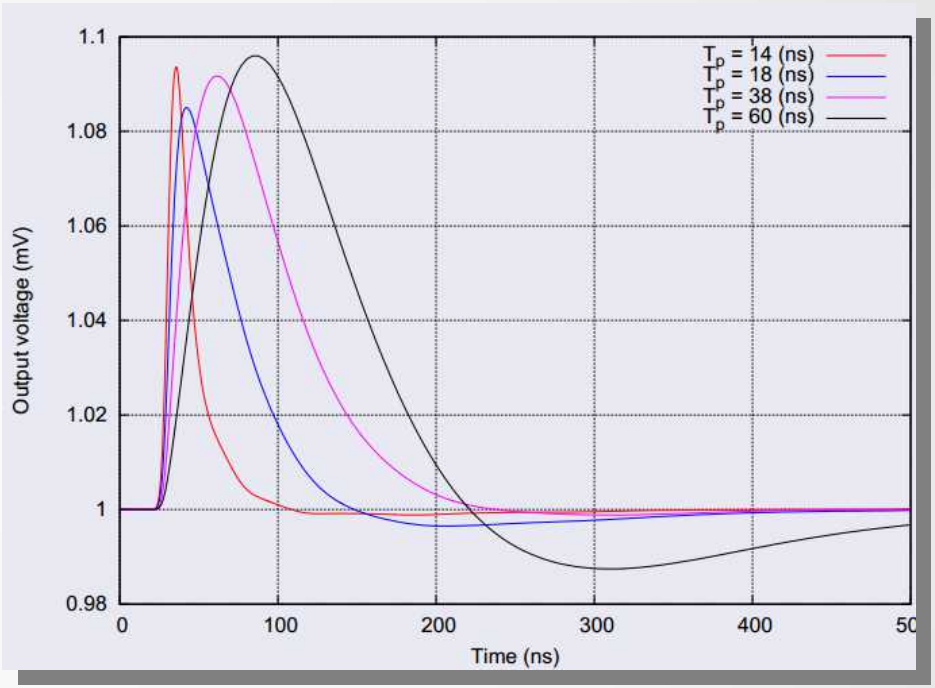
Properties and new features

- 8 channels, analog and digital (LVDS) outputs
- Variable preamp gain: 0.7; 1; 2 & 4 mV/fC
- Variable peaking time: 14, 18, 24, 38 ns – faster than previous chip
- Variable tail cancellation
- 5 bits DACs for baseline level trimming (one per channel)
- 7 bits DAC for thresholds settings (global) – till now external DAC used
- Improved baseline holder stability

ASIC simulation



Response for 1fC delta pulses

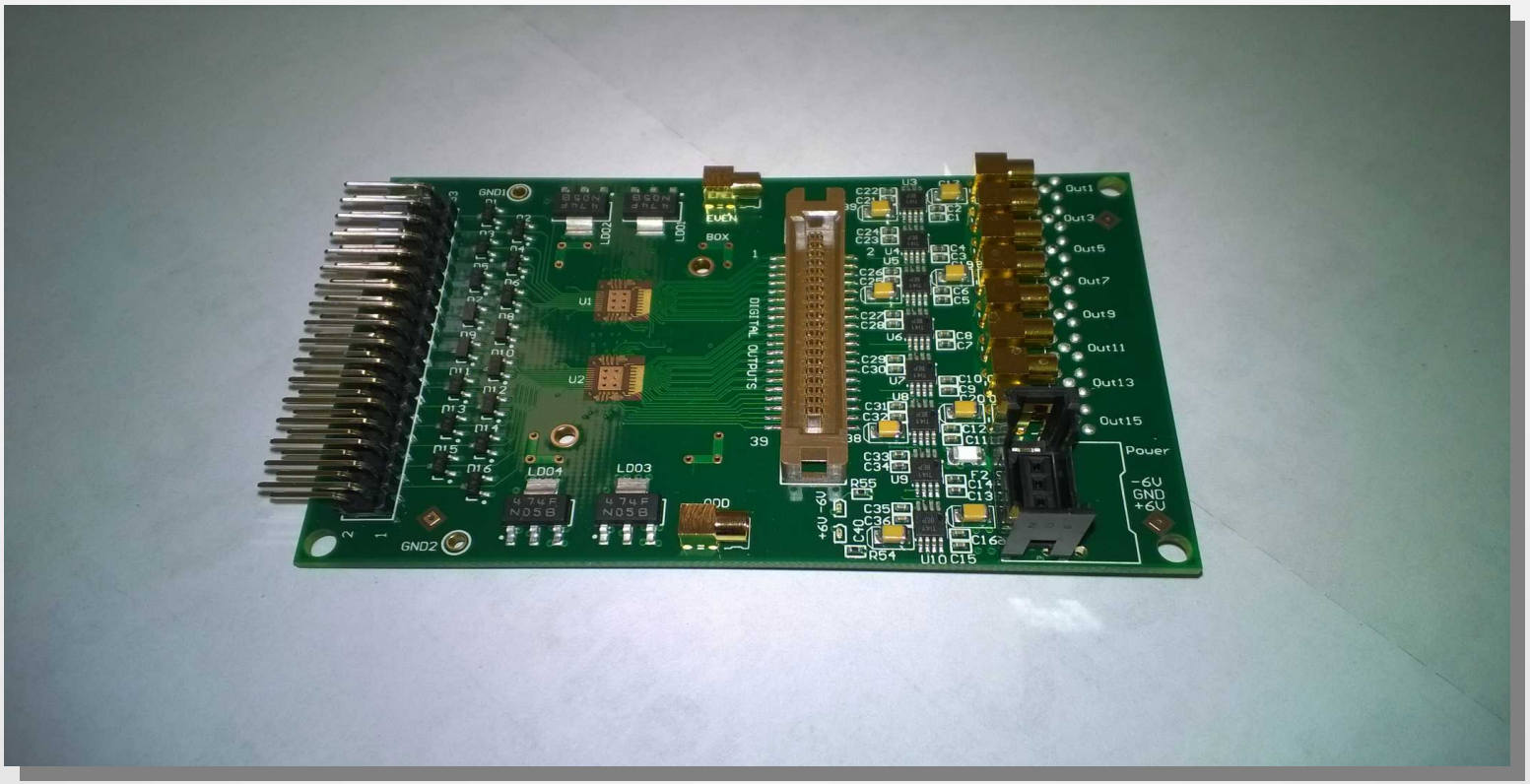


Response for pions

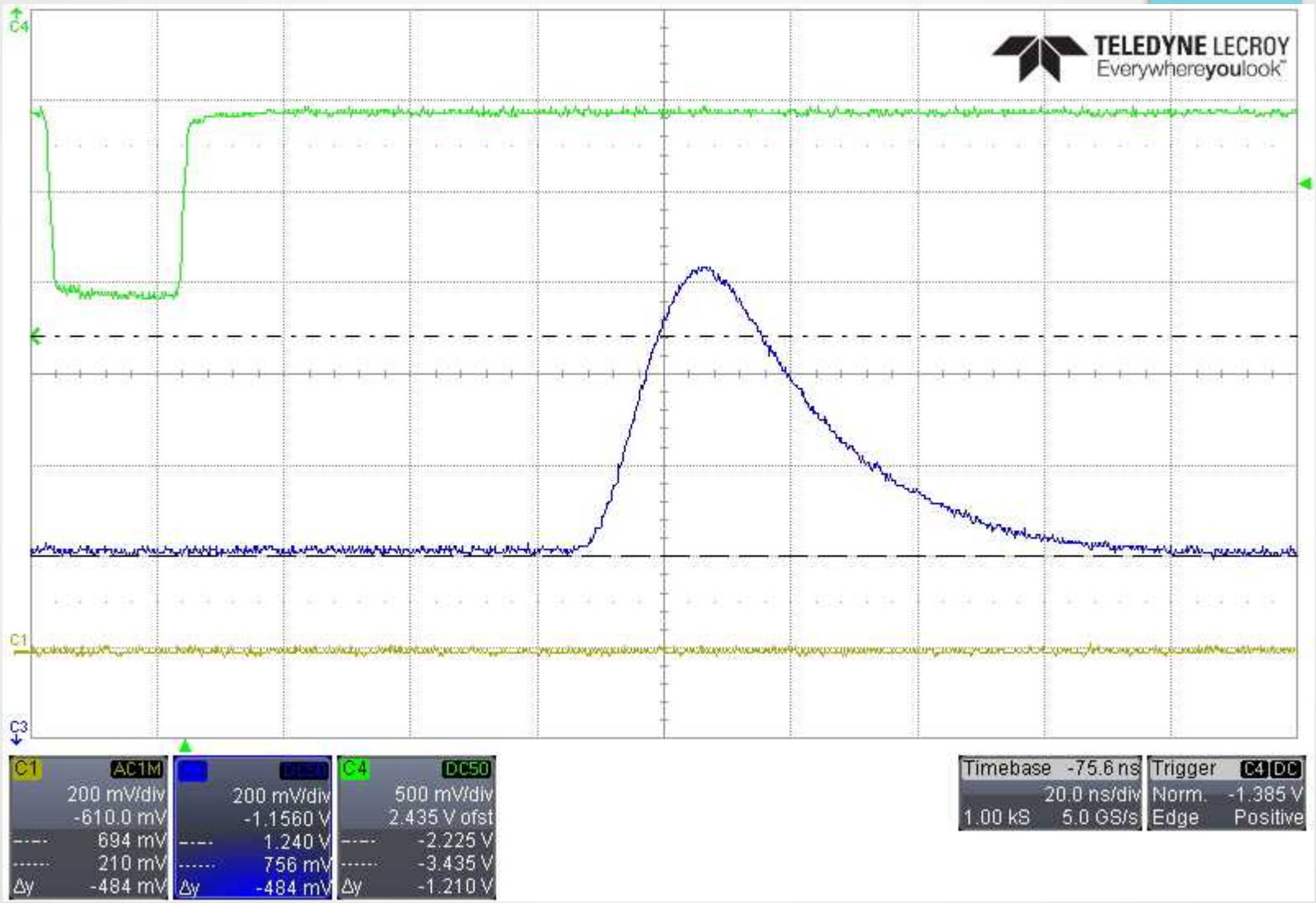
Simulations done by Dominik Przyborowski – chip author.

Current status

- FEB has been produced and initial test were done
- New firmware – slow control almost ready

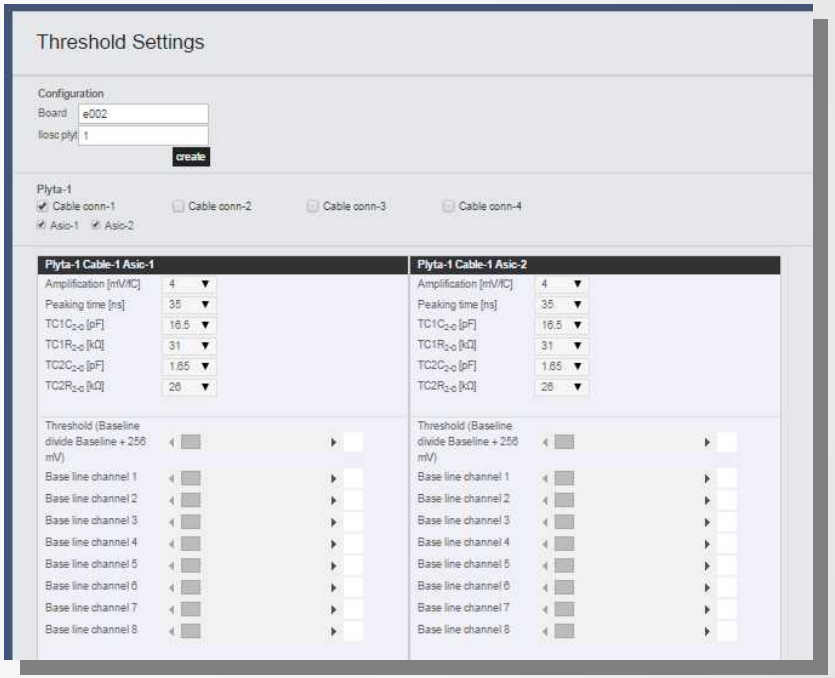


Preliminary tests



Slow control

- Slow control integrated with TRB system.
- Possibility to change individual ASIC settings, baseline for each channel and global threshold.
- Read/write ASIC registers



Outlook

- FEB test in Krakow
- Building new set up for beam test in 2015

Thank you for your attention!

pawel.strzempek@uj.edu.pl

Acknowledgments:
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