Current Status of the SODANET

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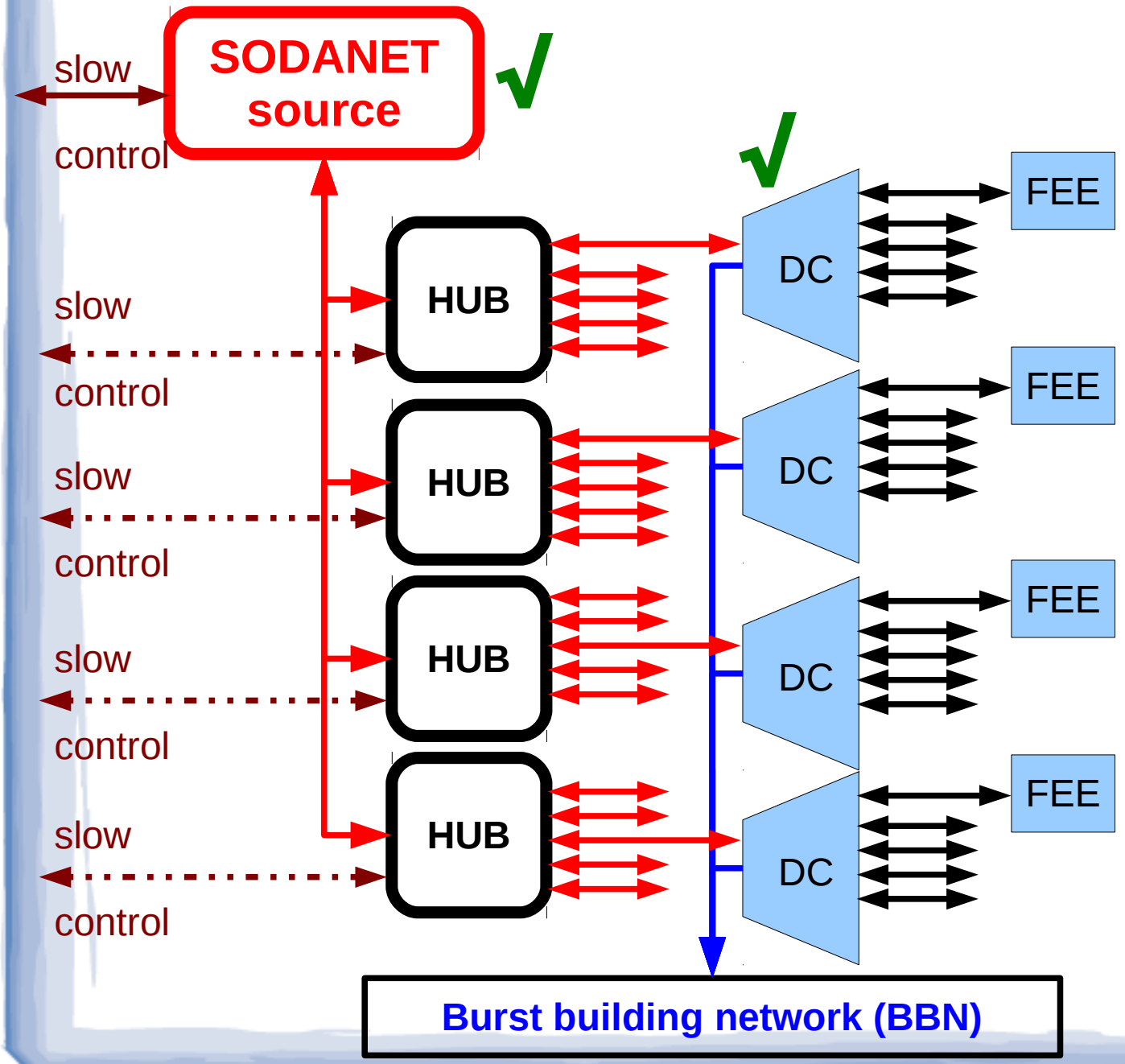
SODANET Topology



SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
  - DC → source: slow control, used for time calibration

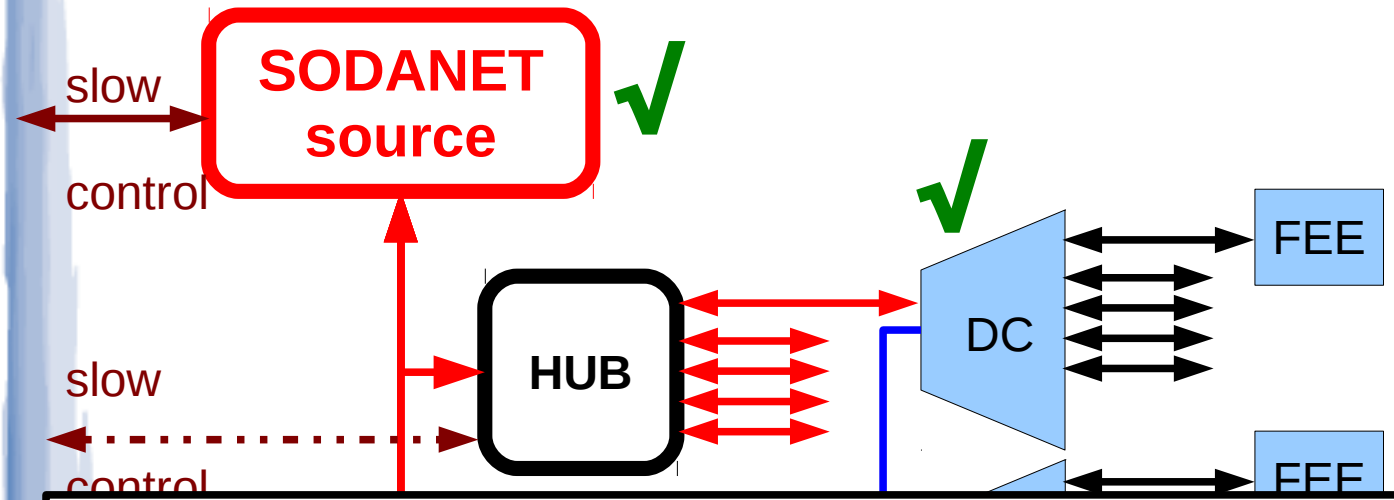
Data link (DC → BBN):

- Unidirectional

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

SODANET Topology



SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization

Done (stable operation of the hardware/firmware):
- SODANET source
- SODANET endpoint (DC)

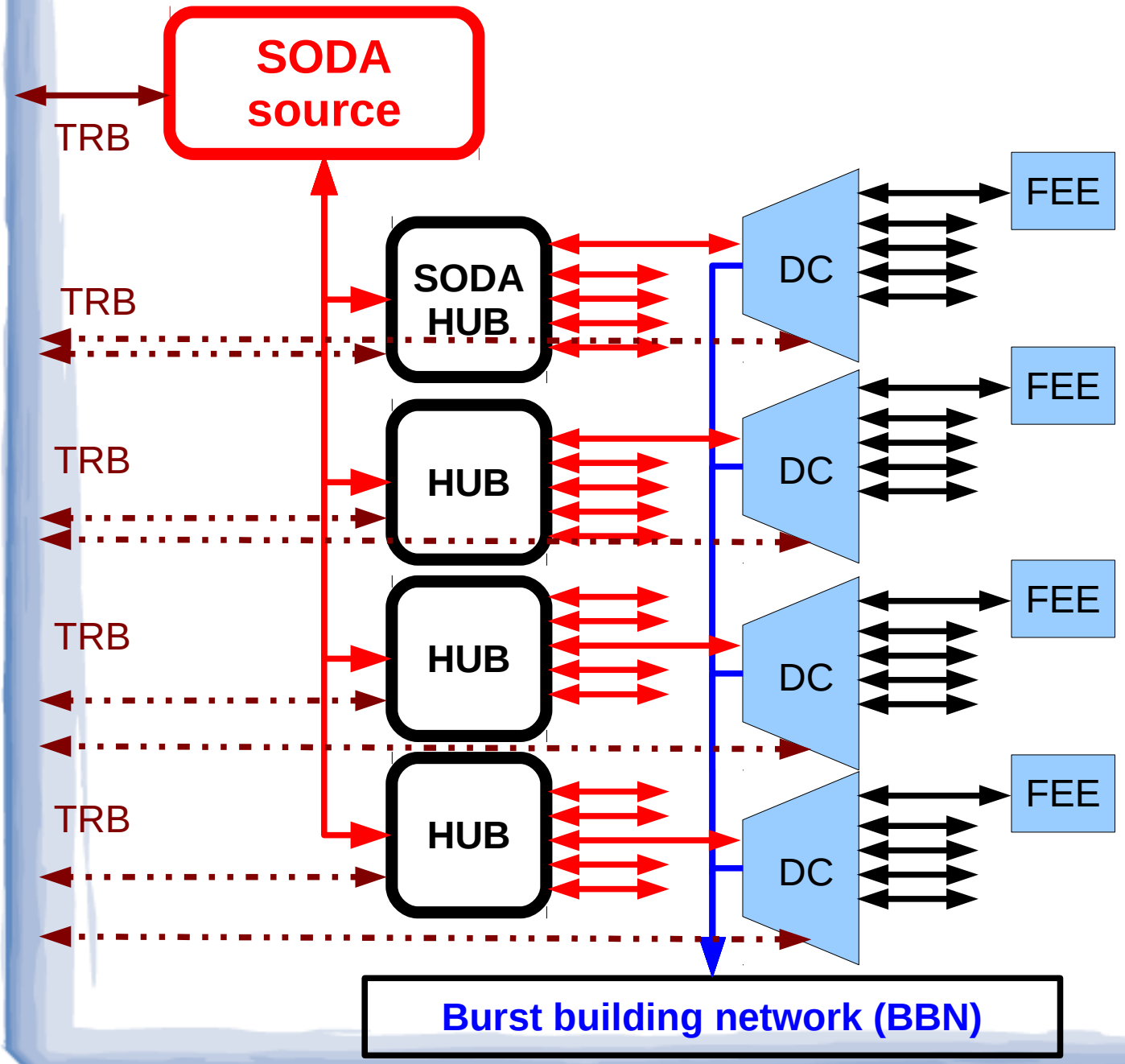
Does not work:
- SODANET HUB (required for multiple endpoints):
  - SODA commands go through the HUB while the TRB hub is hanging

→ **This issue is being investigated by the TRB expert (Jan Michel)**

- Protocol up to subsystem

Burst building network (BBN)

Step I
Each SODA instance is TRB endpoint



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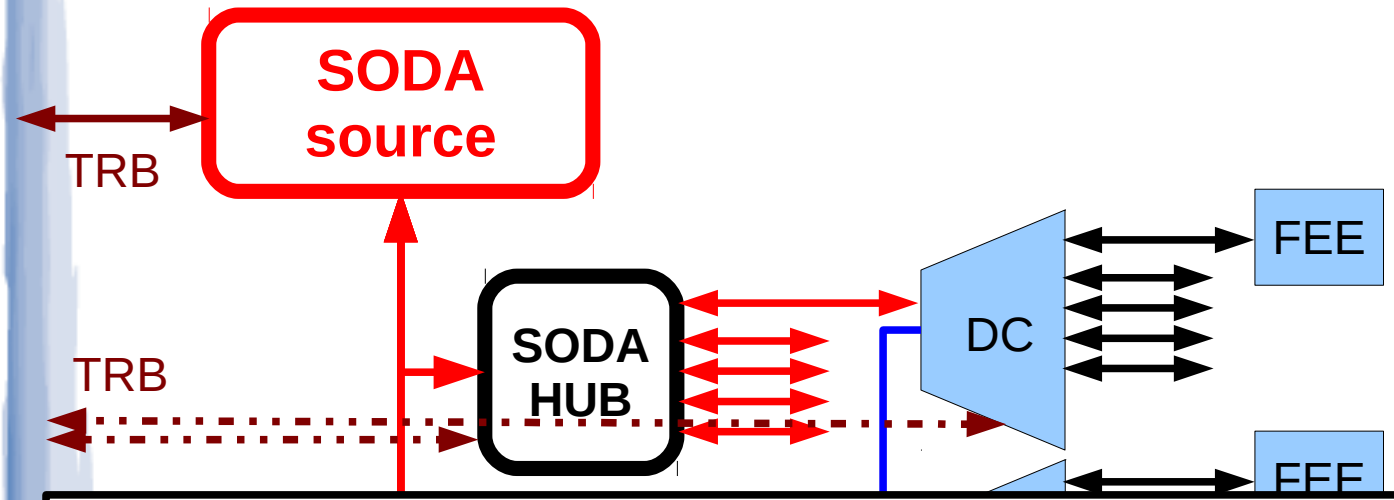

SODA link:

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- Synchronous (only in one direction)
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Done:

- SODA source with built-in hub
- SODA endpoint (DC)

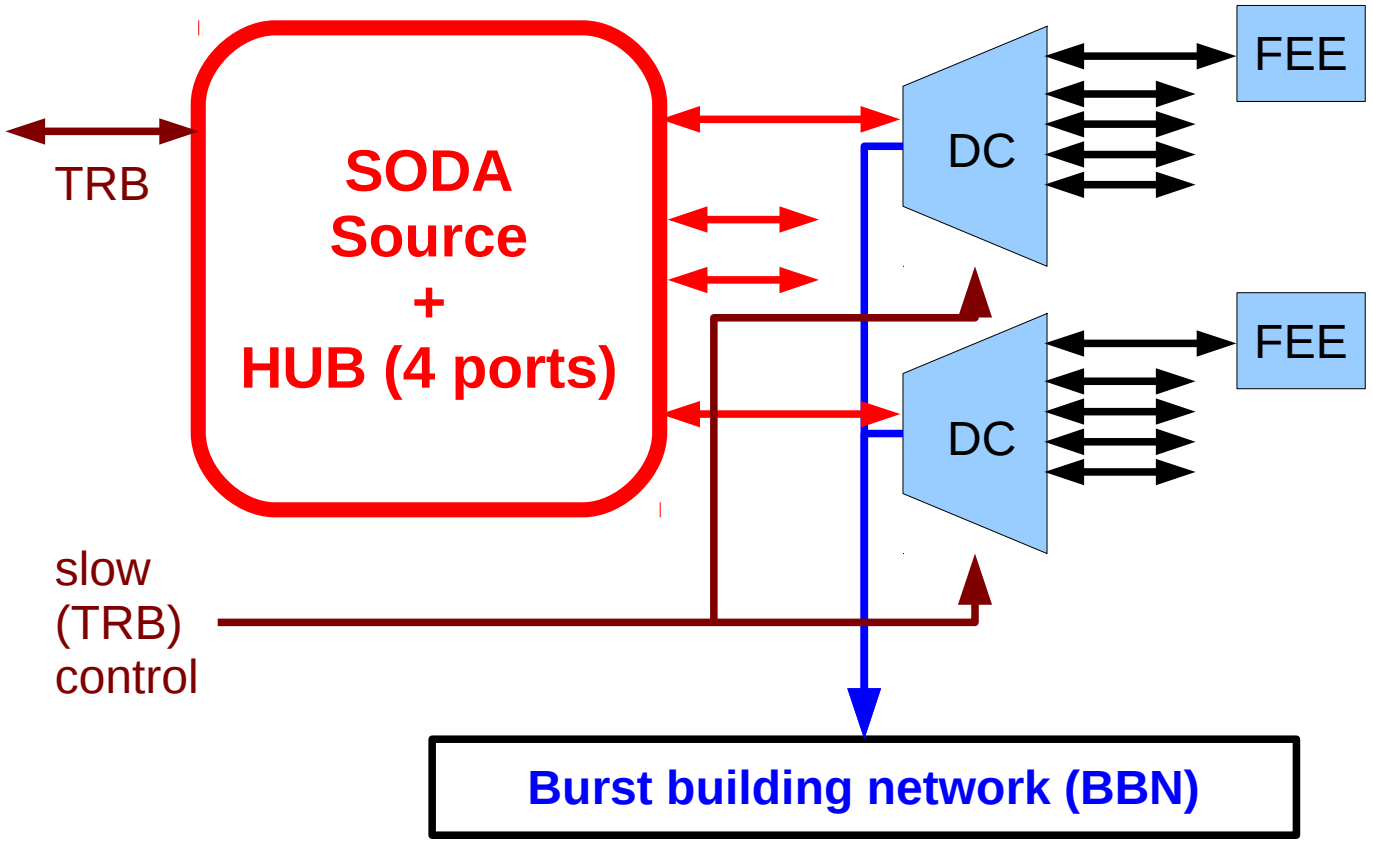
Work in progress:

- SODA hub

subsystem

Burst building network (BBN)

Current Test Set-up



- The readout system may include up to 4 DCs
- Each DC has separate inputs for SODA and TRB
- SODA hub is being developed

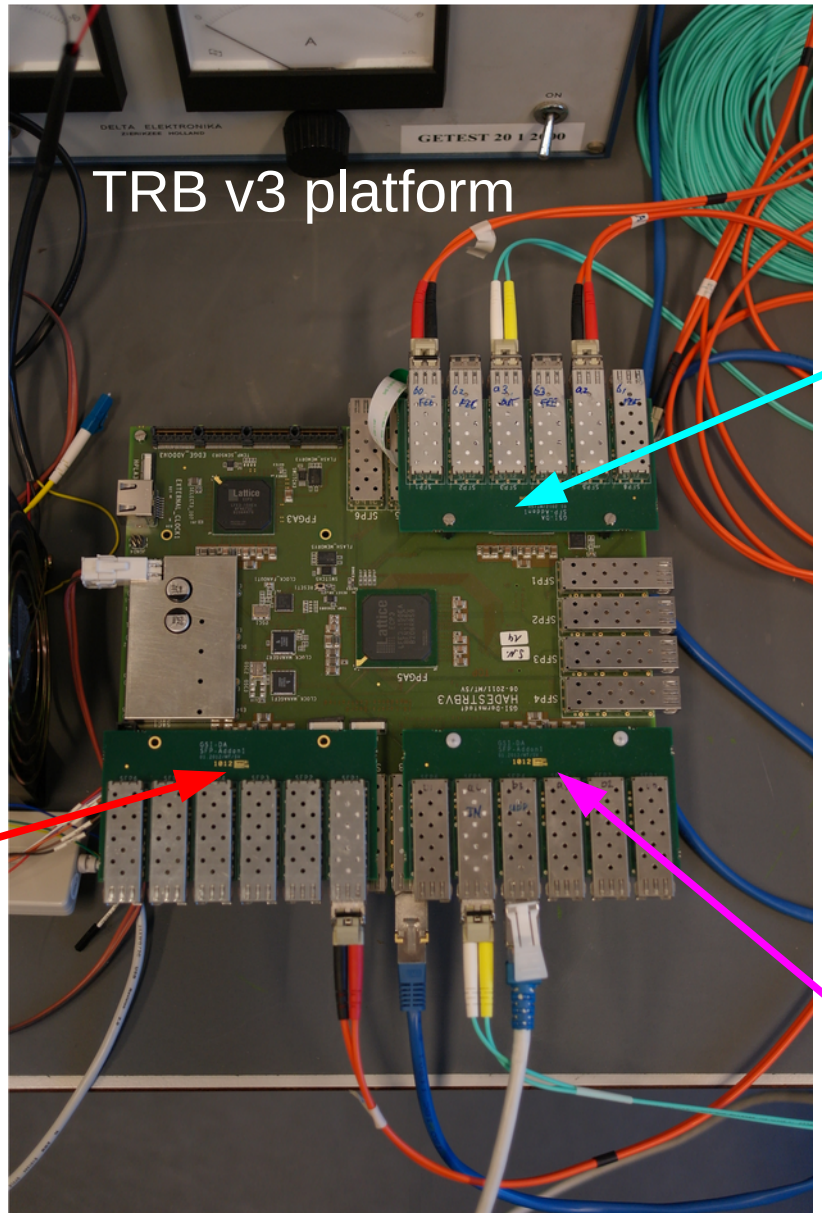
Current Test Set-up

All optical links operate at 2 Gb/s

Synchronous Clocks

ADC operates at 80 MHz

SODA source + Hub (4 ports)



EMC DC:

- 4 FEE inputs
- 1 SODA input (has built-in SODA source for stand-alone operation)
- 1 output to BBN (2 Gb/s link)
- 1 TRB input (copper pair from the central FPGA)

BBN receiver (PC interface):

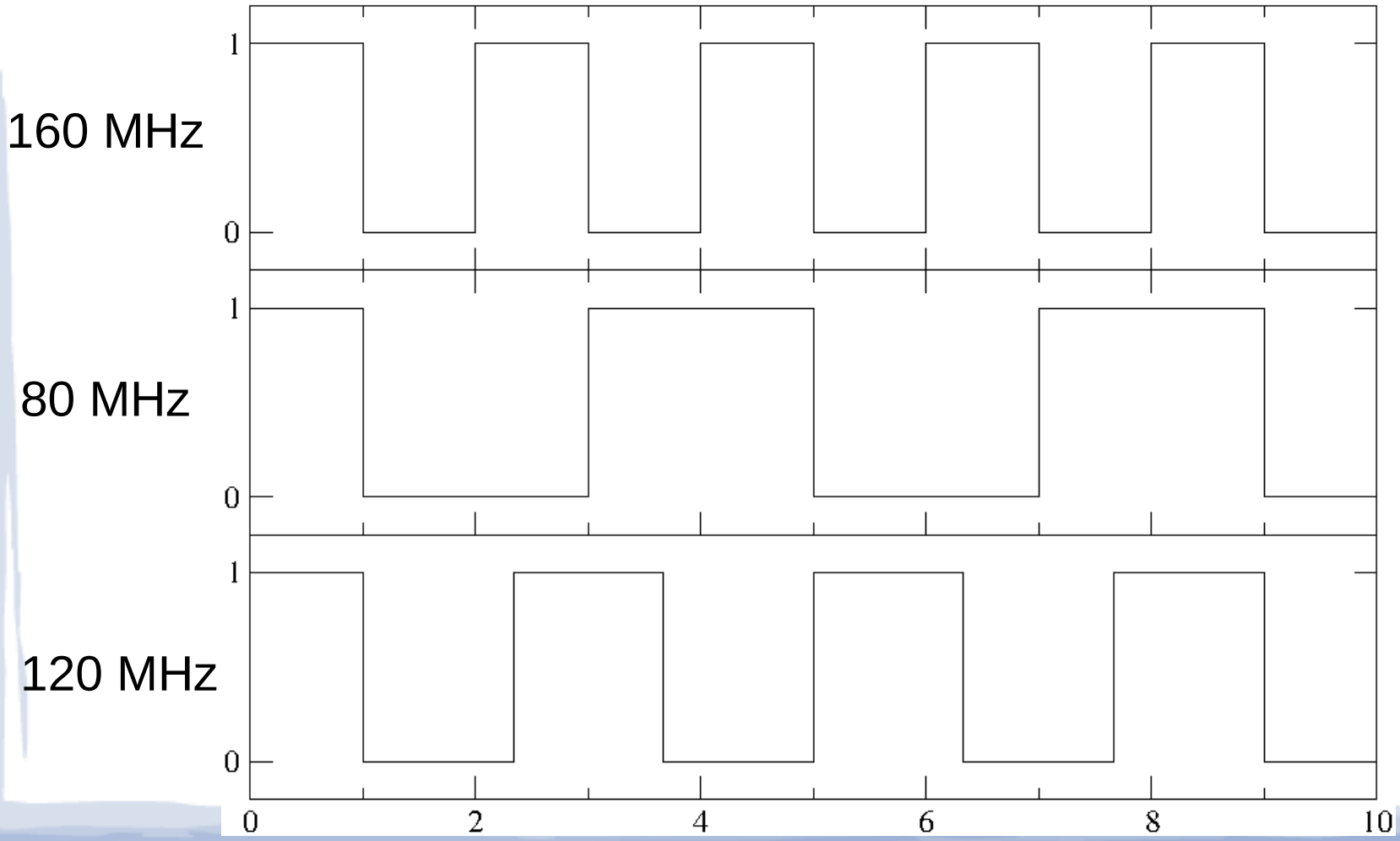
- Receives data from DC (2 Gb/s link)
- Re-transmit data using GBE link (UDP protocol)

Synchronous Clocks

N * 25 ns (periode of 40 MHz clock)

Start of superburst

Start of superburst



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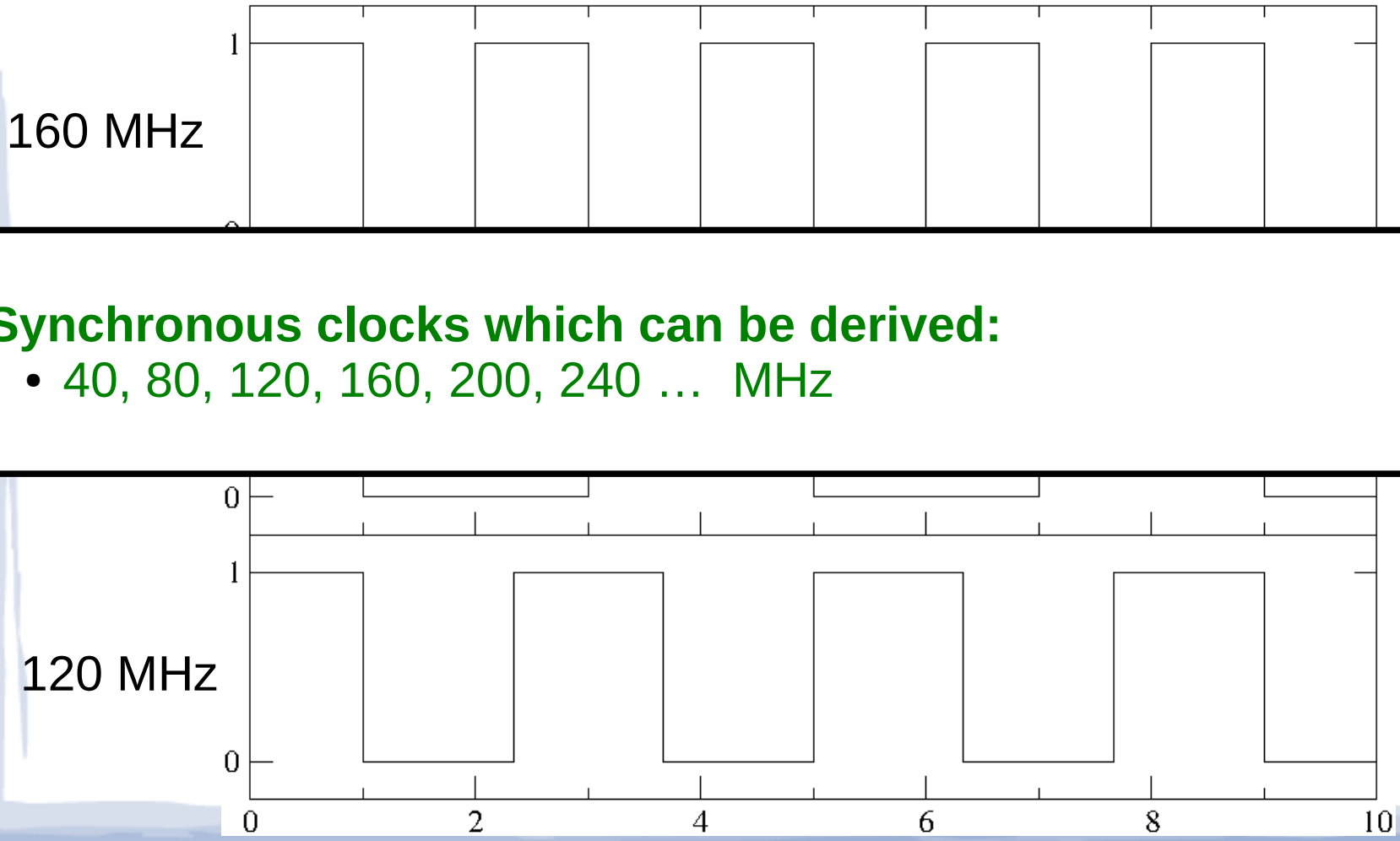
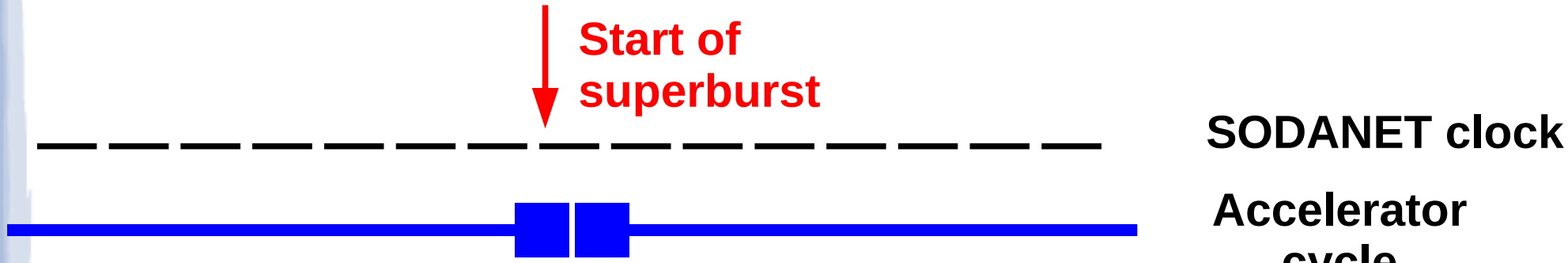


Synchronous clocks which can be derived:

- 40, 80, 120, 160, 200, 240 … MHz

Start of a Super-burst



Accuracy of the super-burst start:

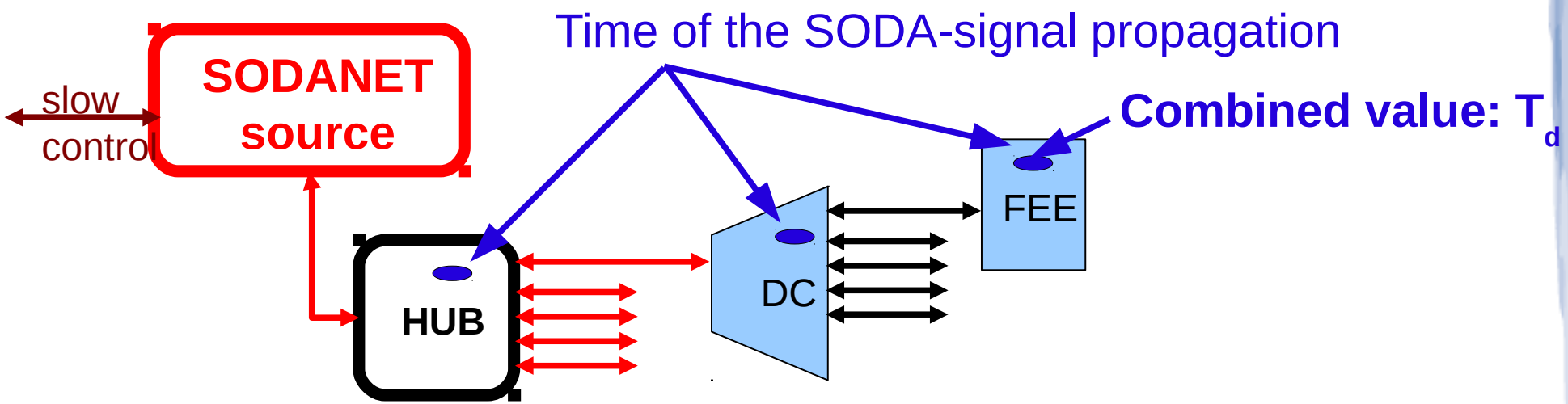
- 160 MHz clock: 6.25 ns
- **40 MHz clock: 25.00 ns**

Super-burst signals will not be periodic:

→ **Is bookkeeping of each super-burst length required?**

→ **Is the global timing required?**

Timing with SODANET



Procedure of time-stamp assignment:

- Each digitizer (FEE) has own timing
- Local “time zero” is reset with each SODA command “start of a superburst”
- Each hit time-stamp is corrected with a T_d value
- After correction the time-stamp the hit data, including current superburst number, are sent to DC module
- At the DC module decision is taken to which superburst the hit belongs

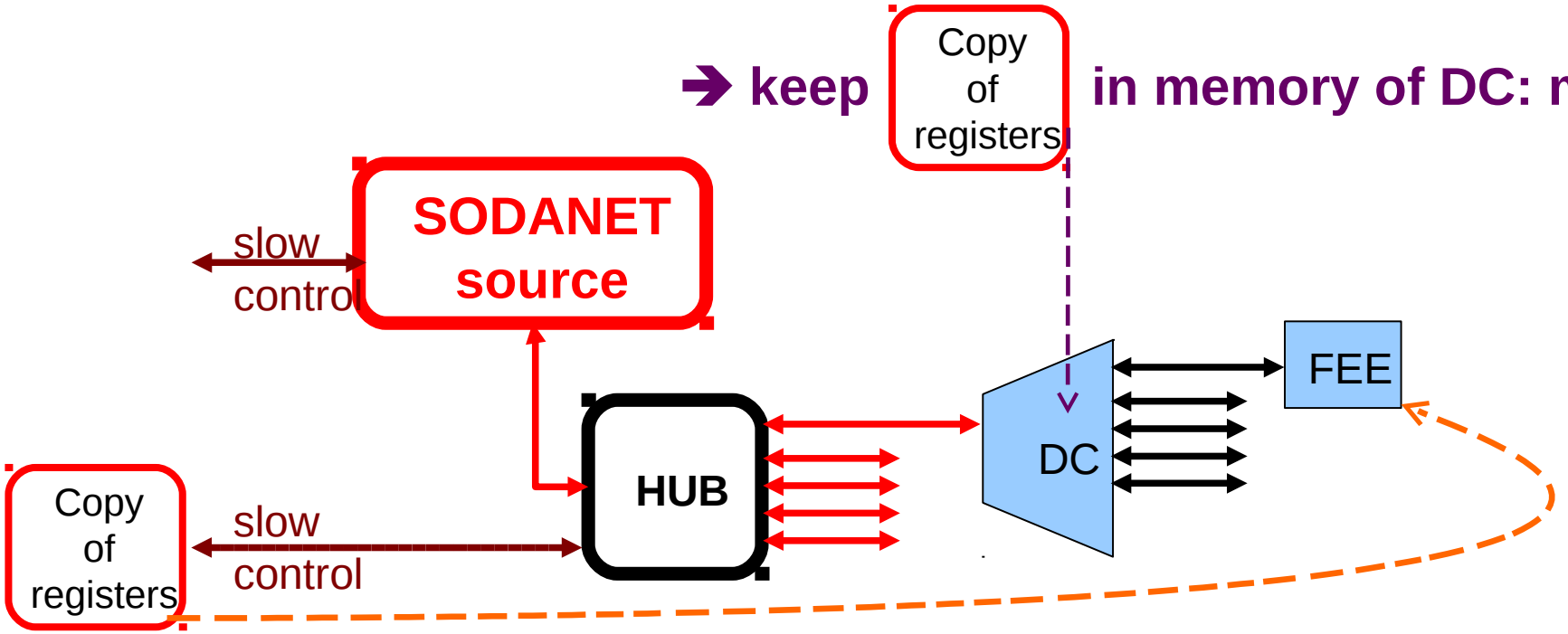
Recovery of EMC Digitizer

configuration change requires restart:

- reconfigure FPGA
- reprogram registers used by the on-line feature-extraction algorithm

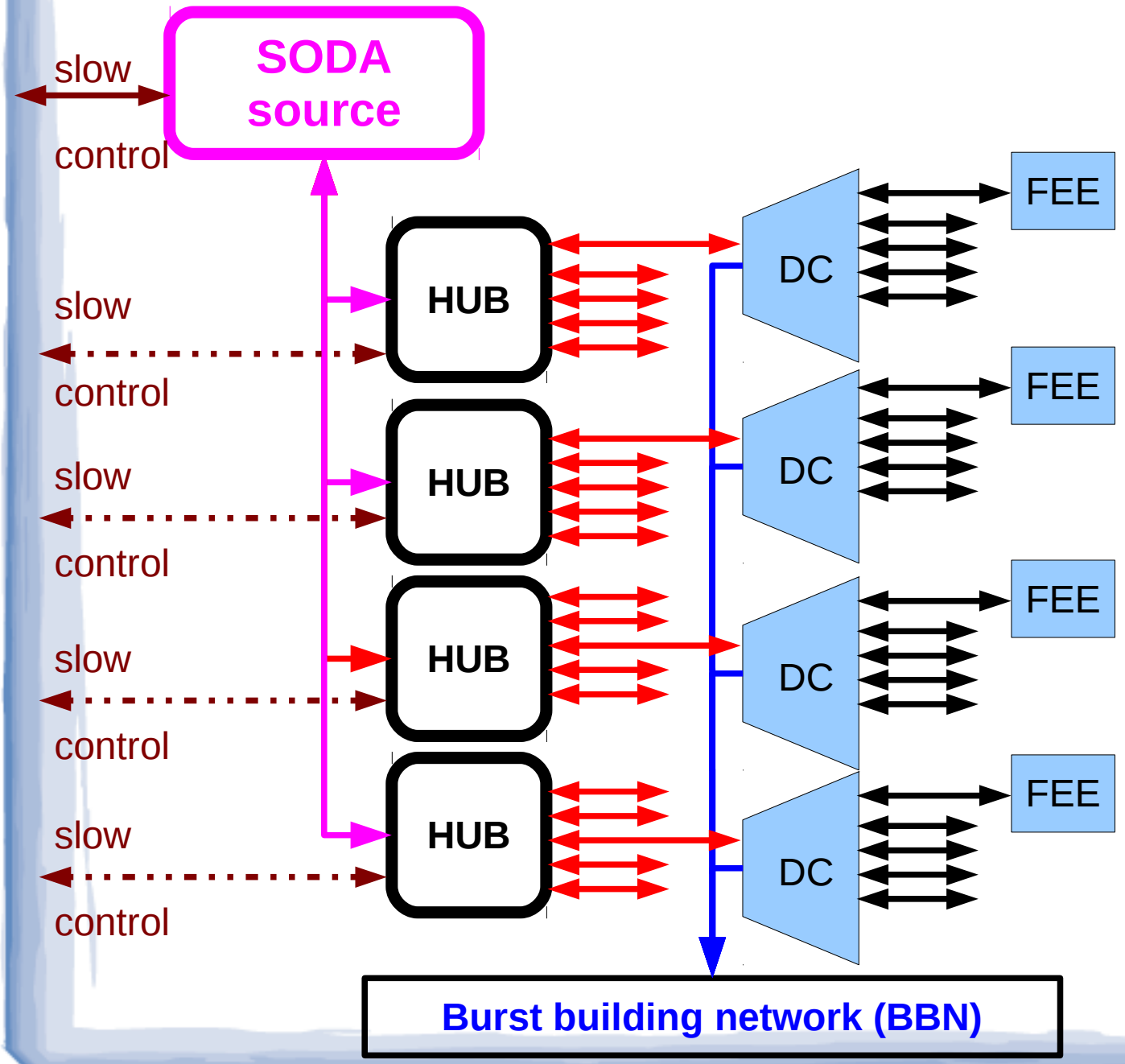
Fast reprogramming is crucial for decreasing the dead time:

too slow (~seconds) via slow control



Together with a fast reload of configuration from a flash memory: implemented reboot procedure takes ~ 10 ms

Step II
Each HUB has separate separate TRB input



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Summary

- **SODANET on TRB v3 (Lattice ECP3) platform**
  - SODA-only source with four outputs is completed
  - Complete system with two EMC DC and two EMC FEE has been tested
  - Generation of synchronous clocks multiple of 40 MHz is implemented and tested

  - The complete SODANET-HUB code is being checked by the TRBNET expert (Jan Michel)

- **SODANET on Xilinx Kintex-7 platform**
  - Is required for the EMC, MVD; by the CBM collaboration
  - Working group is set-up to port TRBNET to Kintex-7 platform (SODA part should work without modifications)