

II. Physikalisches
Institut

JUSTUS-LIEBIG-
UNIVERSITÄT
GIESSEN



Status of PTDAQ and Results of MAMI Test

M.N. Wagner, T. Geßler, W. Kühn, J.S. Lange, B. Spruck, M. Werner

II. Physical Institute, Justus Liebig University, Gießen, Germany

This work was supported in part by BMBF (05P12RGFPF), HGS-HIRe for FAIR and the LOEWE-Zentrum HIC for FAIR



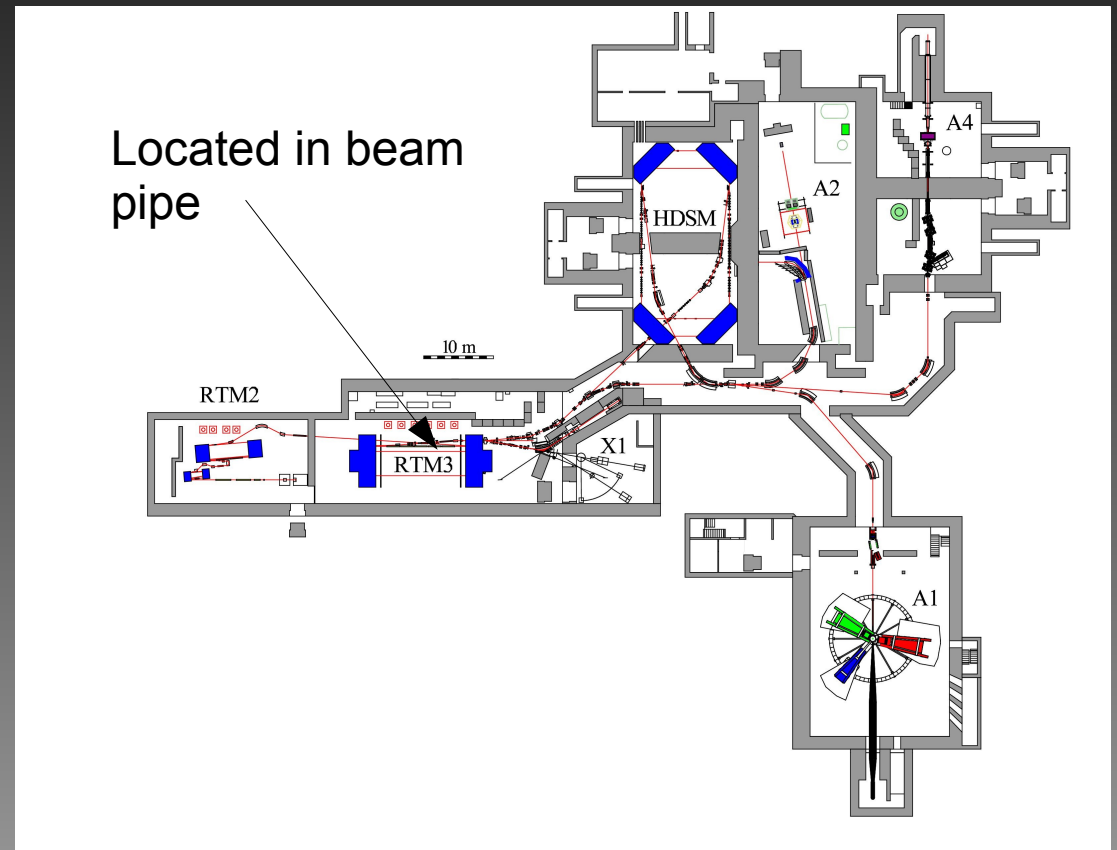
Bundesministerium
für Bildung
und Forschung

HGS-HIRe *for FAIR*
Helmholtz Graduate School for Hadron and Ion Research

HIC | **FAIR**
for
Helmholtz International Center

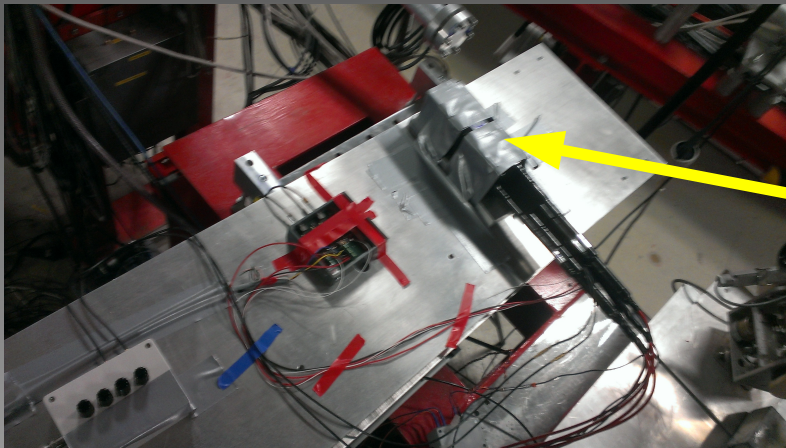
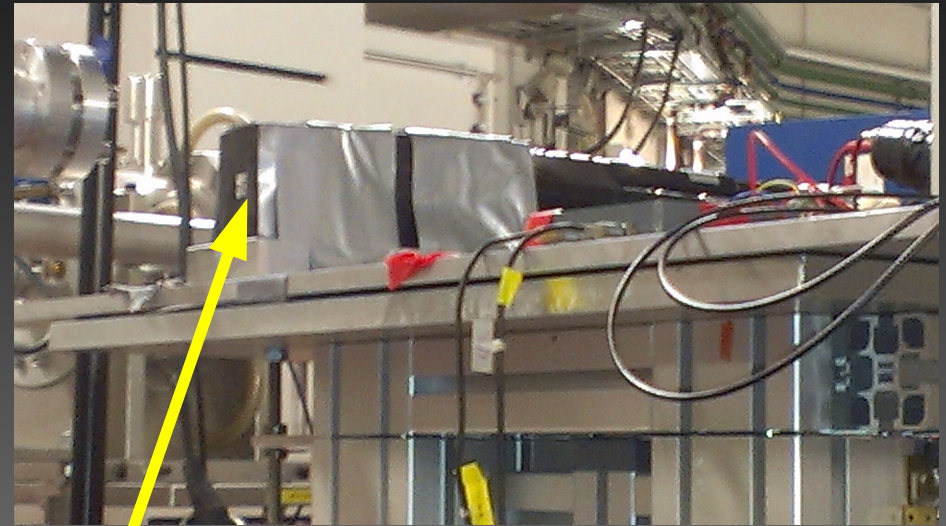
Parasitic Beam Test @ MAMI

- Beam parameter
 - 210 MeV electrons
 - 0.003 - 2 MHz event rate

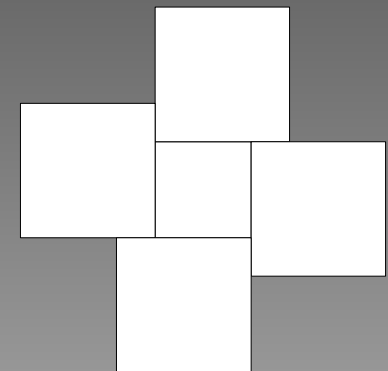


Parasitic Beam Test @ MAMI

- Detector:
 - 1 mini PWO crystal
 - 2 HAMAMATSU SI-PM
 - 4 PANDA crystals

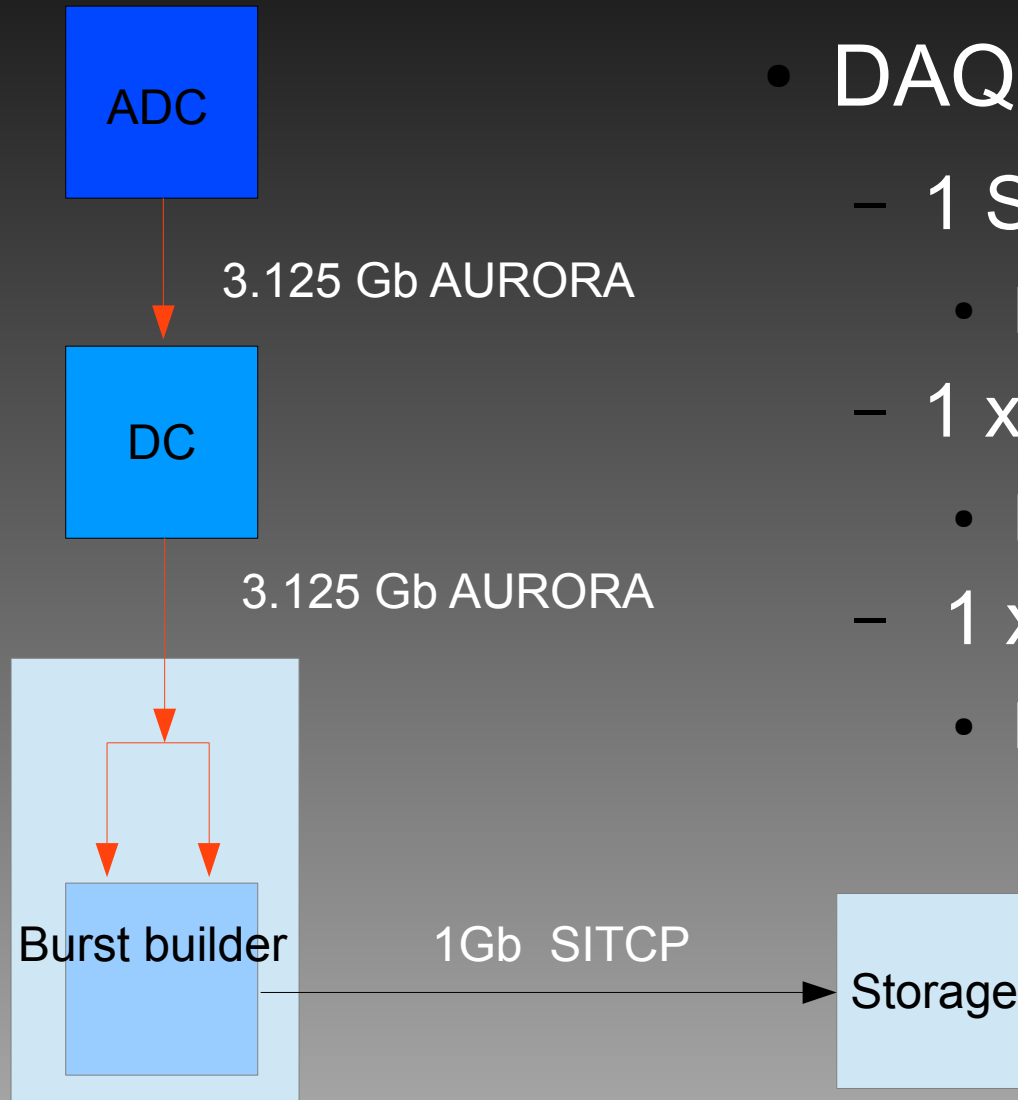


Detector

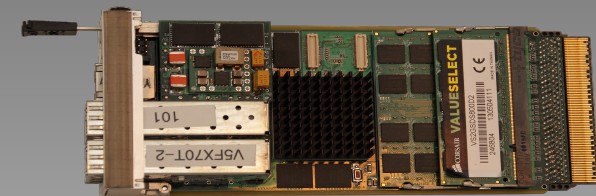


Detector matrix

PTDAQ Chain



- DAQ chain
 - 1 Sampling ADC (Uppsala)
 - Pile-up mode
 - 1 xFP version 2
 - Data concentrator
 - 1 xFP version 3
 - Burst-builder



xFP board

Results



- Stable Connection between DC and xFP
- 2-Input burst building successful
 - for $\sim 15 * 10^6$ events
 - Data rate of ~ 1 Gbit/s from xFP to PC

Whats Next?

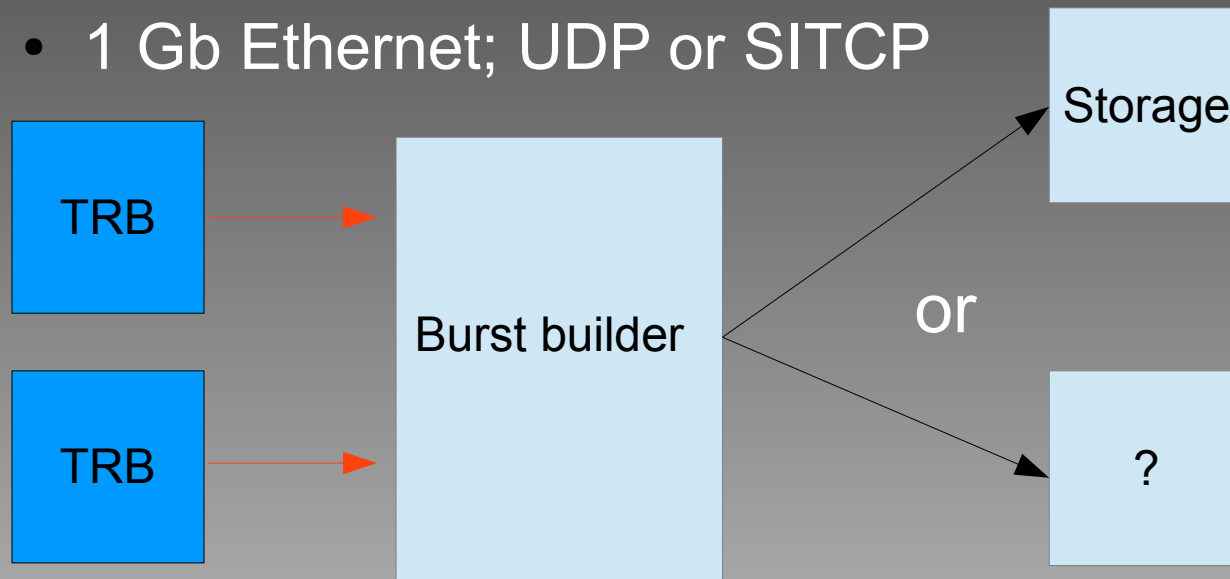
- SODA connection test

- 2 TRBv3

- 1 Gb Ethernet; Transport protocol (P. Schakel)

- 1 CN

- 1 Gb Ethernet; UDP or SITCP



Whats Next?



- SODA connection test
 - 2 TRBv3
 - 1 Gb Ethernet; Transport protocol (P. Schakel)
 - 1 CN
 - 1 Gb Ethernet; UDP or SITCP
- Participation on beam tests, if possible?
 - Need informations
 - What DC?
 - What transport protocol?



Backup

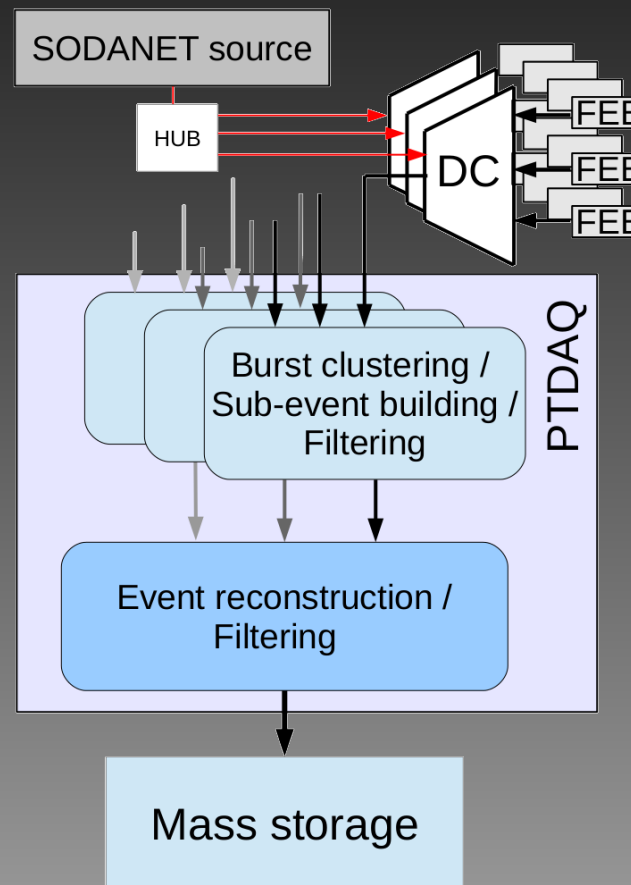
Prototype Trigger-less Data Acquisition (PTDAQ)

First step of the pre-assembly DAQ:

- Small but scalable start version
- Parts of the final functionalities
- Similar hardware to the final DAQ

Functionalities:

- Digitized data received from front end electronics (FEE) is synchronized at the data concentrator (DC)
- Sub-event building and first filter algorithms
- Event building and second stage filter algorithms



PTDAQ can be used for testing:

- Synchronization of data acquisition (SODANET)
- Sub detector prototypes
- Reconstruction algorithms
 - FPGA based Helix tracking

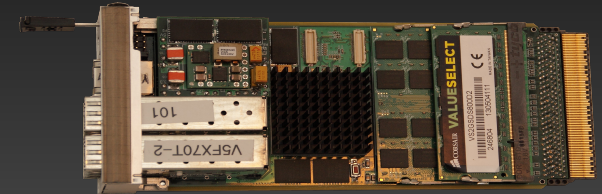
Hardware Components

PTDAQ setup:

- μ TCA shelf
- 4 xTCA compliant boards
- 9 data concentrator boards

xTCA compliant board:

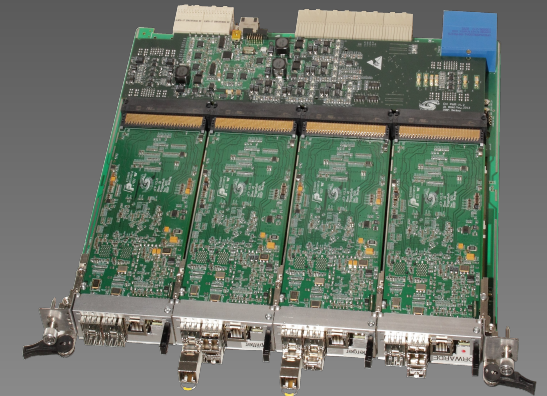
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 x SFP+ cages
- 6.25 Gbit/s optical interfaces
- AMC form factor
- 1 Gbit Ethernet



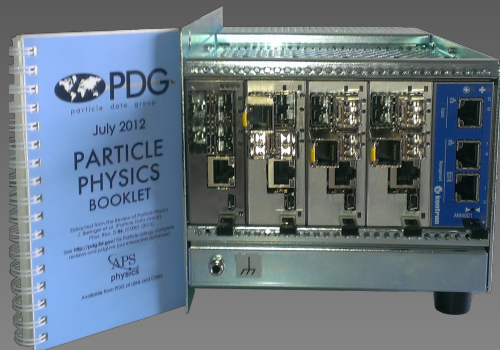
xTCA compliant board used as a main hardware component of the PTDAQ.

Compute Node:

- Xilinx Virtex 4
- ATCA based carrier board
- Up to 4 xTCA compliant boards



ATCA based Compute Node. Will be used in the upgrade of the PTDAQ. Developed in cooperation between IHEP Beijing and JLU Gießen



PTDAQ setup with 4 xTCA compliant boards and a shelf controller in a μ TCA shelf

Status & Outlook



Status:

- One board setup
 - Connection for of up to 4 DCs
 - Tested with simulated DCs

Outlook

- Tests with different types of DCs
- Test different kinds of detectors with beam
- Upgrade to ATCA based Compute Node DAQ using carrier boards and xTCA compliant boards