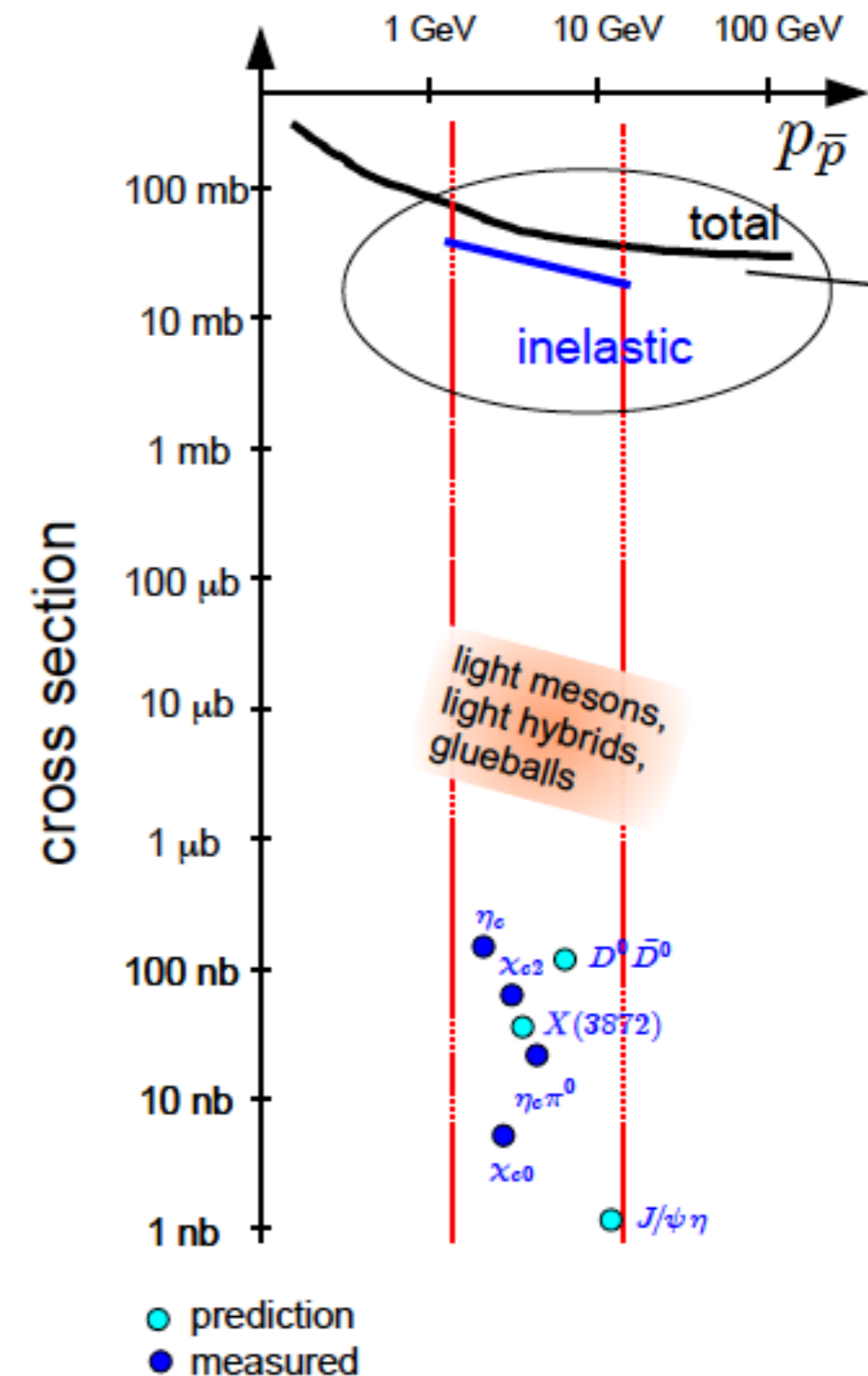


# Data Acquisition and Event Filtering

- Problem: finding the needle in the haystack
- total inelastic cross section
  - 50 mb
- Interesting physics
  - most channels  $< 100$  nb
- $2 \times 10^6$  interactions /s
- Data rate after FEE reduction: 200 GBytes/s
  - 17 PBytes/day
- Goal for online event filtering:
  - reduce “background” by factor of 1000



# FAIR Tier 0 Data Center

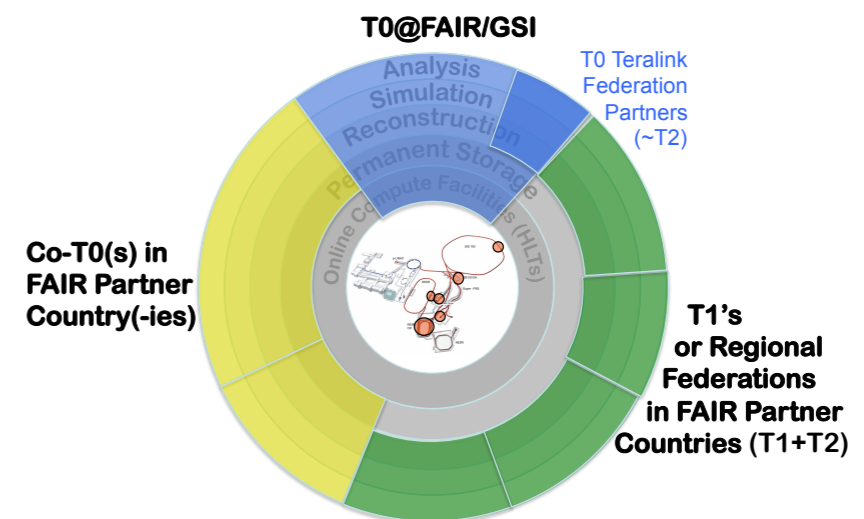
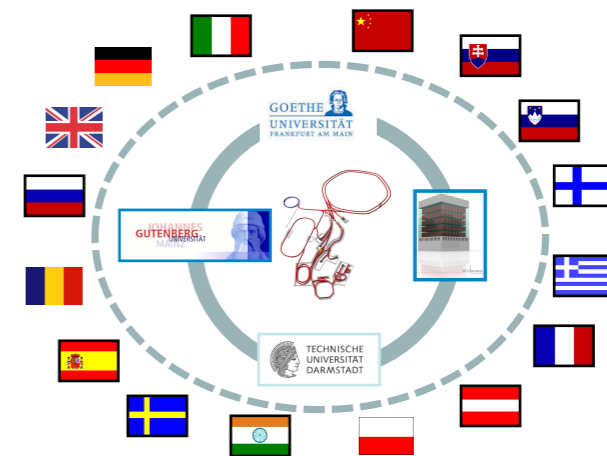
Estimated total for full FAIR  
FAIR Tier 0

- 300.000 CPU-cores
- 35 PByte/year Online-Storage (HDD)
- 30 Pbyte/year Permanent-Storage (Tape)

Comparable resources in FAIR  
partner countries

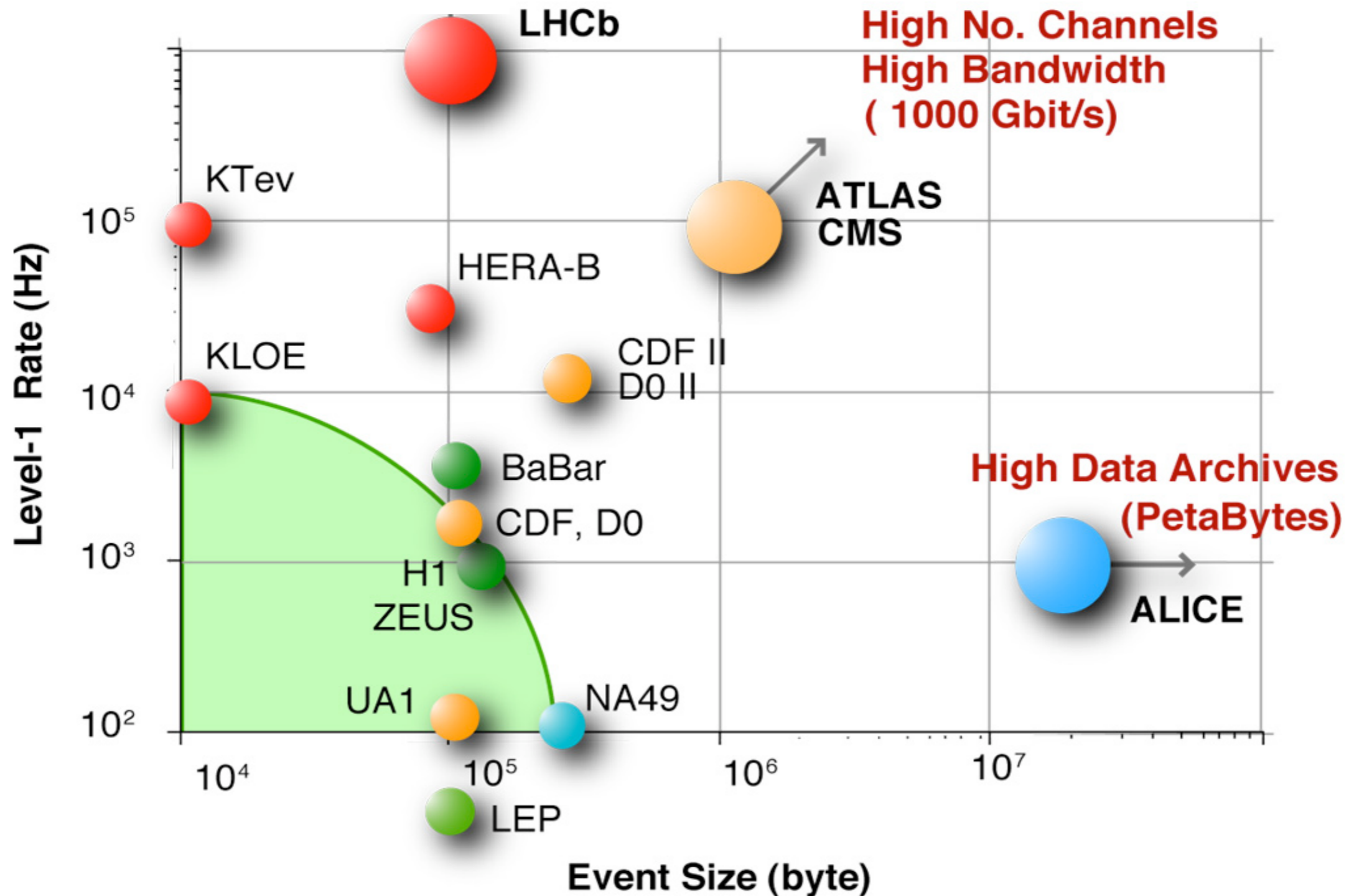
## Key Points

- Few big, highly efficient data centers
- Further partner connected via regional federations



# The PANDA DAQ Challenge

● PANDA

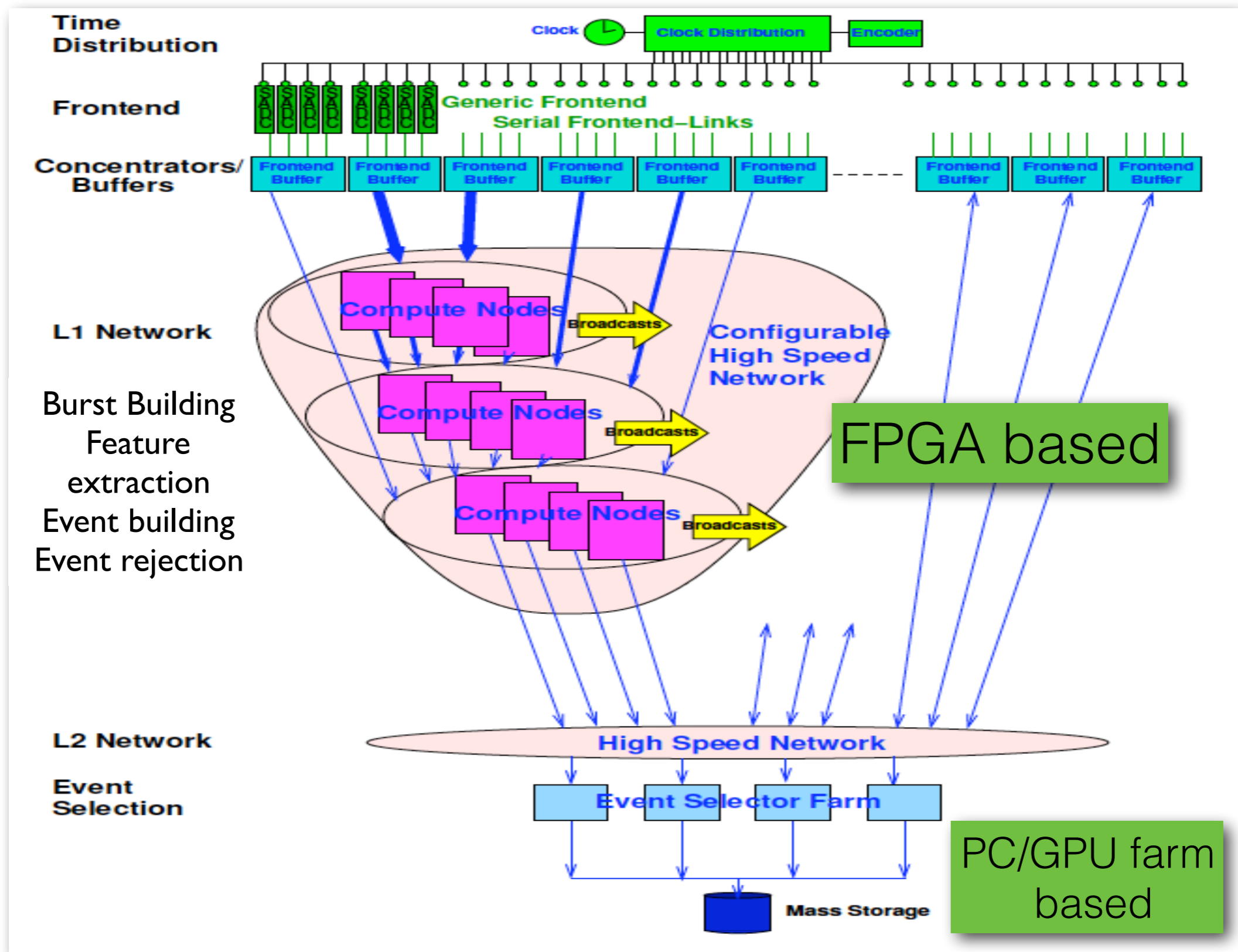


# PANDA DAQ Approach

- Freely streaming data :“Trigger - less”
  - No hardware triggers
    - However, there will be event filtering, we cannot record everything !!
- Autonomous FEE, sampling ADCs with local feature extraction
- Time-stamping (SODAnet)
  - Data fragments can be correlated for event building
- Caveat: the high-rate capability implies overlapping events !!!
  - average time between two events can be smaller than typical detector time scales
  - This “pile-up” has to be treated and disentangled
  - Real-time event selection in this environment is very challenging and requires a lot of studies

# Challenges

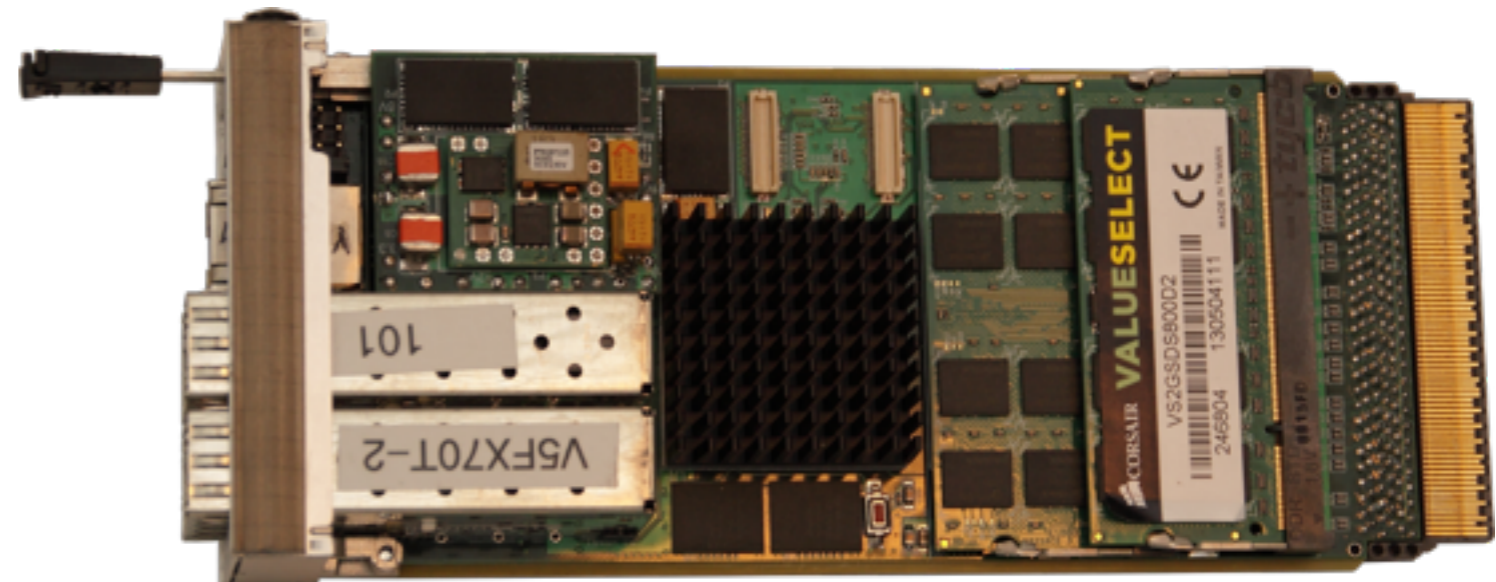
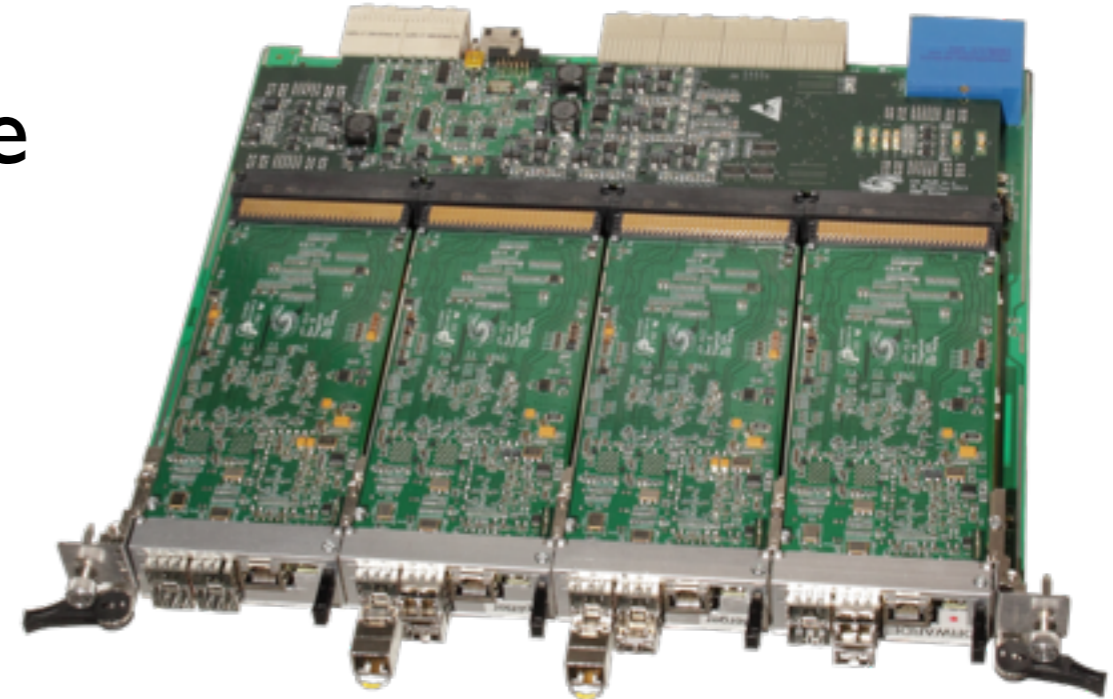
- How much can we reduce the primary data rate ?
  - Software trigger group (principal physics simulations)
    - Answer: maybe up to factor 1000, some loss of efficiency
- Caveat: event based estimate, but overlapping data @ 20 MHz
  - A priori, there are no “events”, there is just a stream of “data” from each sub-system
  - Worst case: if we cannot assemble events online, we have to store everything, because we cannot reject anything !
    - 200 GB/s -> 17 PB/day, compare to 30 PB mass storage/year @ FAIR Tier 0
      - Impossible !
    - Even running at 200 KHz only would exceed the available yearly storage capacity
- The PANDA physics program is not feasible without effective filtering, reducing the event rate by more than 2 orders of magnitude
- This works only if we are able to reconstruct most of the raw data in realtime. Massive challenge !
  - We need full time-based simulation and reconstruction software to judge feasibility and determine required resources (work in progress !!!)



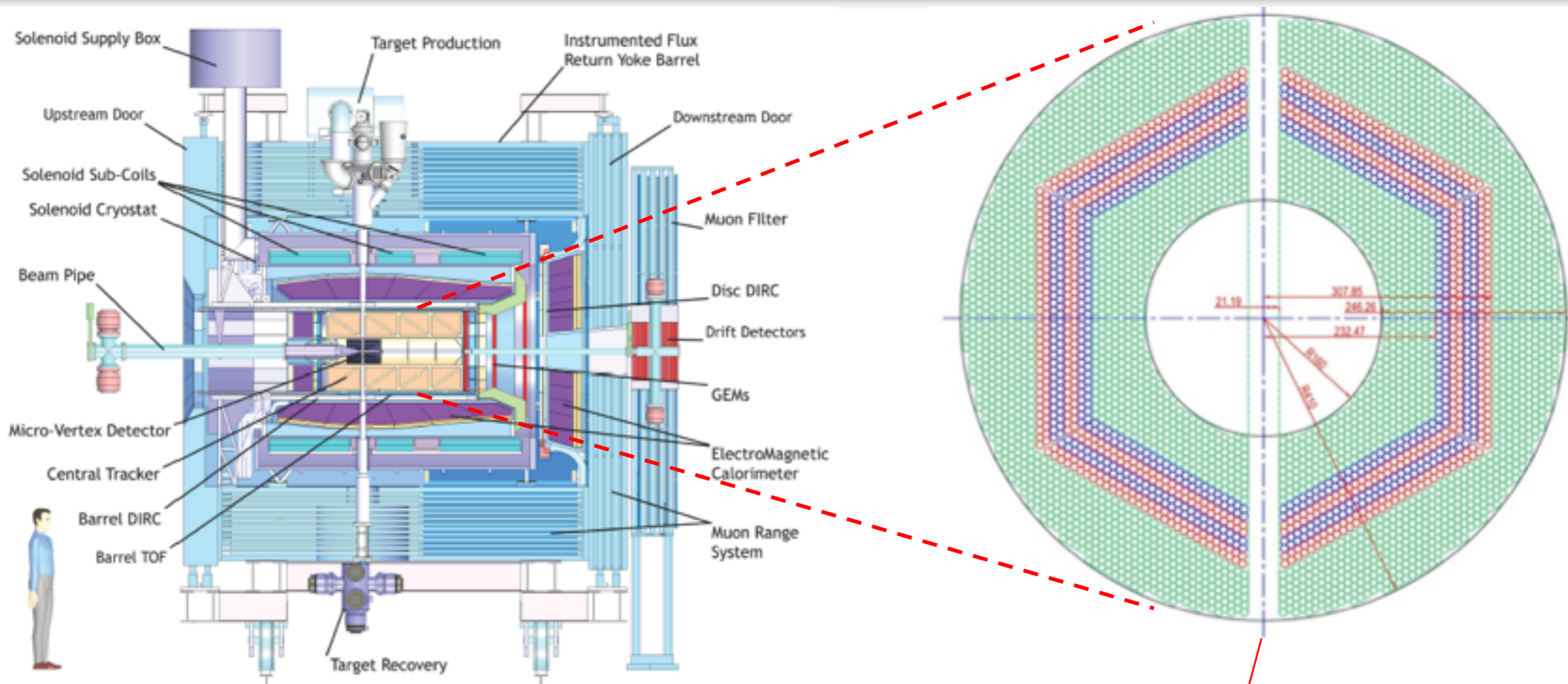
# PANDA DAQ / Event Filter

# Building Blocks (L1 network)

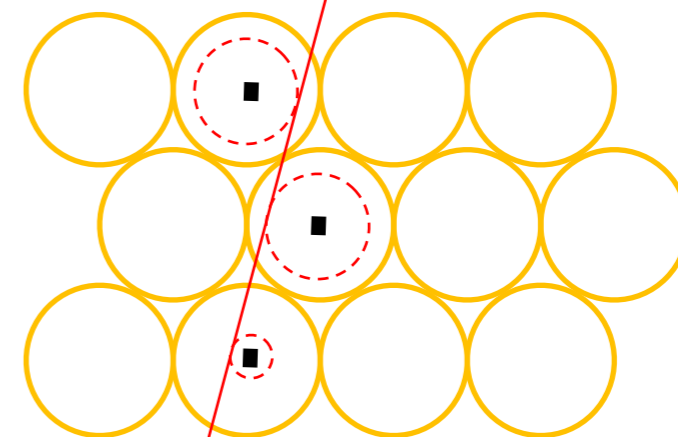
- FPGA based Compute Nodes (CN)
- ATCA standard, full mesh backplane
- 4 + 1 FPGA Virtex5 70FXT
- 16 optical links, GbE
- 18 GBytes DDR2 RAM



# Application Example: Tracking for STT



- 4636 Straw tubes
- 23-27 planar layers
  - 15-19 axial layers (green) in beam direction
  - 4 stereo double-layers for 3D reconstruction, with  $\pm 2.89$  skew angle (blue/red)

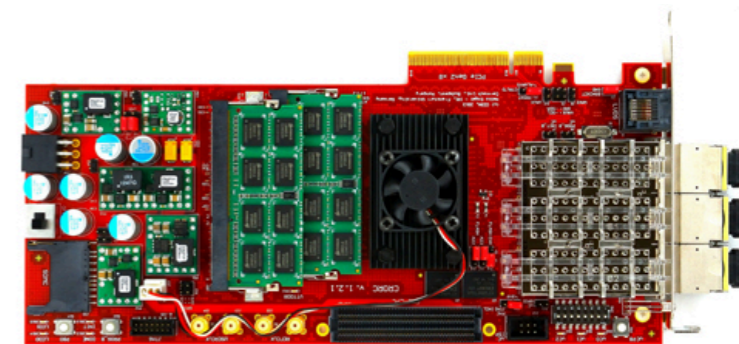


From STT : Wire position + drift time

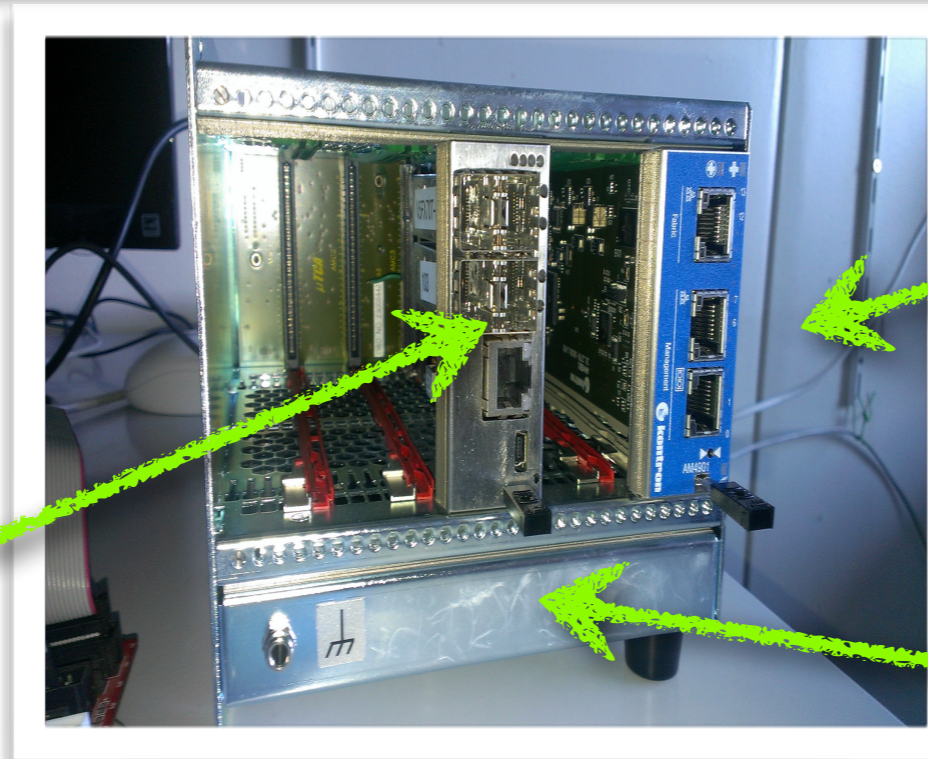


# Current Activities

- Hardware: outdated, needs upgrade to most recent FPGA generation
  - Move from Virtex 5 to Kintex 7 UltraScale(+) architecture
    - BMBF funding for this project available
- Toy DAQ system with scaled down architecture for detector prototype tests in realistic DAQ environment
  - Freely streaming, FEE feature extraction, event building, high level feature extraction on FPGA, L2 network processing with small farm for final event selection, full support for SODAnet
  - First test with beam at MAMI (tagged photon facility & EMC prototype) this month
- Connectivity to server farm: two solutions explored
  - ATCA backplane connection to 10Gb Ethernet switch
  - PCIe card with optical links (C-RORC ALICE development by Budapest group)



# Toy DAQ Hardware



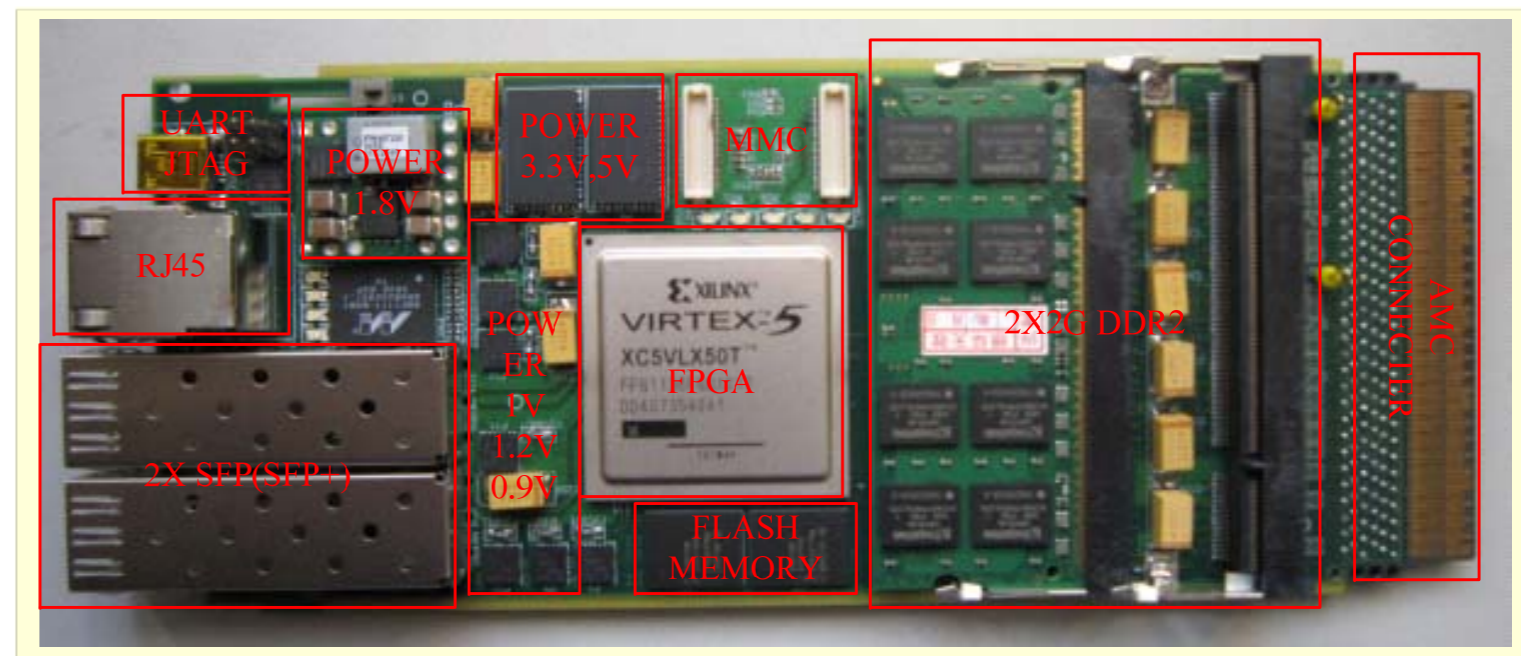
Shelf manager  
(networked)

Compute Node  
xFP module

uTCA shelf

- xFP module (building block of ATCA Compute Node)

- XILINX Virtex 5 70FXT FPGA
- 4 GB DDR2 Ram
- 4 optical links (up to 6.5 Gb/s)
- Gbit Ethernet



# Consequences of PANDA staging scenario

- Rate down by a factor of 10 (2 MHz)
  - Full time-based simulations less critical
  - Requirements for background rejection:
    - Factor 100 (down by one order of magnitude)
- Initially no Cherenkov detectors:
  - No discrimination between charged pions and kaons
    - Problem for open charm physics
  - Can still trigger on J/Psi and displaced vertices ( $K_s^0$ , Hyperons)
    - Need to develop online tracking algorithms for displaced vertices
    - Impact on rejection rate needs to be explored by simulations

# Scrutiny Group Conclusions

## Summary:

DAQ developments are on a promising way. There is good progress in interfacing FEE to DAQ. The DAQ-DCS interface has to be defined. Basic DAQ system tests have been completed successfully. The funding situation is alarming: we request the PANDA management to take action immediately. DAQ and Computing managers must jointly organize the completion of urgently needed time-based simulations.

# Ressources and timelines

- Major contributors to DAQ (depending on division between front-end electronics and core DAQ components):
  - Groningen (SODAnet, EMC feature extraction)
  - IHEP Beijing (Compute Node Hardware, PCB design and production)
  - Krakow (SODAnet, Core DAQ Firmware)
  - Uppsala (TRB4 data concentrator)
  - Giessen (Compute Node design and hardware debugging, Core DAQ firmware, event filtering algorithms, DAQ coordination)
    - **With my retirement (9/2017 - maybe 8/2018), this group will cease to exist**
- **Potential interest of new group: T. Kiss, J. Imrek et al. (Wigner Research Center for Physics, Budapest)**

# Ressources and Timelines

- Funding situation:
  - R&D funds available, **no construction funds (and no EOI !)**
  - **Shortage of manpower**, not easy to get new students in view of the currently uncertain situation for FAIR & PANDA
- TDR: **Decision to be made:**
  1. Staged TDR (2 MHz, no treatment of overlapping events)
    - Later: second TDR for upgraded DAQ supporting 20 MHz
  2. Full TDR
- **Timeline for TDR depends on FAIR / PANDA schedule (2022 or 2025 or ???)**
  - TDR to be submitted 2-3 years before construction of DAQ:
    - New generation of CN hardware (Xilinx Kintex 7 UltraScale(+) based) should be available late 2017 and could still be the basis in a staged TDR for a PANDA physics start in 2022
    - **If PANDA will be further delayed (2025), the new generation of hardware will be obsolete, too !**