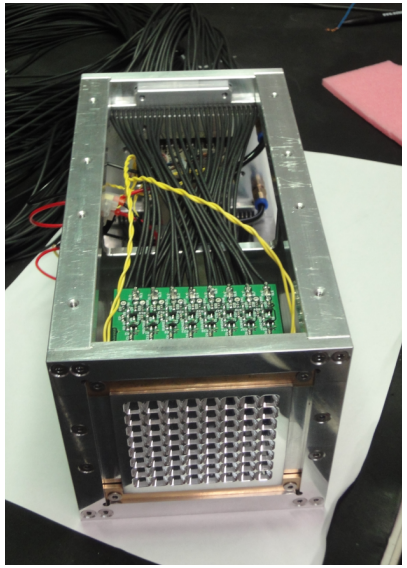
ÖAW
Austrian Academy
of Sciences

# SiPM related projects and perspectives at SMI Vienna

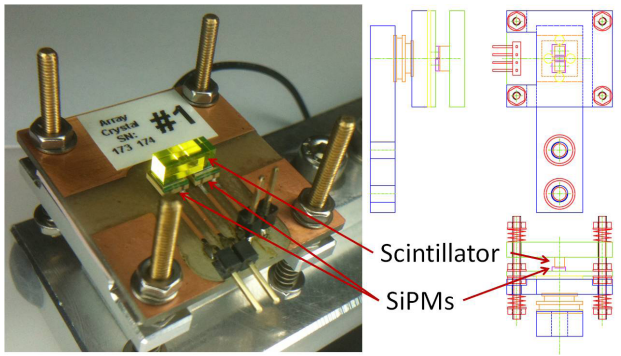

# Current projects - overview

- Position sensitive photo detector
  - 8 x 8 SiPM array for low level light detection (DIRC, RICH,…)
  - 64 Hamamatsu MPPCs (3 x 3 mm², 100 x 100 µm² pixel size)
  - Light concentrator on top
  - 5.6 x 5.6 cm² detection area with 97% fill factor
  - 4 preamplifier boards with 16 preamplifiers each
  - Water- and Peltier-cooling
  - Test beam data are under investigation
  - Simulations and measurements are ongoing
  - We are searching for ASICs for SiPM readout that can be integrated in our setup

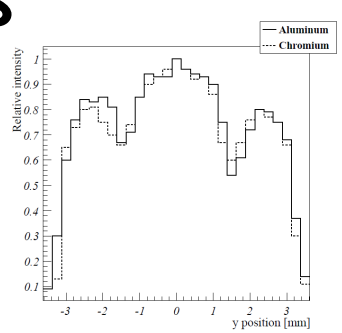


- Recovery time of SiPMs
  - Measurements of the recovery time for different SiPMs using two successive signals with variable delay

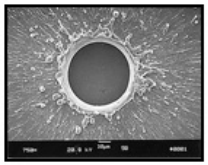
- TOF-PET with SiPMs
  - Implement SiPMs to improve TOF-PET
  - Possibility of new detector designs (compact size)
  - High detector granularity
  - First prototype with 3 x 3 mm² MPPCs is ready



# SiPM array – plans and activities

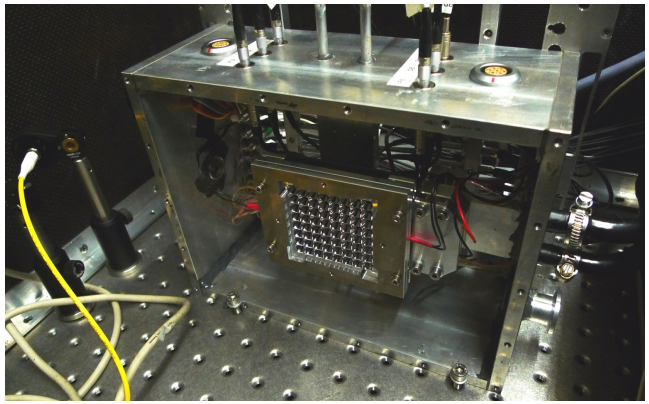



- **Measurements**
  - Scan the whole array to see if all channels are behaving in a similar way → map of the whole array
  - Scan with smaller laser spots using pinholes in the range of the MPPC pixel size and below (10 µm) → better resolution, understand features
  - Study the behavior for different incident angles, which is important for the use in DIRC detectors
  - CERN test beam data are currently under investigation




  - Test different light concentrators (solid pyramids,…) and SiPMs (FBK-irst, full arrays,…) for comparison

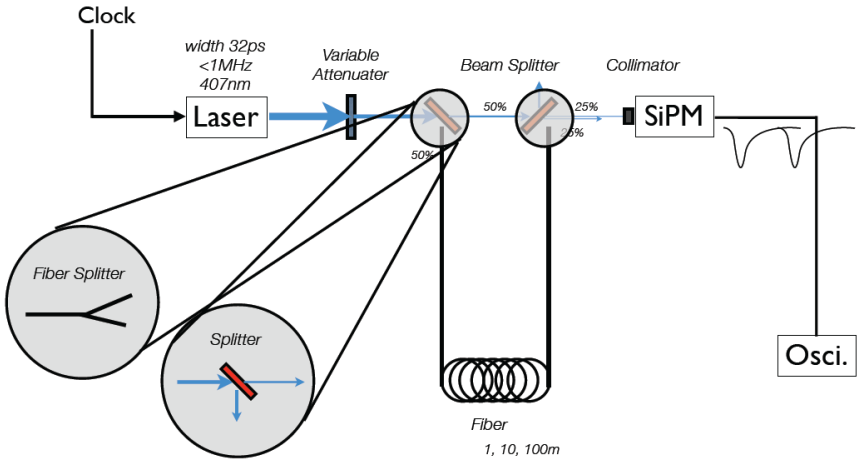
- **Simulations**
  - More sophisticated simulations with exact geometry



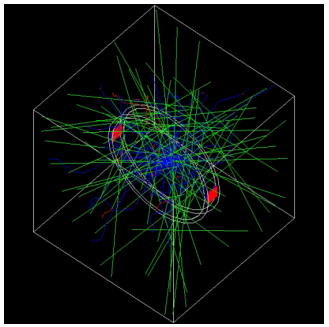
- **Electronics**
  - 64 channels to bias and readout
  - Integrated electronics are needed to reduce size
  - Low noise electronics needed
  - Temperature stabilization crucial
  - Existing ASICs for SiPM readout will be investigated
  - Integrate chips/test boards in the detector
  - Test performance in combination with the SiPM array

# Other projects

- Recovery time measurements
  - Measurements at INFN Frascati are planned in Nov
  - Different delay times (mirrors or fibers)
  - Use sensors with different pixel sizes (different capacitances)
  - Study temperature variations

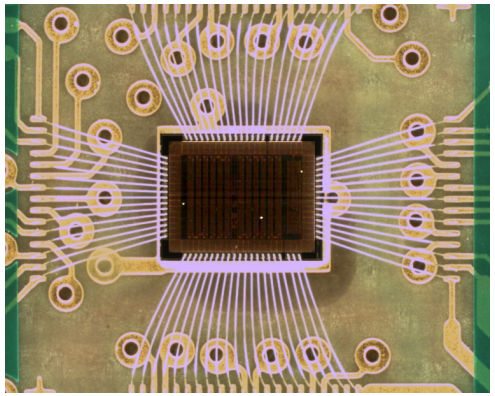



- PET detector
  - First measurements with the prototype detector (Laser and $^{22}Na$ source)
  - Test different scintillator materials
  - Test different detector designs
  - Use ASICs for SiPM readout
  - GATE simulations of detector design, etc.

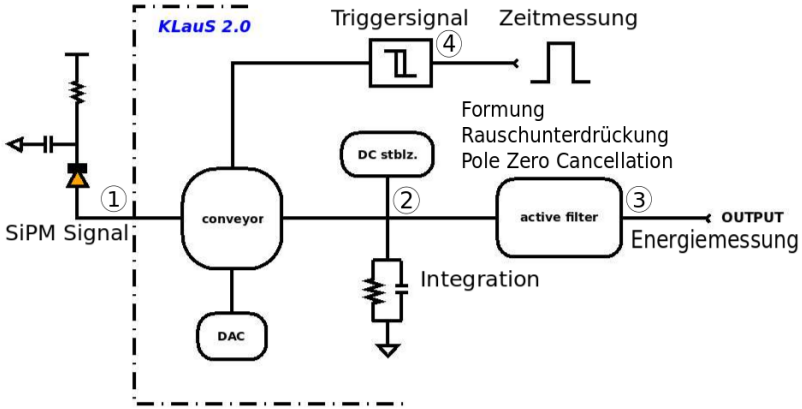


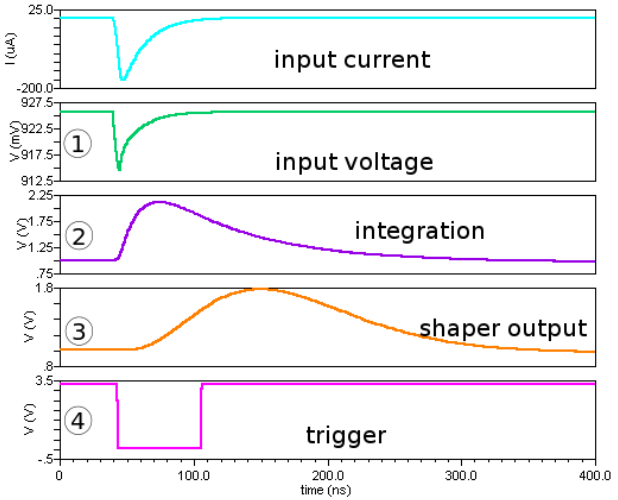
# Integrated electronics – KLauS 2v0

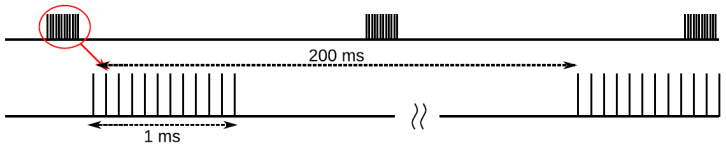
KLauS – Kanäle für Ladungsauslese von SiPMs



- KLauS 2v0:
  - Developed at KIP Heidelberg
  - Dedicated to charge measurement with high dynamic range and fast timing (ILC HCAL)
  - Replaced Klaus 1v0 in Nov 2010
  - 12 channels, individual bias
  - SiPM bias tuning for gain stabilization (DAC)
  - Power gating: 2.5 mW → 25 µW per channel



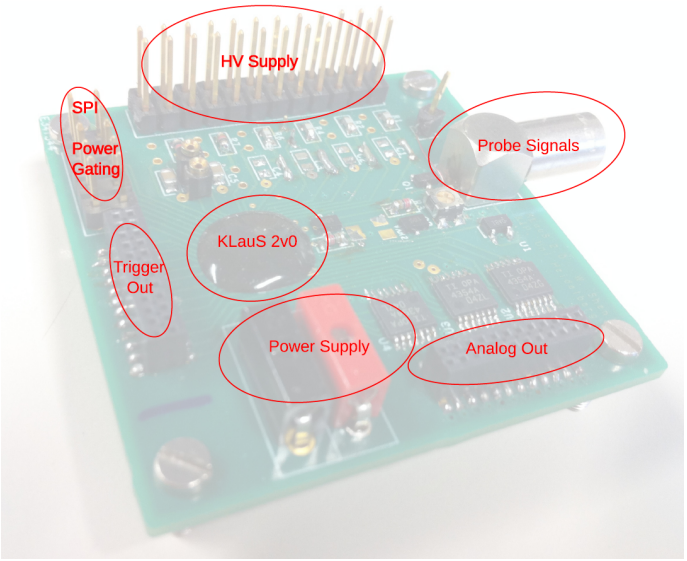



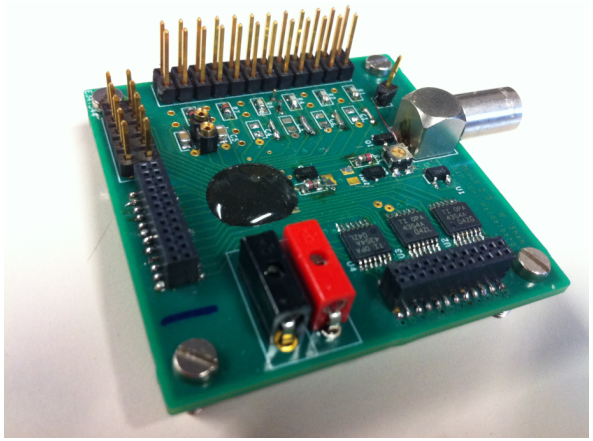

Michael Kolpin, Bachelor-thesis, KPI Heidelberg

# Integrated electronics – KLauS 2v0

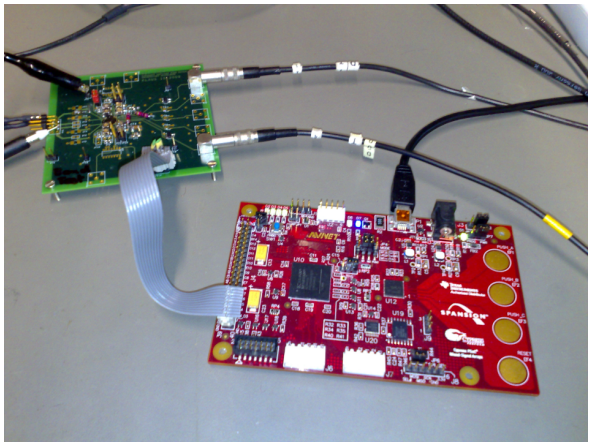
KLauS – Kanäle für Ladungsauslese von SiPMs

- KLauS 2v0 test board:
  - We have now two test boards at SMI
    (thanks to H.C. Schultz-Coulon, T. Harion, Wei Shen from KIP)



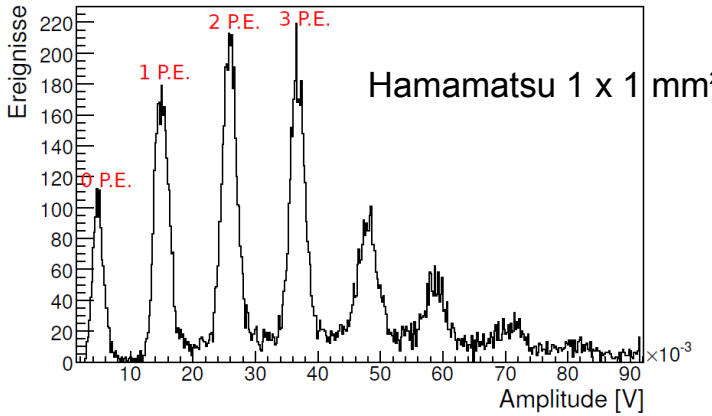
- The chip is configured via FPGA board

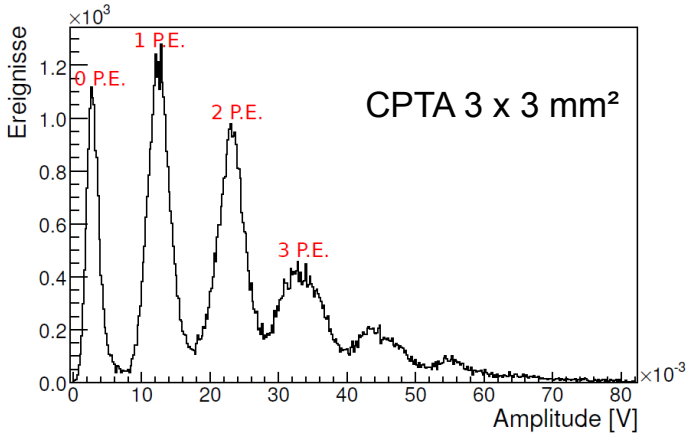


# Integrated electronics – KLauS v2.0

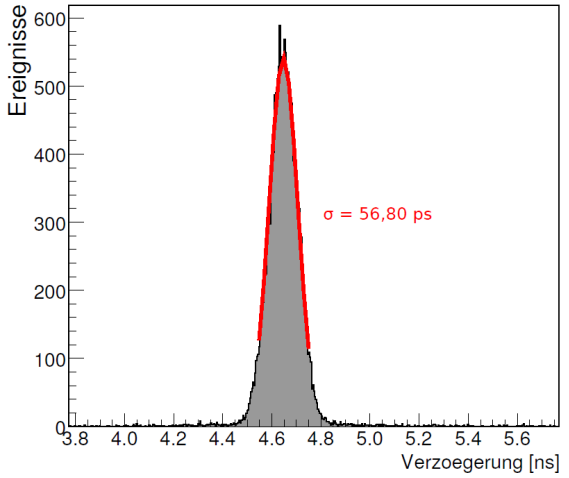
KLauS – Kanäle für Ladungsauslese von SiPMs

- Measurement setup:
  - Measurements done by KIP Heidelberg (Michael Kolpin, Bachelor-thesis)
  - Pulse generator + LED
- Single photon spectrum:



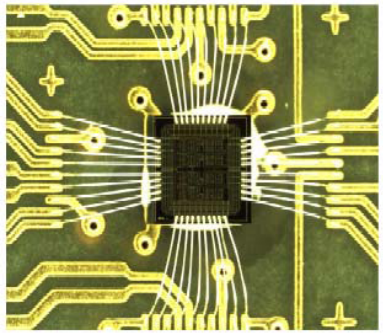




- Trigger jitter
  - Intrinsic jitter (pulse generator + board)

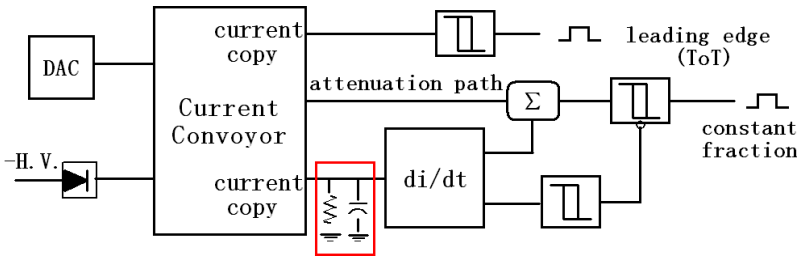


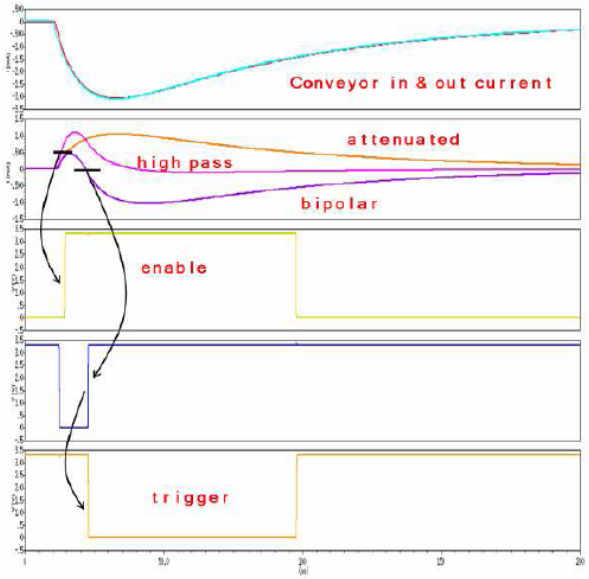
# Integrated electronics – STIC

## STIC – SiPM Timing Chip



- STIC:
  - Developed at KIP Heidelberg
  - Designed in AMS 0.35 µm CMOS technology
  - Dedicated to fast timing discrimination (TOF applications with SiPM, PET with SiPM)
  - 1st prototype with 4 channels
  - Each channel can be operated in leading edge (LE) or constant fraction (CF) triggering: time jitter ~ 60 ps
  - Charge integration and Time over Threshold (ToT) for energy measurement
  - DAC to tune the SiPM bias voltage, individual bias
  - Total power consumption < 10 mW per channel



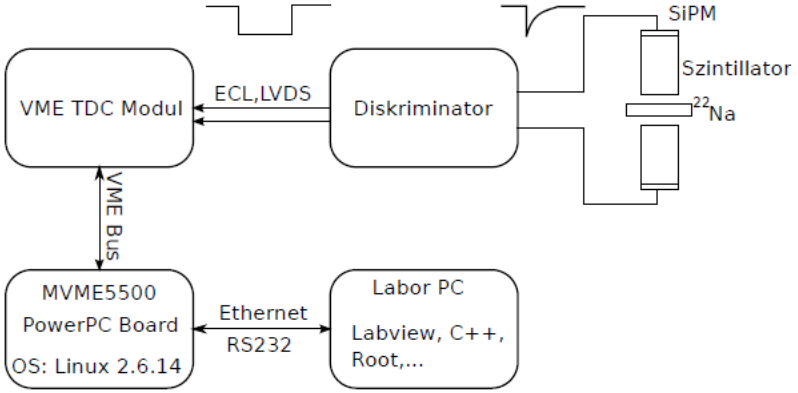




Tobias Harion, Diploma-thesis, KPI Heidelberg

# Integrated electronics – STIC

## STIC – SiPM Timing Chip

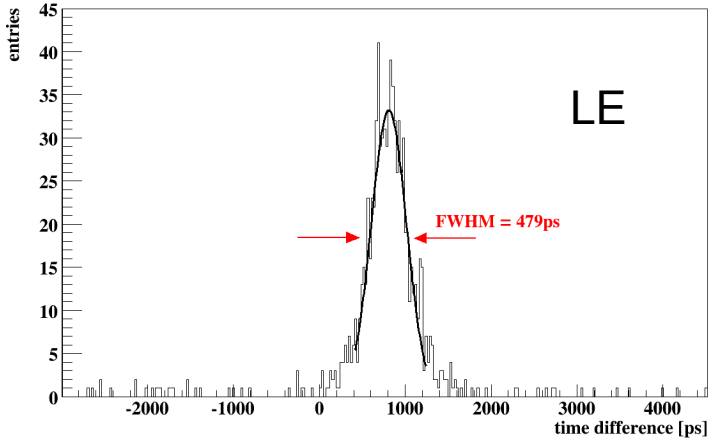
- Measurement setup:
  - Measurements done by KIP Heidelberg
  - $^{22}$Na source
  - LFS crystal
  - Hamamatsu 3 x 3 mm²

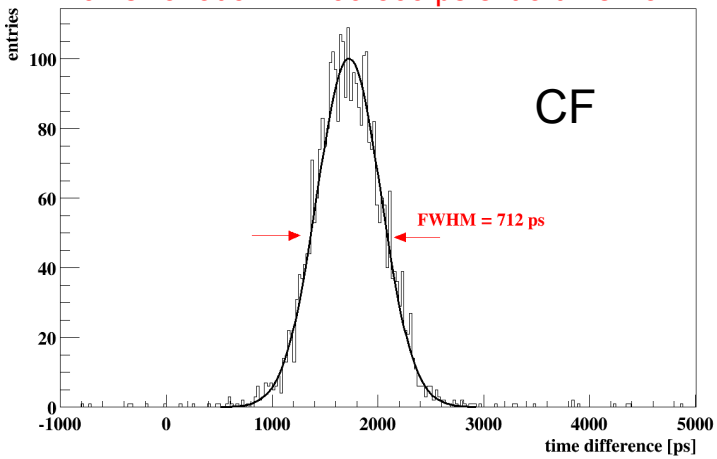



2010 IEEE, 10.1109/NSSMIC.2010.5873790

- Coincidence time resolution:

peaking time variation not considered
10 ns variation → 400-500 ps extra time walk



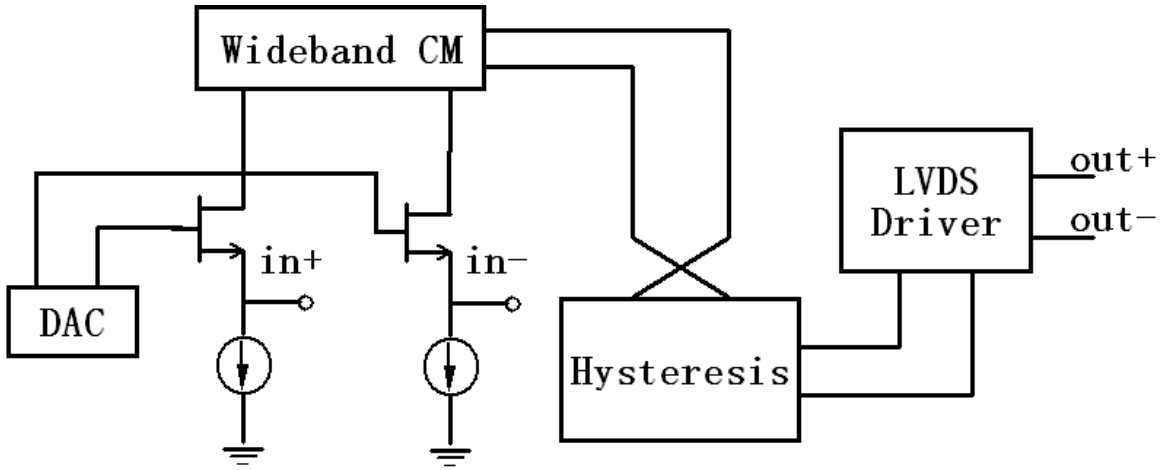




- Energy resolution:
  - 11% energy resolution using the charge integration method
  - 20% energy resolution using ToT (Time over Threshold) method

# Integrated electronics – STIC 2.0

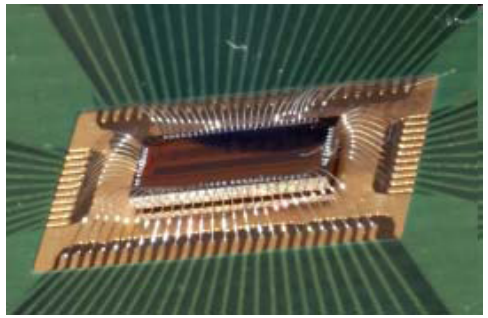
STIC – SiPM Timing Chip

- STIC 2.0:
  - UMC 180 nm CMOS technology
  - Lower threshold triggering (reduce rise time effect)
  - Higher transfer bandwidth of the conveyor stage
  - Differential readout scheme
  - Available beginning of next year → we will get a test board from KIP

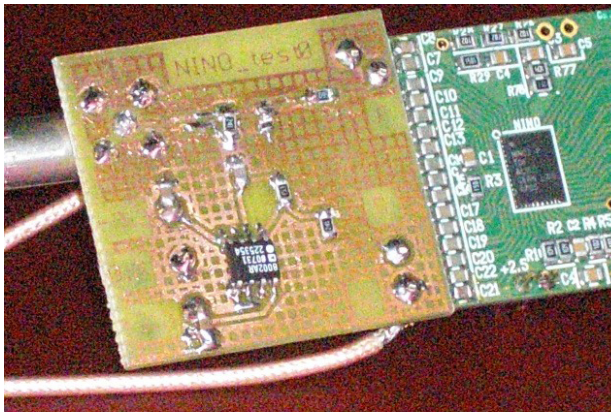


# Integrated electronics – NINO

An ultrafast front-end preamplifier-discriminator chip

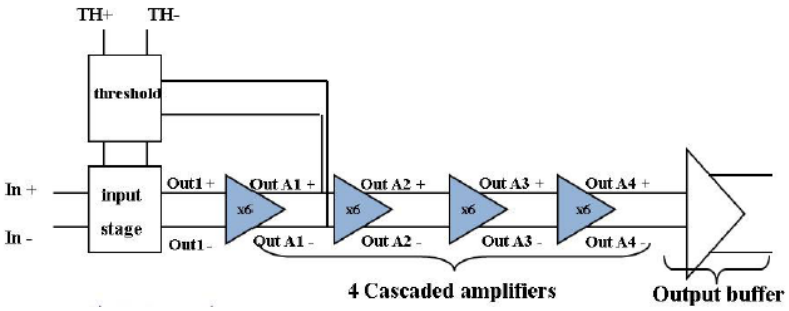


- NINO:
  - IBM 0.25 µm CMOS technology
  - Time-of-flight measurements in the ALICE experiment
  - Differential readout
  - 8 channels
  - We have a NINO test board at the institute (thanks to C. Schwarz)



NINO Chip Specifications

| Parameter | Value |
|---|---|
| Peaking time | 1ns |
| Signal range | 100fC-2pC |
| Noise (with detector) | < 5000 e- rms |
| Front edge time jitter | < 25ps rms |
| Power consumption | 30 mW/ch |
| Discriminator threshold | 10fC to 100fC |
| Differential Input impedance | 40Ω< Zin < 75Ω |
| Output interface | LVDS |

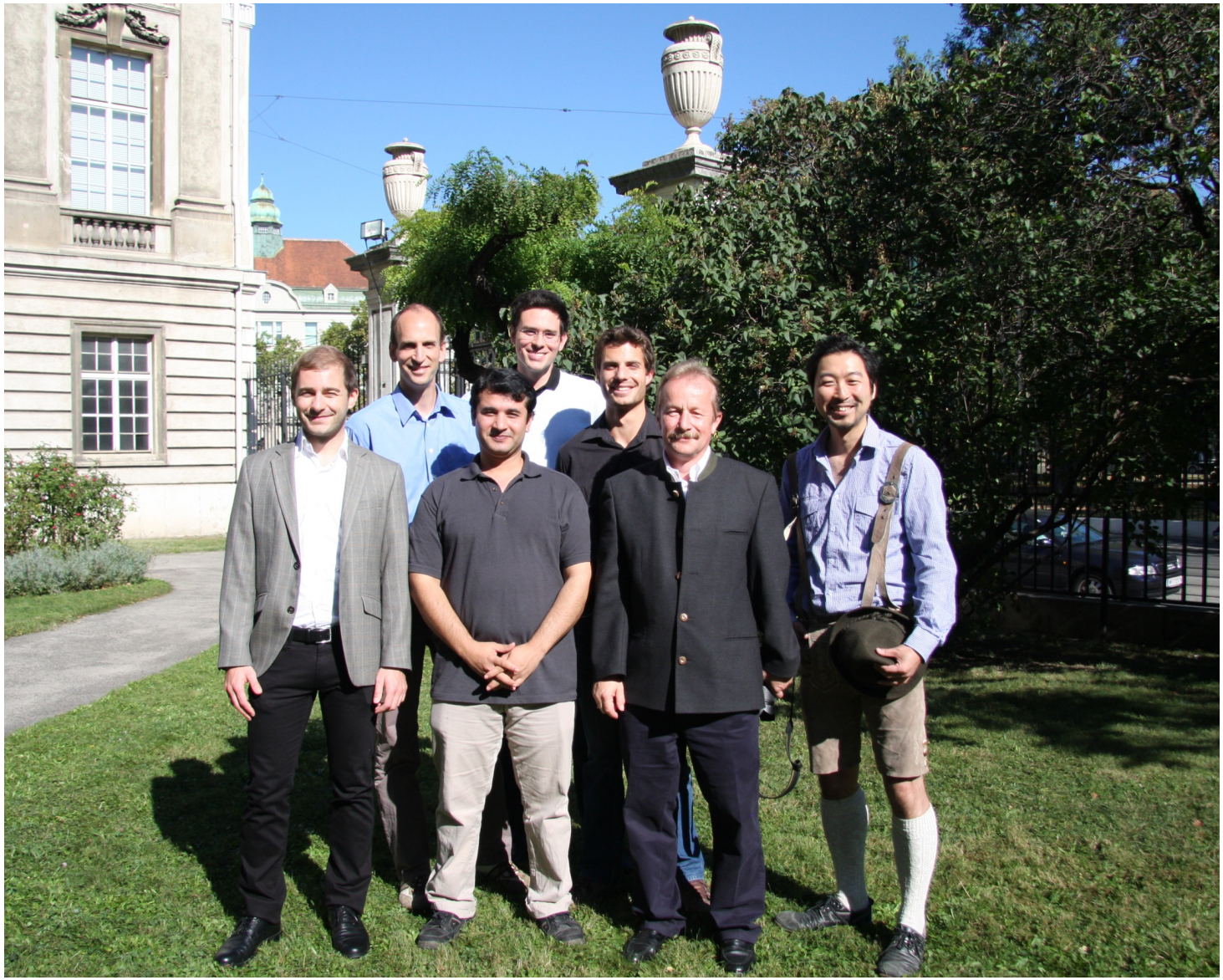


# Summary

- Measurements with the 64 channel SiPM array are ongoing. We plan to do more laser tests with different incident angles and smaller laser spots.
- More detailed simulations of the light concentrator performance will be carried out in order to get a better understanding of the measurements.
- We will investigate several ASICs (KLauS, STIC, NINO,…) for the readout of SiPMs in order to reduce the size of the SiPM module and achieve a better performance. Temperature controlling is a crucial point. Also other projects will benefit from this investigation.
- We plan to do systematic measurements of the recovery time for different SiPMs.
- We want to study the benefit of using SiPMs for TOF-PET using measurement and simulation.

Thanks to Hans-Christian Schultz-Coulon, Wei Shen and Tobias Harion
from KIP Heidelberg and Carsten Schwarz from GSI.

# SiPM group



Stefan Meyer Institute