FEE-free FADC readout for the STT

Henner Ohm *(Forschungszentrum Jülich, IKP)*
Krzysztof Pysz *(IFJ PAN Kraków / Forschungszentrum Jülich, IKP)*
Susanna Costanza *(INFN Pavia)*
Andreas Erven *(Forschungszentrum Jülich, ZEA)*
Wilhelm Erven *(Forschungszentrum Jülich, ZEA)*
Tanja Hahnraths - von der Gracht *(Forschungszentrum Jülich, IKP)*
Lioubov Jokhovets *(Forschungszentrum Jülich, ZEA)*
Paweł Kulessa *(IFJ PAN Kraków / Forschungszentrum Jülich, IKP)*
Robert Nellen *(Forschungszentrum Jülich, IKP)*
James Ritman *(Forschungszentrum Jülich, IKP)*
Valery Serdyuk *(Forschungszentrum Jülich, IKP)*
Peter Wintz *(Forschungszentrum Jülich, IKP)*
Bogusław Włoch *(IFJ PAN Kraków / AGH Kraków)*

Two optional STT readout

Two options of PANDA STT readout:

1. ASIC – specialized, programmable chip allowing for tail cancellation and baseline restoration:
   - time information (digital) (+ Time over Threshold → energy)
   - energy information (analog)

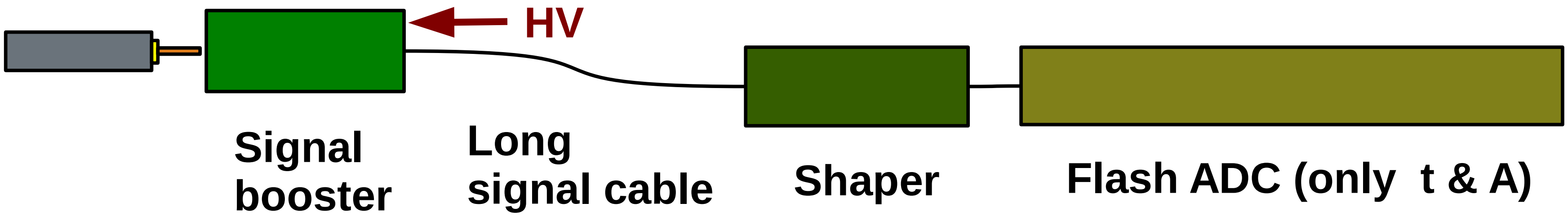
AGH University + Jagellonian University Kraków (Poland)

2. Signal booster + Shaper + FPGA-FlashADC; fixed optimal integration time, tail cancellation, baseline restoration:
   - time information (from FPGA discriminators)
   - energy information (from FPGA amplitude search procedure)

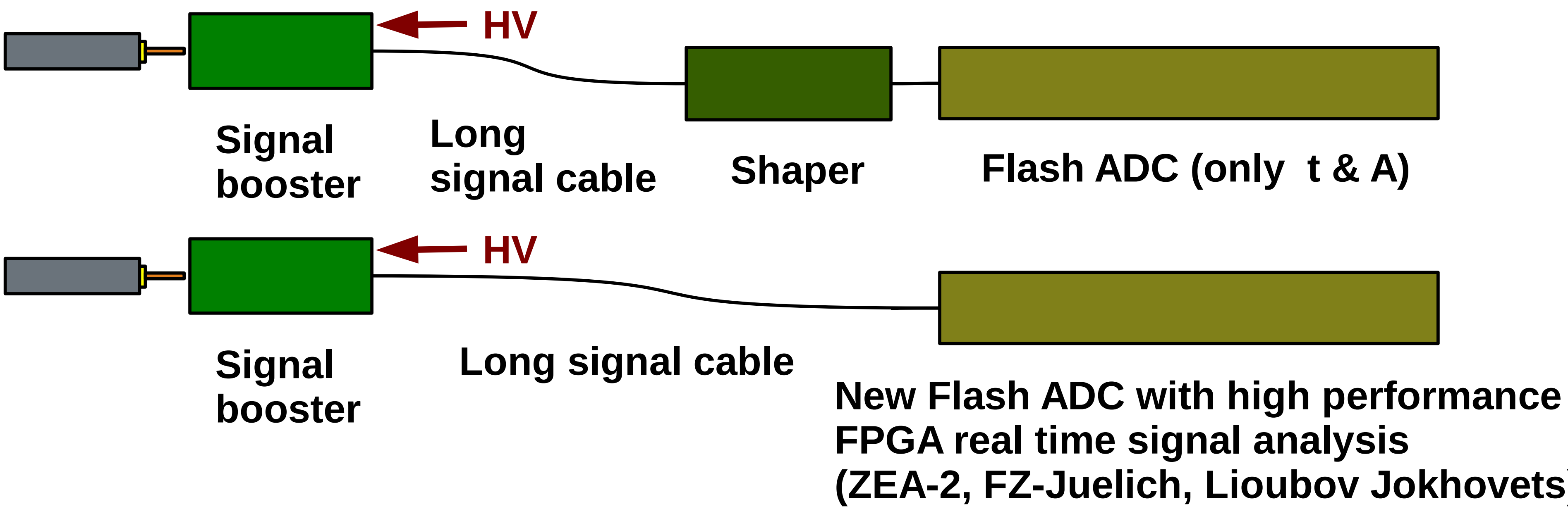
FZ Juelich (Germany) + INP PAN Kraków (Poland)

With option 2 the simultaneous measurements of track position as well as the energy loss with the demanded precision was obtained !

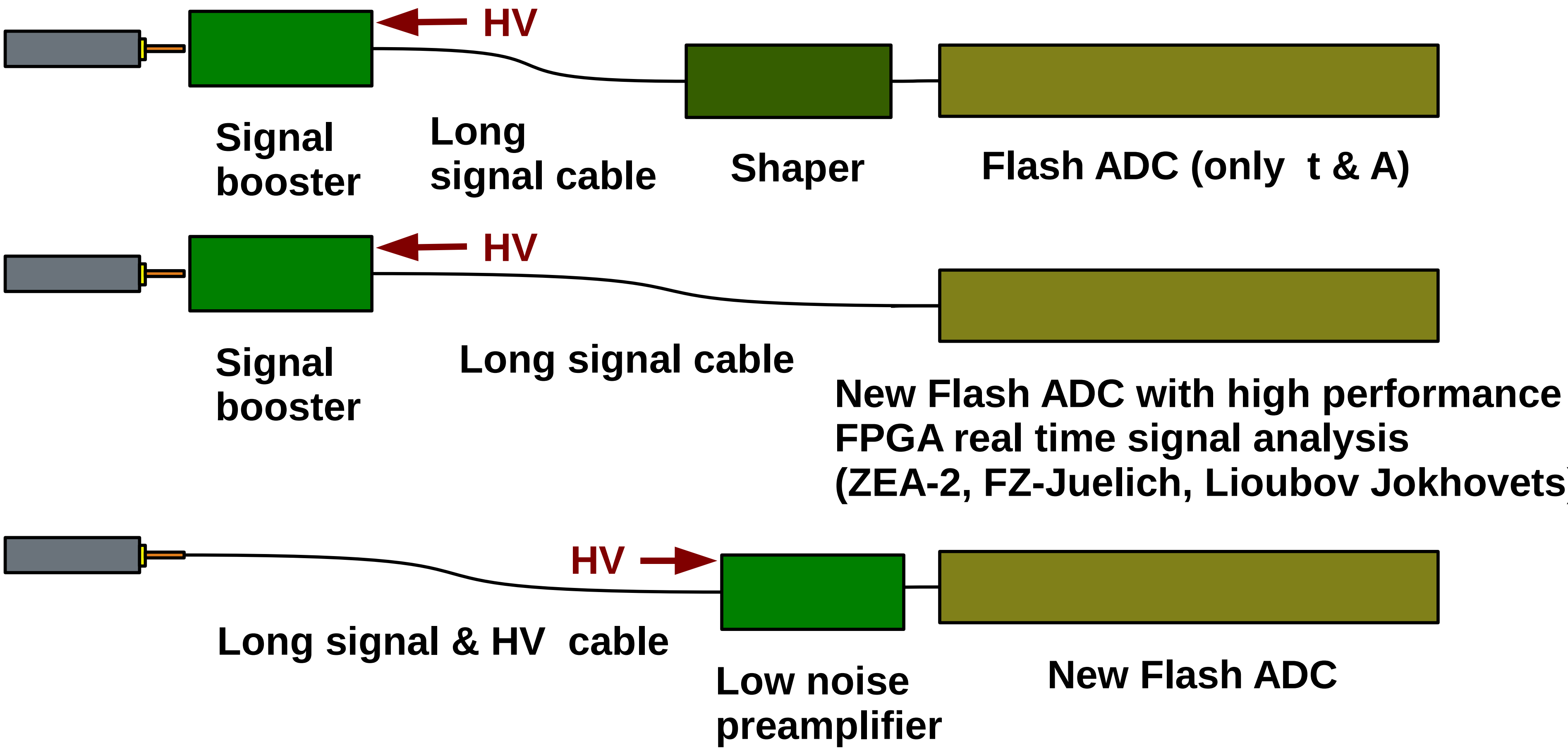
Evolution of OPTION 2



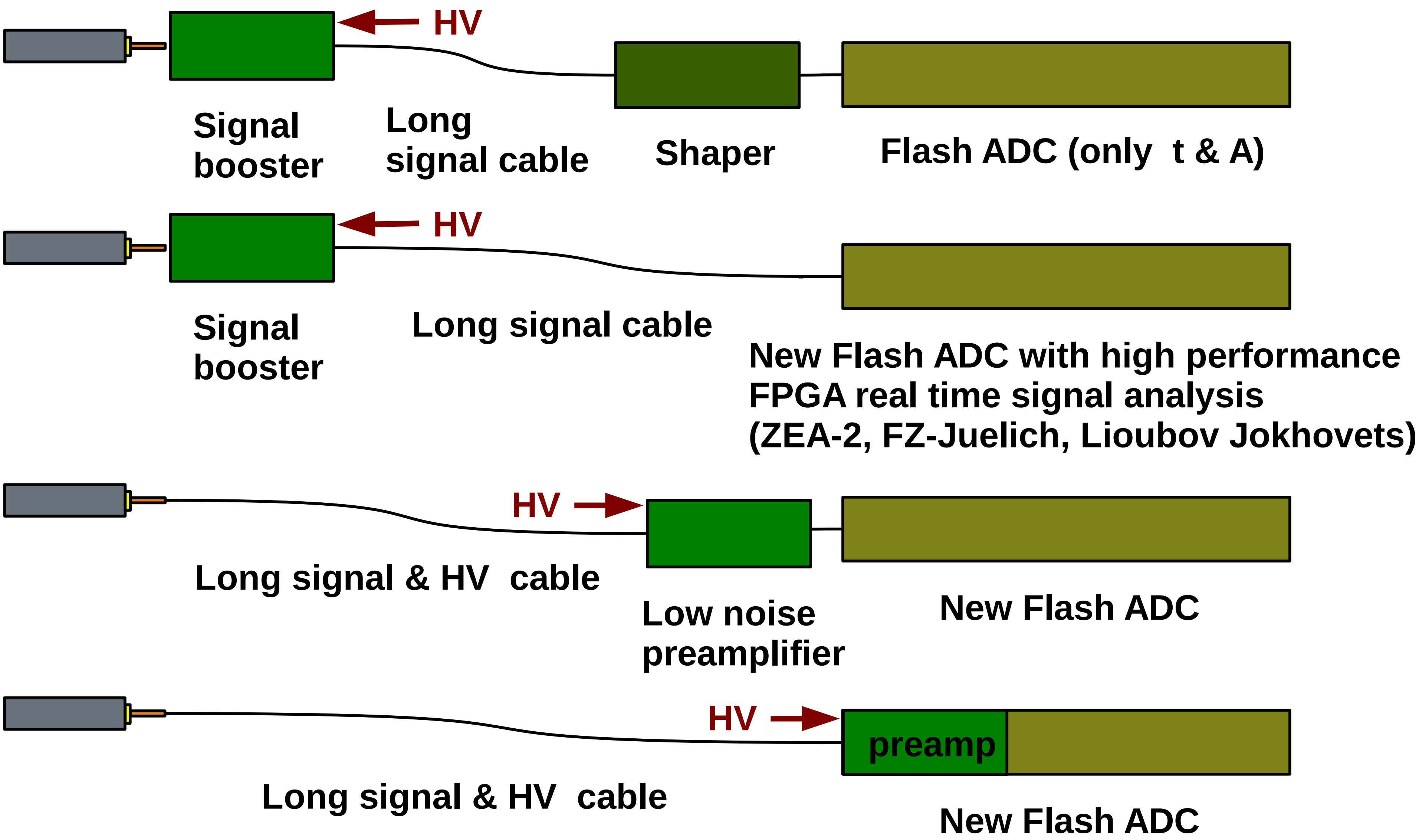
Evolution of OPTION 2



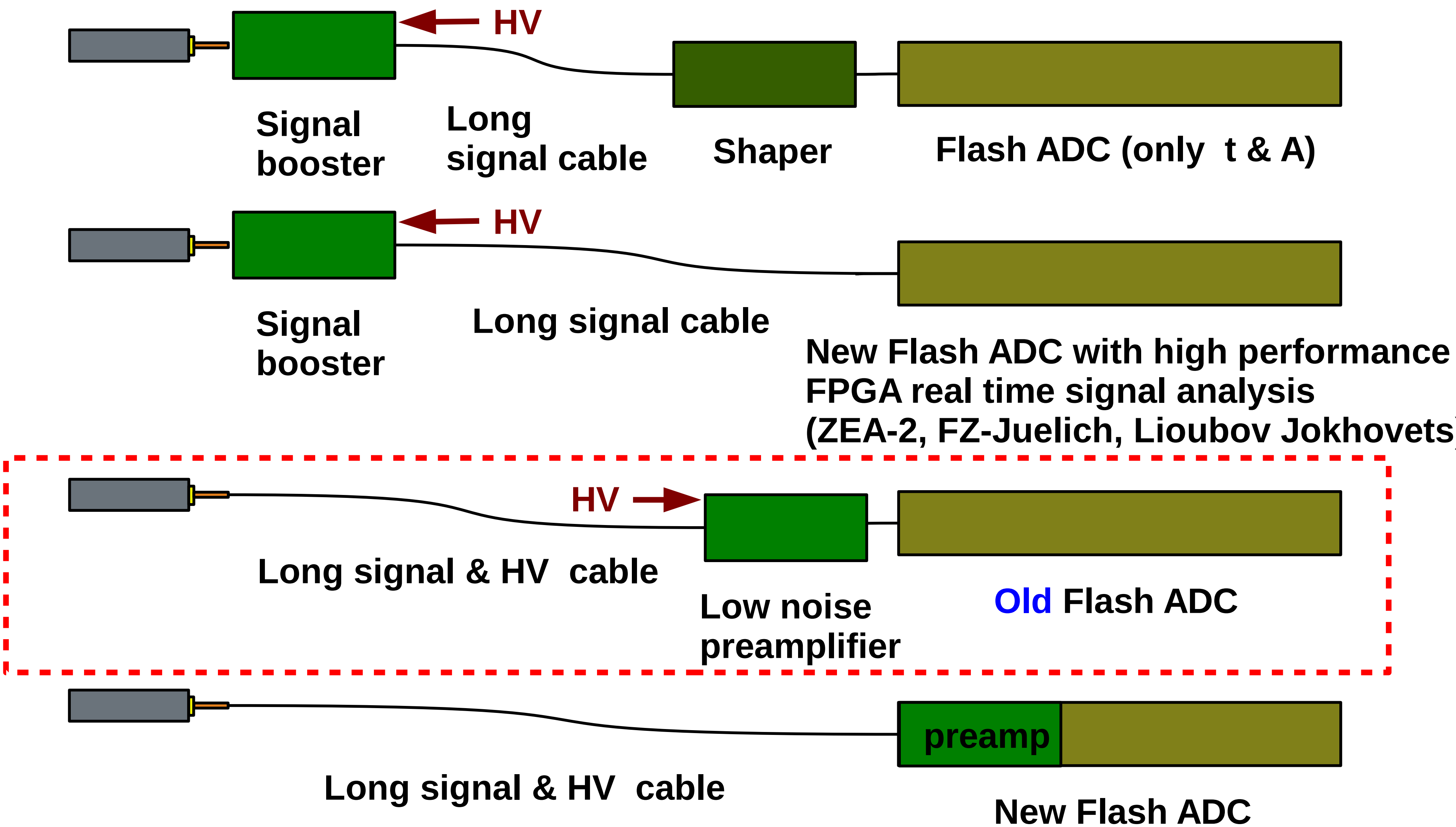
Evolution of OPTION 2



Evolution of OPTION 2



Evolution of OPTION 2



Challenges

Energy loss measurement → robust method, proper signal integration and data truncation needed.

dE/dx resolution → confirmed – but depends on tracking precision

Track position measurement → delicate, depends strongly on signal quality

- onset of the signal on the first clusters → reasonably short integration time;
- sufficient number of samples on the rising edge → reasonably long integration time;
- low curvature of the rising edge (for determination of “Zero Crossing Time”);
- low noise level;
- precise method for signal time definition (ZCT, CFD, LED, …);
- influence of long signal cables (signal dumping, noise pickup, ...) .

Preamplifier performance has to be optimized for above requirements

Preamplifier TIA04

Three amplification stages:

1. Broad bandwidth transimpedance amplifier of the low noise

2. Broad bandwidth voltage amplifier

3. Integrating amplifier

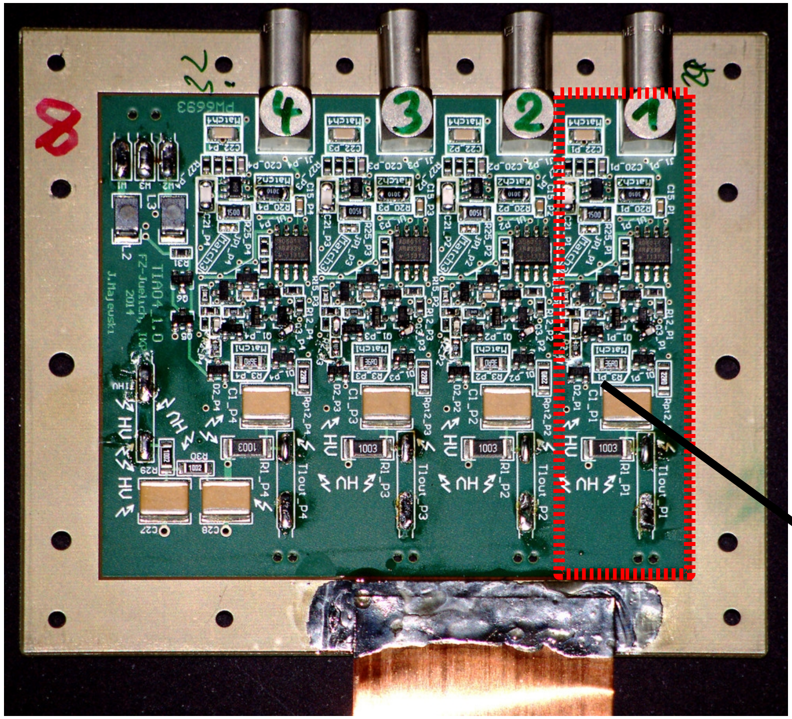
First stage is build with the use of bipolar transistors → low noise level of this stage

Integration only in one stage → low curvature of rising edge of the signals

Integration in the last stage → further reduction of noise

Preamplifier

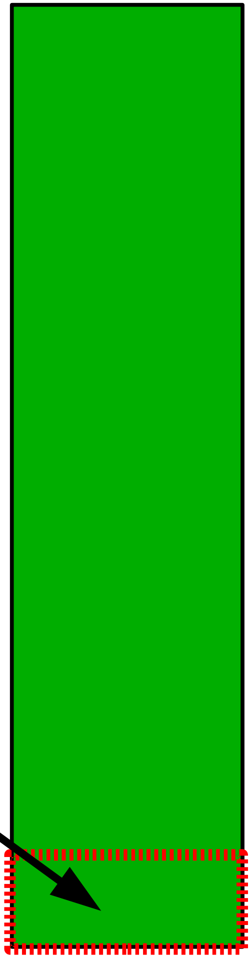
output



input

4-channel TIA04 board used in July experiment

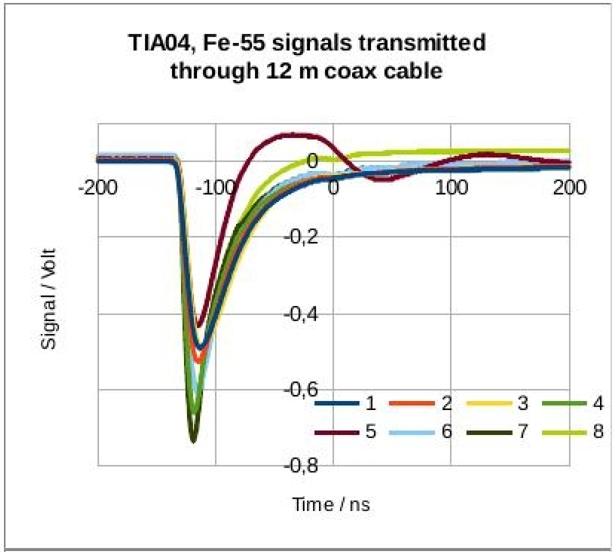
New FlashADC

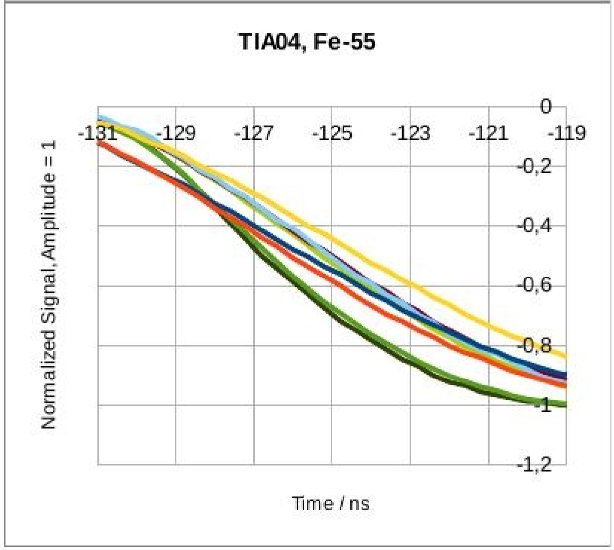


Parameter optimization

Tab. 2: Pulse risetimes (from 10% to 90% of the amplitude), signals amplitudes and noise voltages of TIA04 for pulse-generator signals or Fe-55. The electronical time resolution was estimated as $\sigma_{time} = \sigma_{rms} / (dV/dt)$. For simplicity the signal slope was taken as dV/dt = amplitude/risetime.

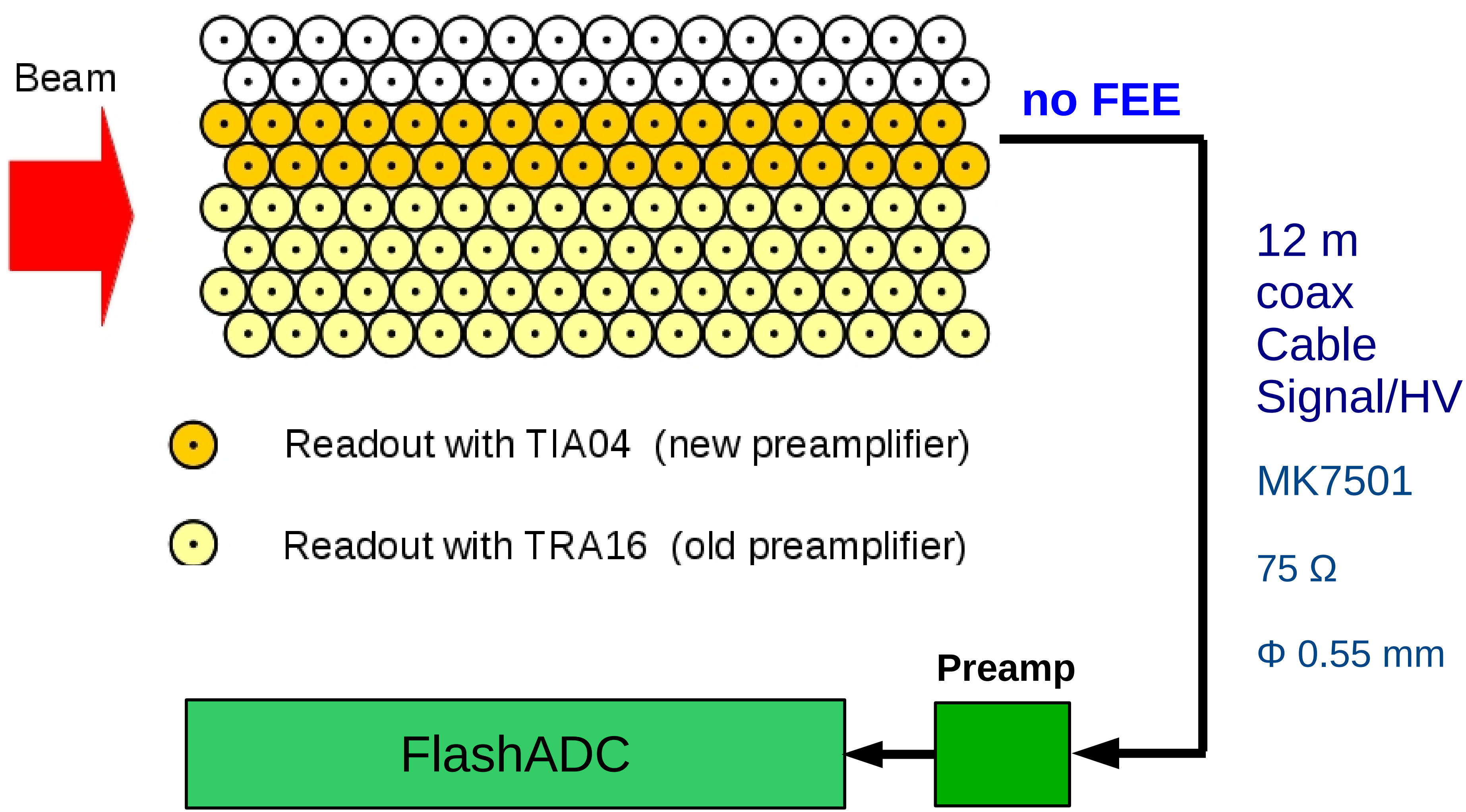
Ch. No.	10% - 90% Rise Time			Signal ampl.	RMS Noise	Time Resolution Estimate	Comments
	Generator		Fe-55			Fe-55	
	direct	via 12 m cable					
	ns	ns	ns	mV	mV	ps	
1	6,3	10.5	12,5	492	1.14	29	
2	5,5	9.4	11,3	532	1.13	24	
3	6,2	10.2	12,5	496	1.07	27	
4	4,3	6.4 ?	8,2	658	1.35	17	
5	5,7	8.6	11,1	432	1.01	26	Signal overshoot when 12 m cable is used; oscillates occasionally with ~ 20 MHz
6	**5,0**	**8.5**	**10,4**	**624**	**1.20**	**20**	
7	4,0	6.2	7,9	752	1.49	16	Oscillations on the trailing edge
8	5,2	8.9	11,1	596	1.22	23	Signal overshoot



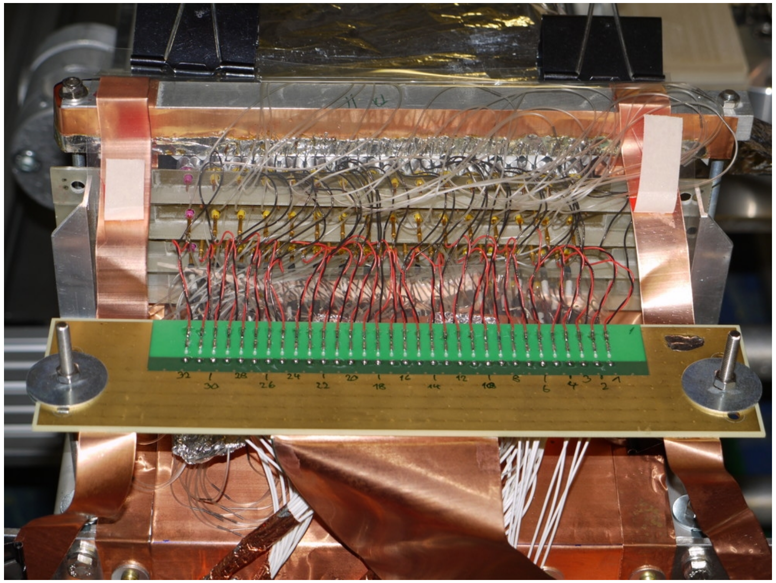


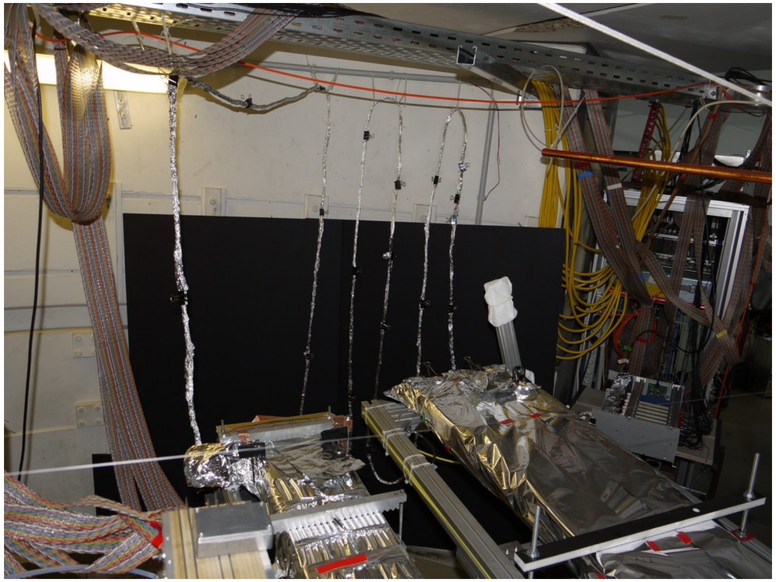
Henner Ohm's tests (parameter selection, long cables influence) → presentation in December CM

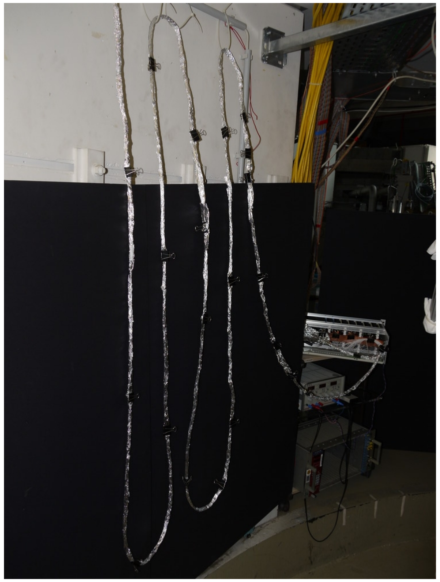
July beamtime

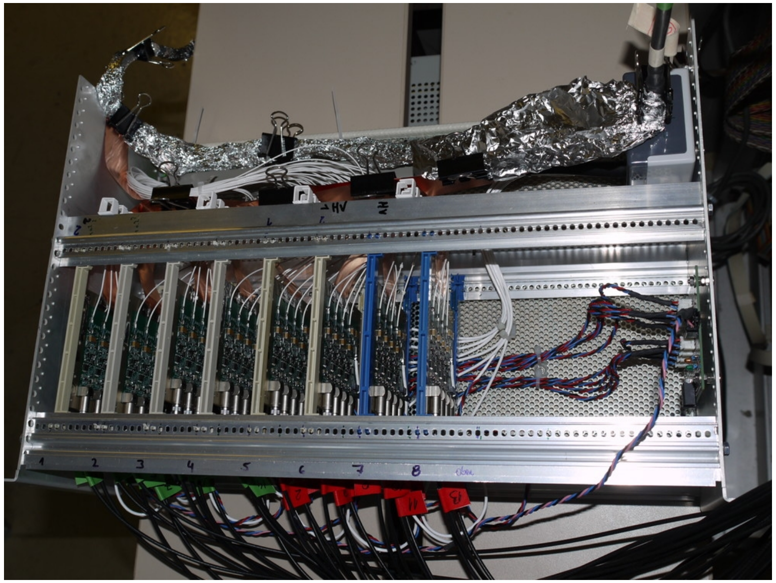


Setup

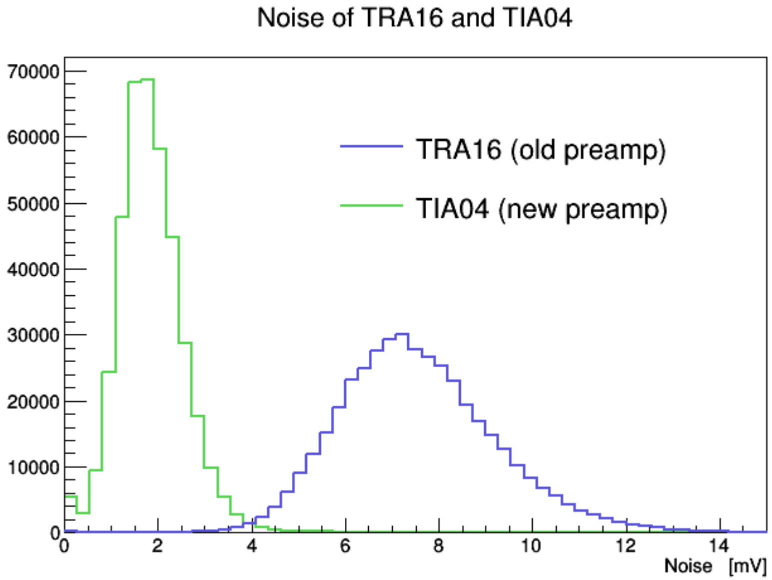


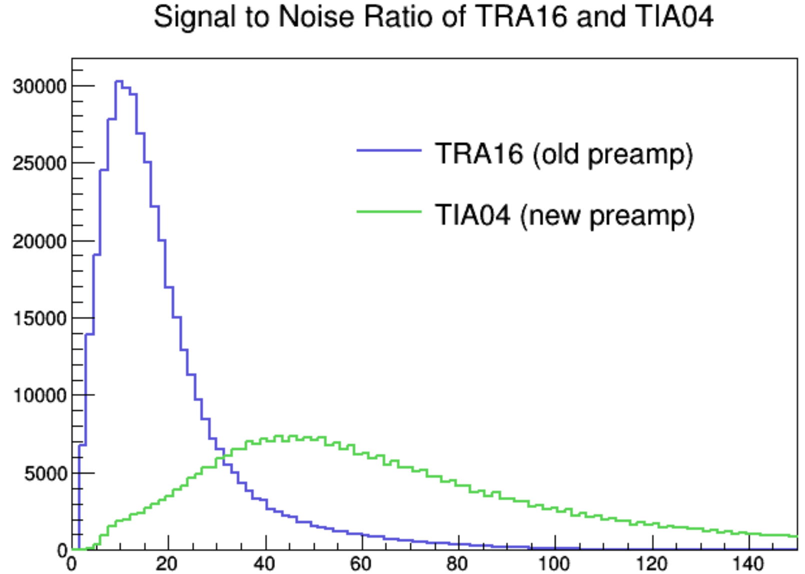




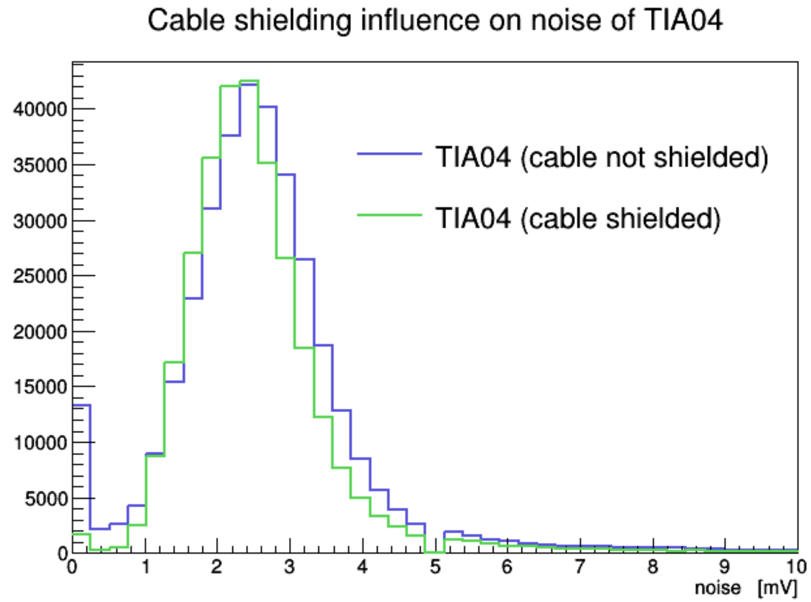


Noise performance of TIA





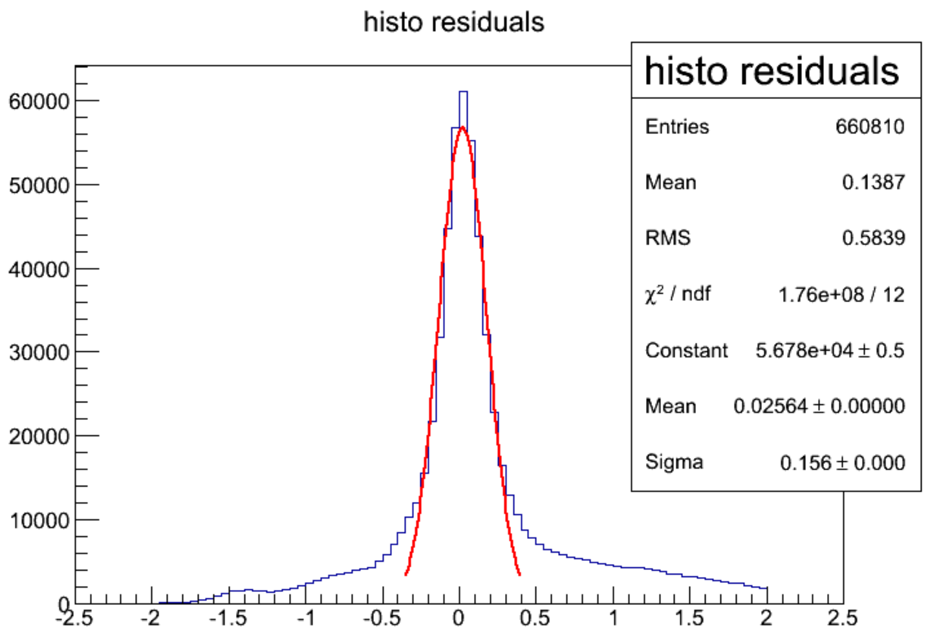
No noise pickup by the long cables during the beamtime



Preliminary Results

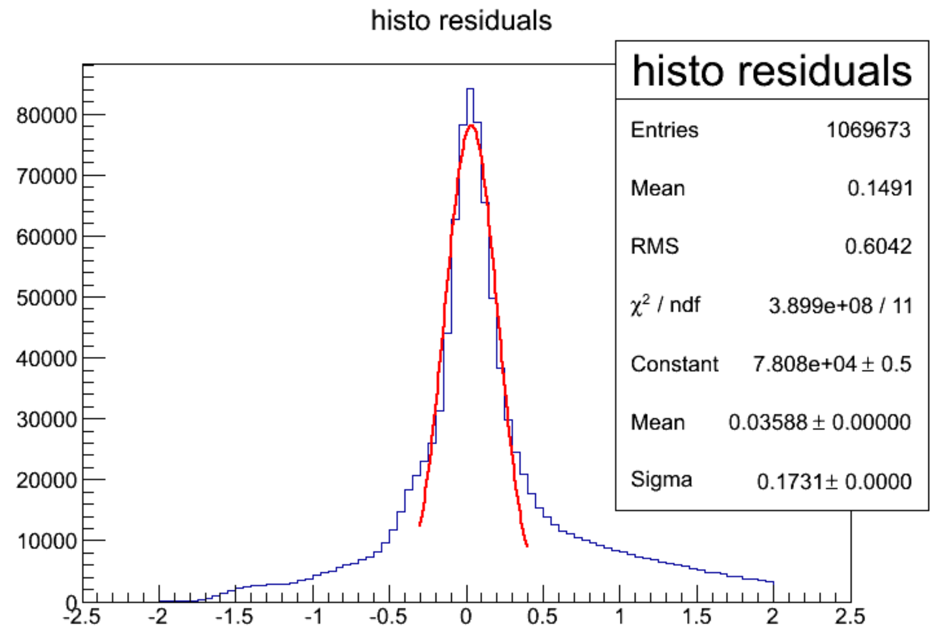
Position resolution derived from simplified tracking

3.0 GeV, one layer (no 5)



~150 µm

0.6 GeV, one layer (no 5)

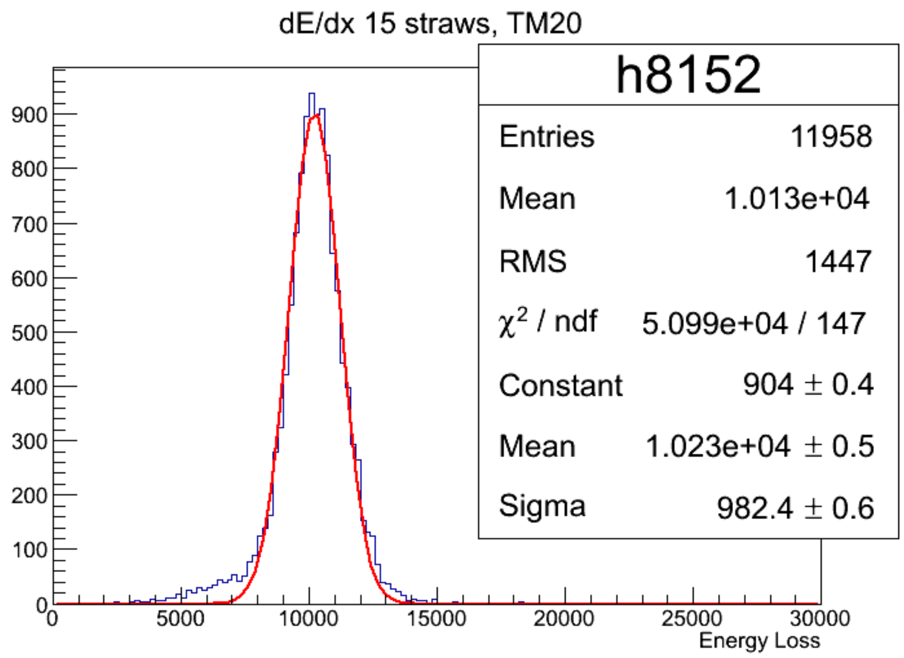


~170 µm

Preliminary Results

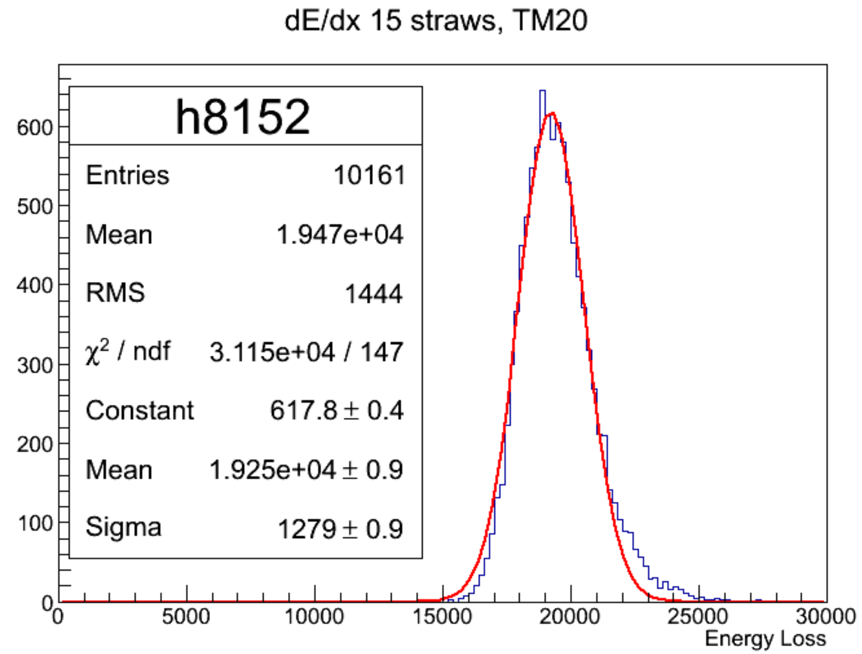
Energy resolution

3.0 GeV



9.6 %

0.6 GeV



6.7 %

Summary & Outlook

Prototype of analog preamplifier suitable for STT readout with the use of long signal/HV cables has been designed and constructed.

The design of the preamplifier is ready for incorporation into new FlashADC as as input stage.

The laboratory tests for parameter optimization were done.

The first beam test with readout of 32 channels of STT prototype with new preamplifier and 12 m long cables in between was performed.

The preliminary results are very promising.

Additional preamplifier board are under construction in order to readout 6 layers of STT prototype (96 channels) during October beamtime.

Thank you !