

# - SADC development for PANDA



**2008**

16-ch, 12-bit  
160 MSPS ADC  
Used for the  
first tests, sold  
to WIENER

**2010**

16-ch, 2Gbit/s  
Optical Data  
Concentrator  
Used in many  
experiments  
including  
WASA, KLOE2

**2011**

16-ch, 14-bit  
125 MSPS ADC  
Virtex-5  
Used for  
evaluation of  
DSP algorithms

**2012**

32-ch, Dual-  
range, 14-bit  
80 MSPS ADC  
Virtex-6  
Used for first  
data taking and  
durability tests

**2013**

64-ch, 14-bit  
80 MSPS ADC  
Kintex-7  
Close-to-final  
prototype

# - ADC\_64K, a close-to-final prototype



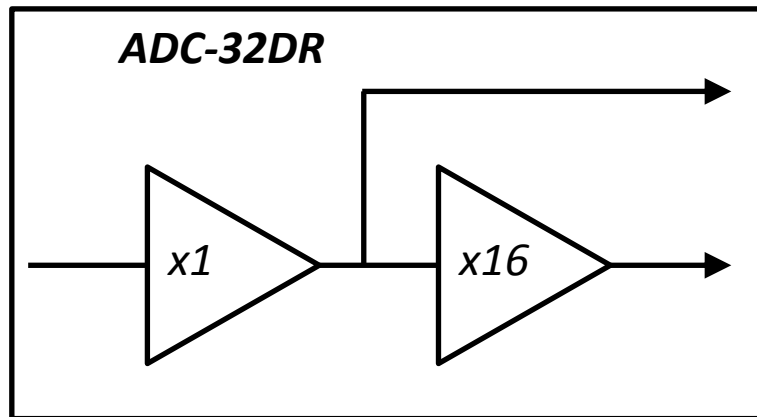
ADC Model	ADC_32DR	ADC_64V	ADC_64K
No. of channels	32 (64)	64	64
Sampling rate	80-125 MSPS		
Input coupling	DC, positive, negative, diff		
Resolution (ampl)	14-bit dual range	14-bit	
Input Connector	uFL	Samtec	
Baseline	0V		
Input range (dual)	±1.0V, ±100 mV		
Noise	100uV		
Data retention	32us	32us	32us
Input filter	Active-filter/Amplifier	CR-passive	Active filter/Amplifier
Interface	Optical, SFP, LC-type, 2 Gbit/s		
Feature extraction:	Signal search within window Partial integrals, Arrival times, Maxima, Minima, Baseline and noise		



# Issues to be addressed - Noise

With the PbWO4 + VPTT + Basel pre-amp the signal is ca. **100uV/MeV**

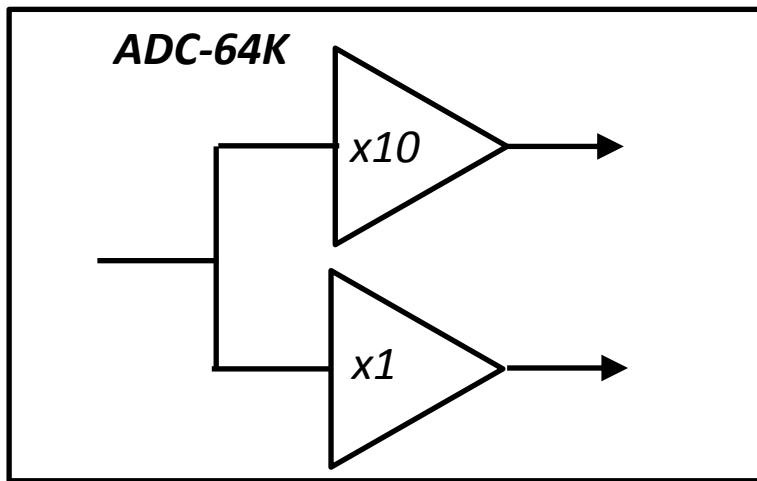
From the pre-amp



1Vpp → **750uV** noise  
(FWHM)

60mVpp → **150uV** noise  
(FWHM)

From the pre-amp

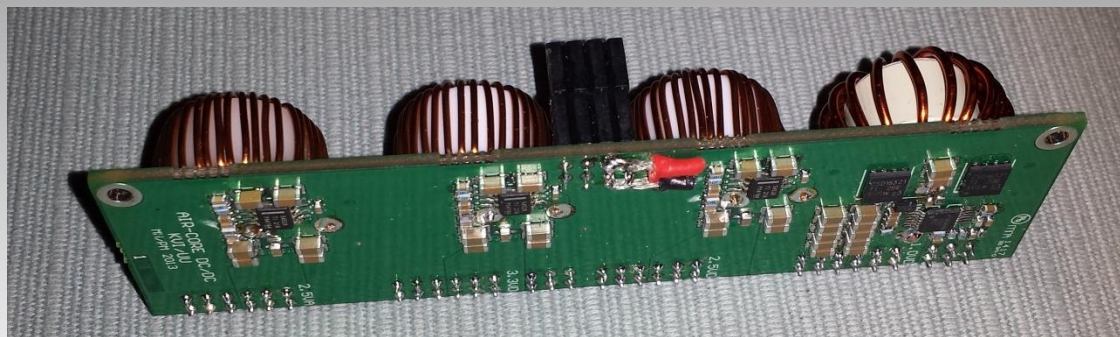
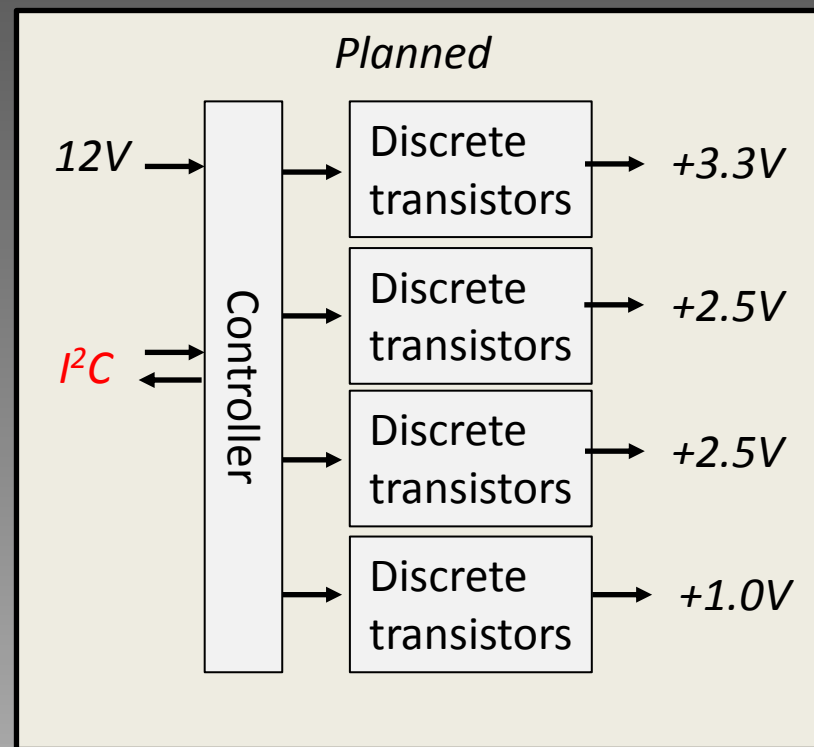
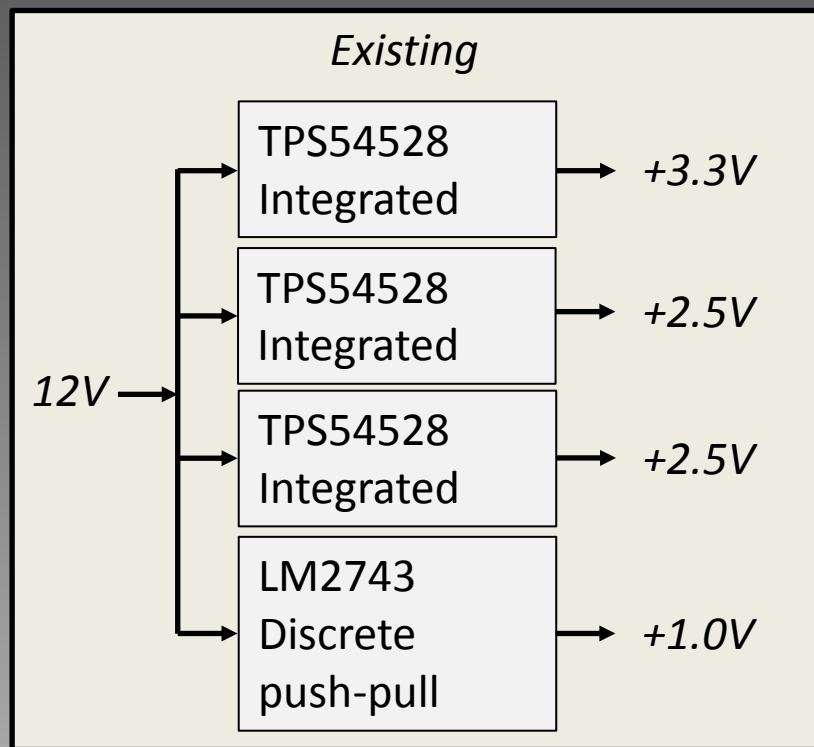


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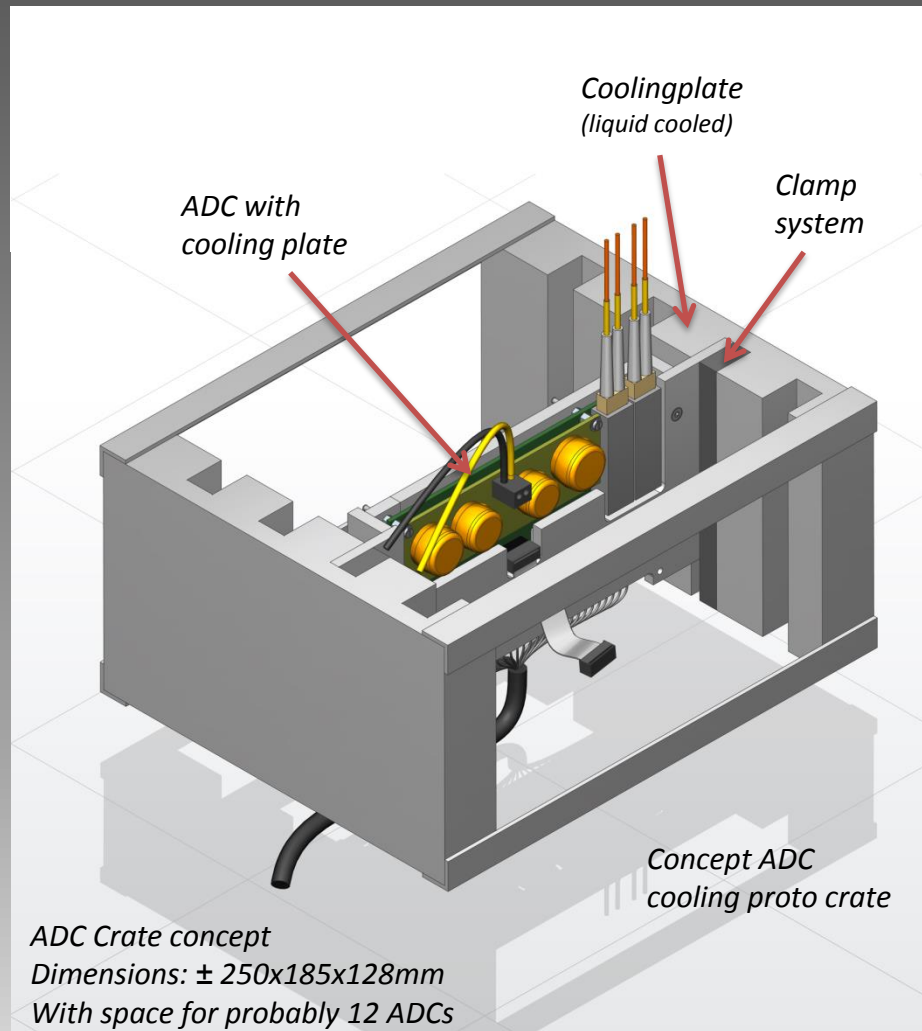
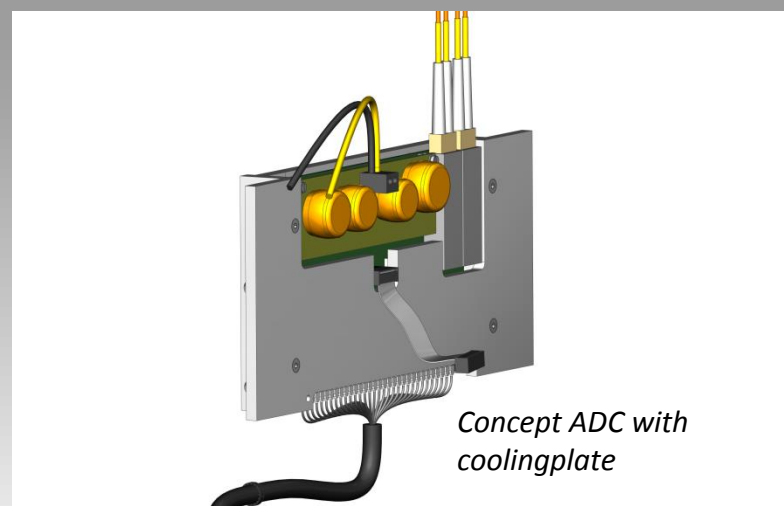
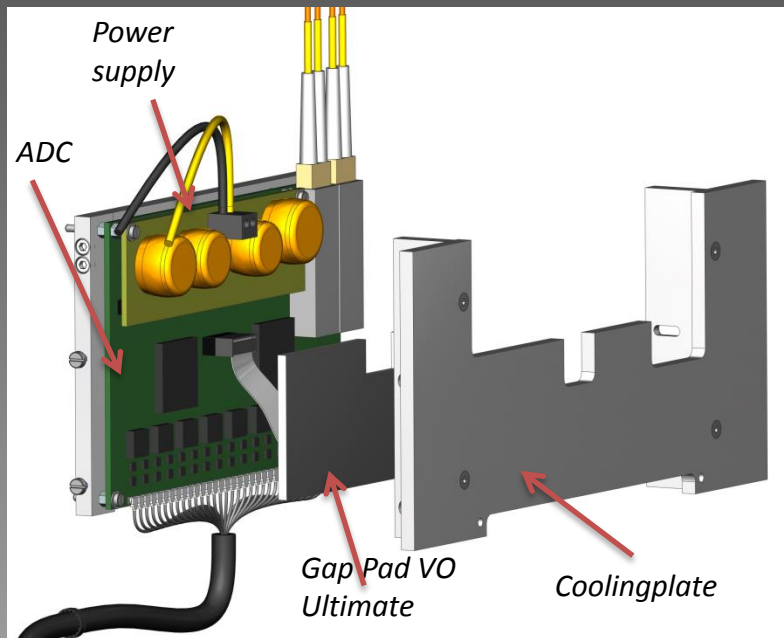


# Issues to be addressed - Powering/monitoring





# Issues to be addressed - Encapsulation and Cooling



Courtesy KVI

