Update of the PAnda STrip ASIC (PASTA)

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Design team:

Designers:

V. Dipietro, A.Riccardi (supported by Uni Giessen)-analog
A. Goerres – FZ Juelich – digital design

Technical Advisors:

A. Rivetti, M. Rolo

Key specs and architecture

Specifications

Input capacitance: 5 pF to 25 pF

Maximum rate per strip: 50 kHz

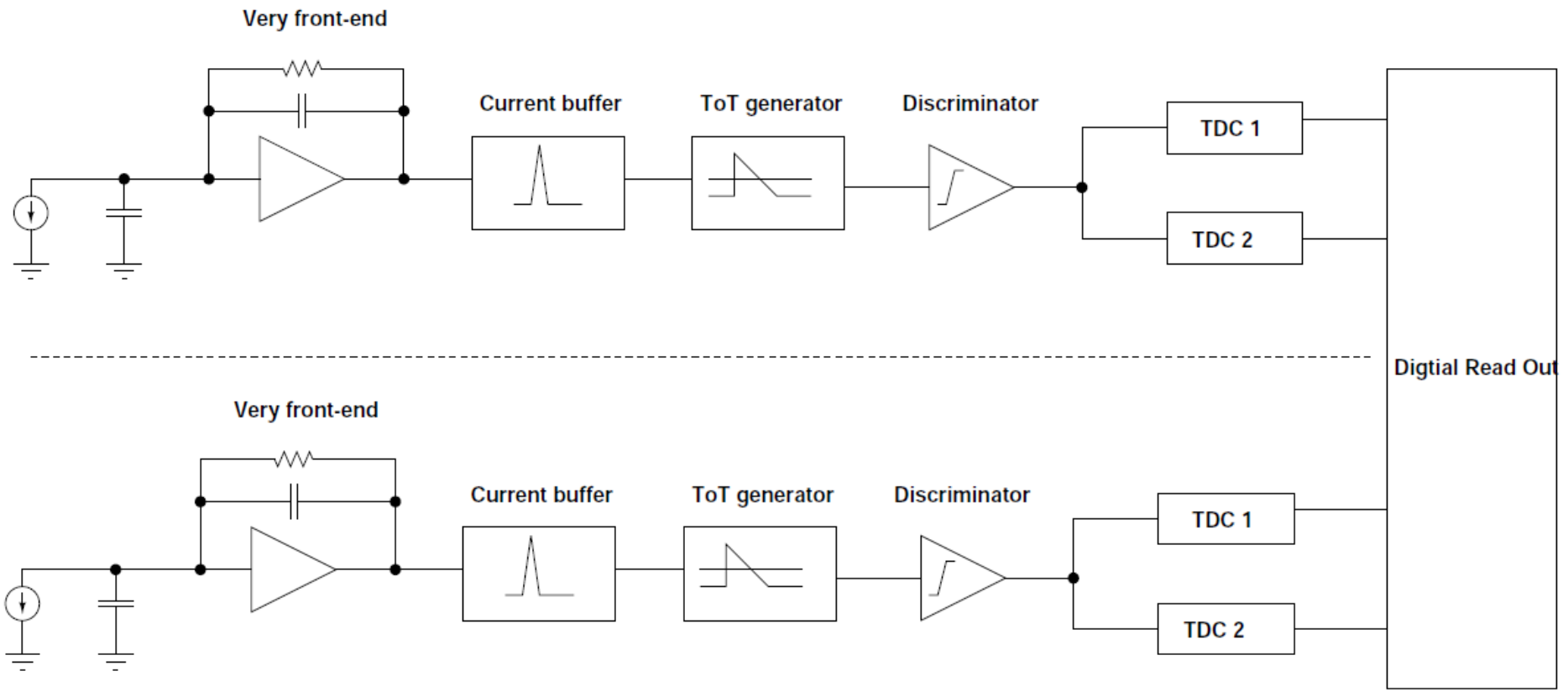
Power consumption < 4mW/ch

Channel per chip: 64

Chip size: 4.5 mm x 5 mm

Charge measurement: 40 fC

Architecture: Binary with fast ToT



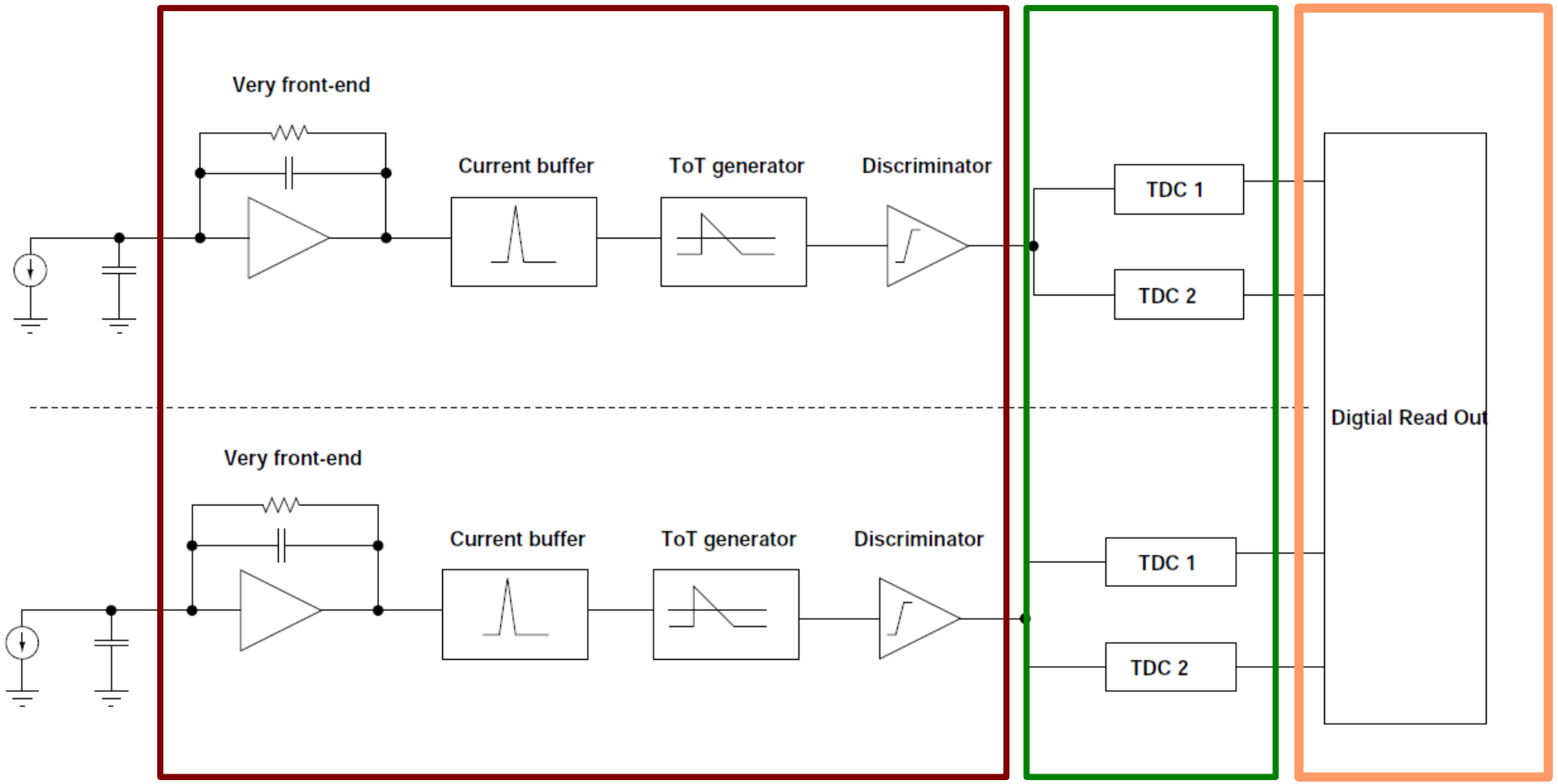
Project back-up

Architecture inspired by the TOFPET chip, but several upgrades necessary

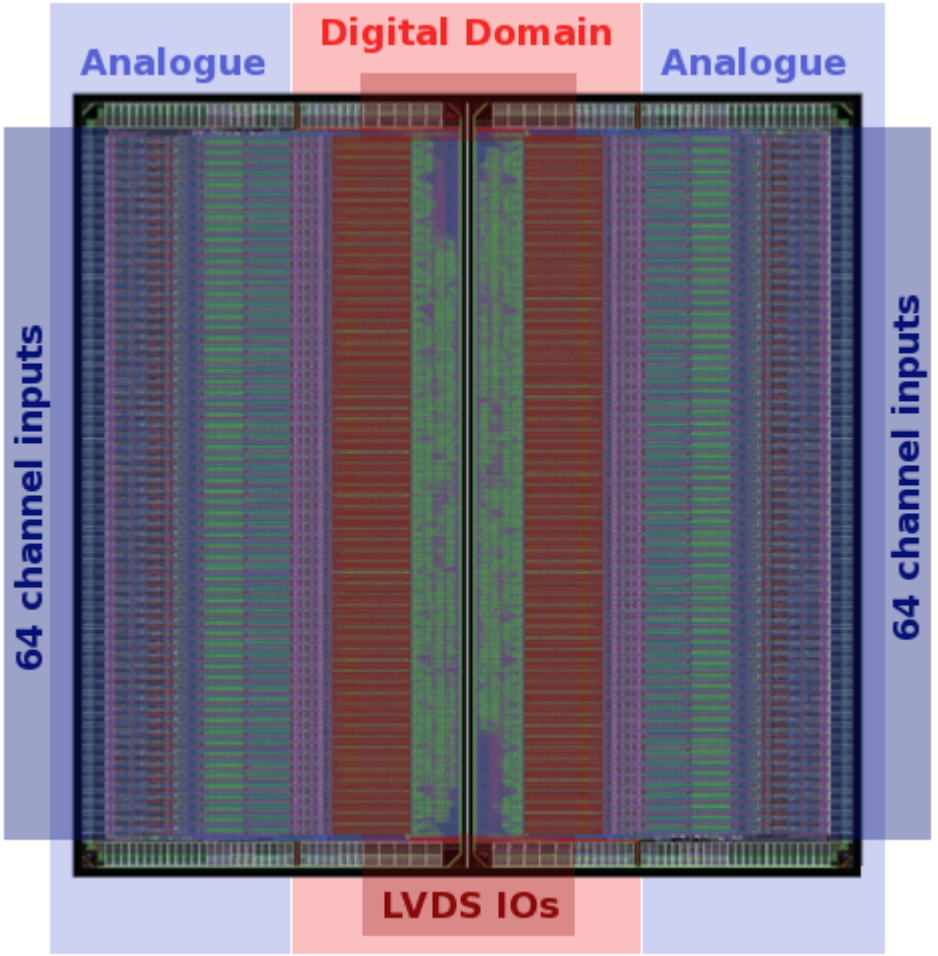
- **Building block upgrades**
  - TOFPET front-end designed for large signals (pC) and large capacitances (300 pF). Complete redesign of very front-end necessary
  - TDC basically OK
  - Digital logic functionally OK, but some “features” need to be fixed and SEU protection must be added
  - Optimize functionality for strip environment
- **Technology upgrades: from IBM 130 nm to UMC 110 nm**
  - Main implications: all the blocks need to be redesign from scratch
  - Global layout modifications also necessary

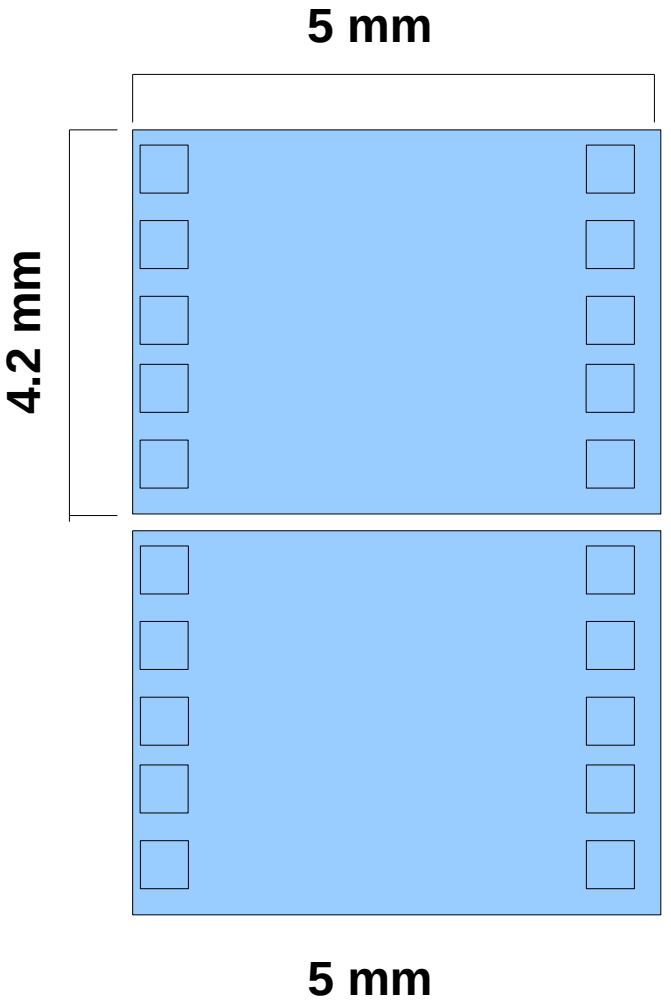
Key changes and updates

Designed from scratch, converted, updated

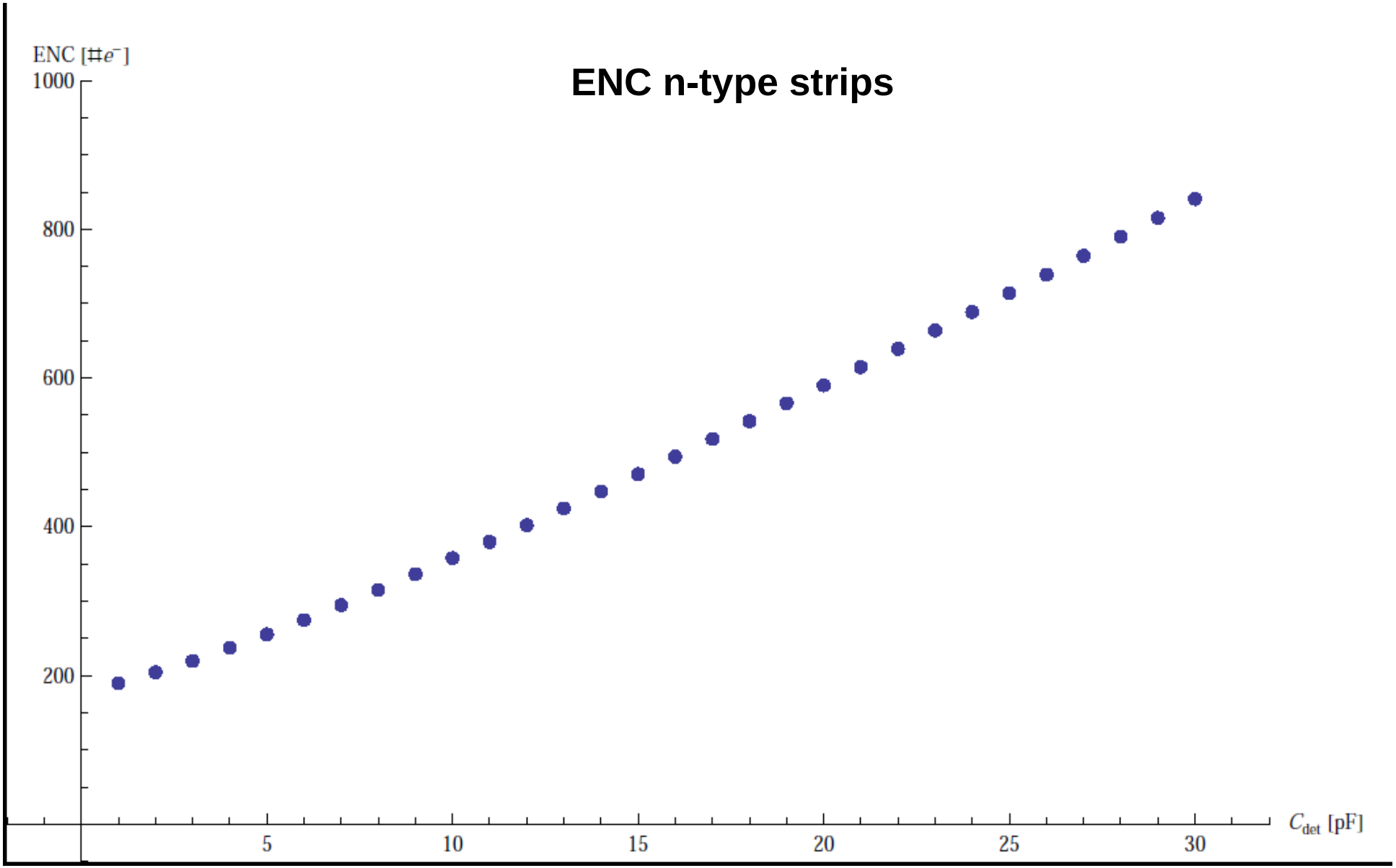


Important Top level changes





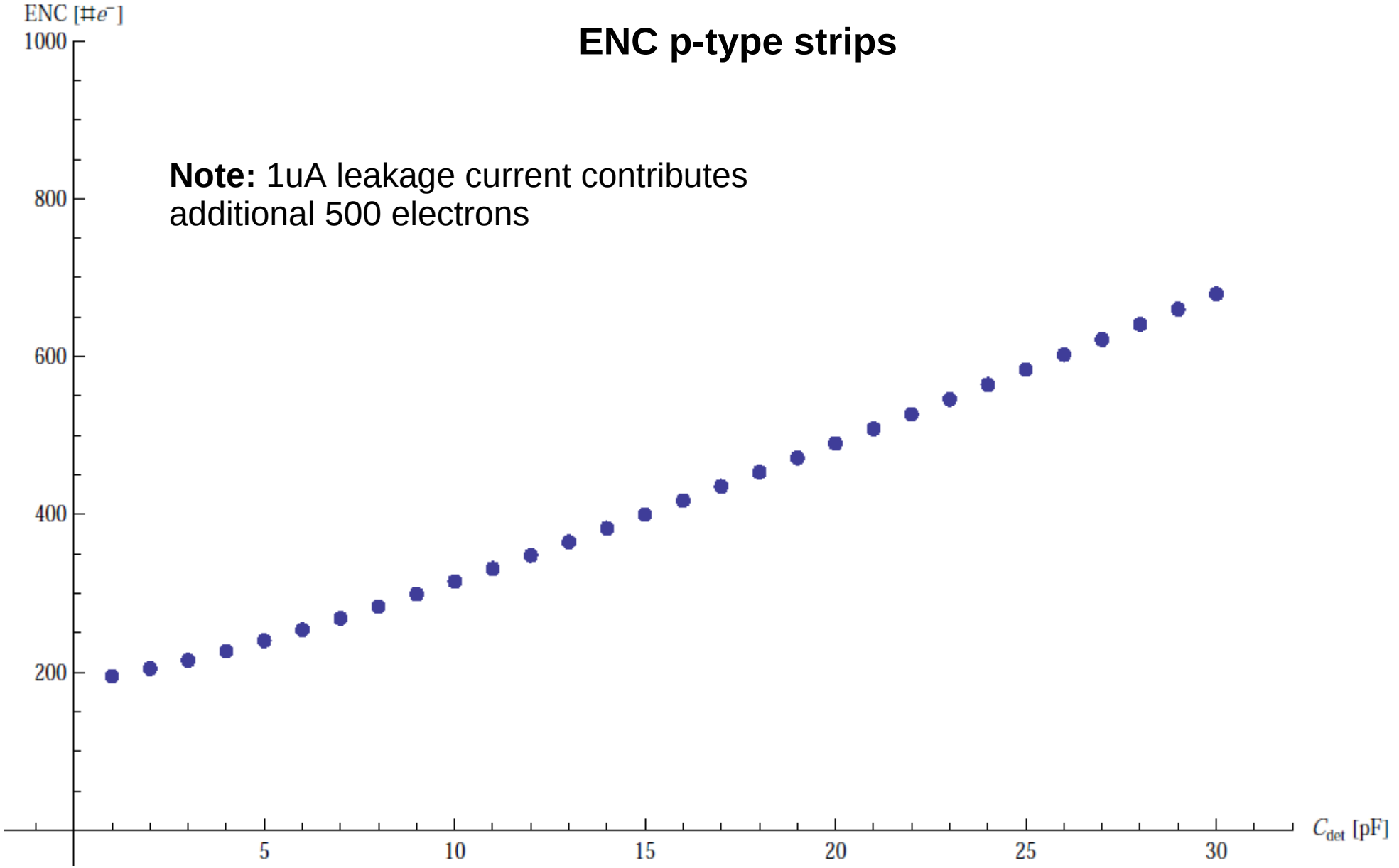
PASTA VFE performance (1)



PASTA VFE performance (2)

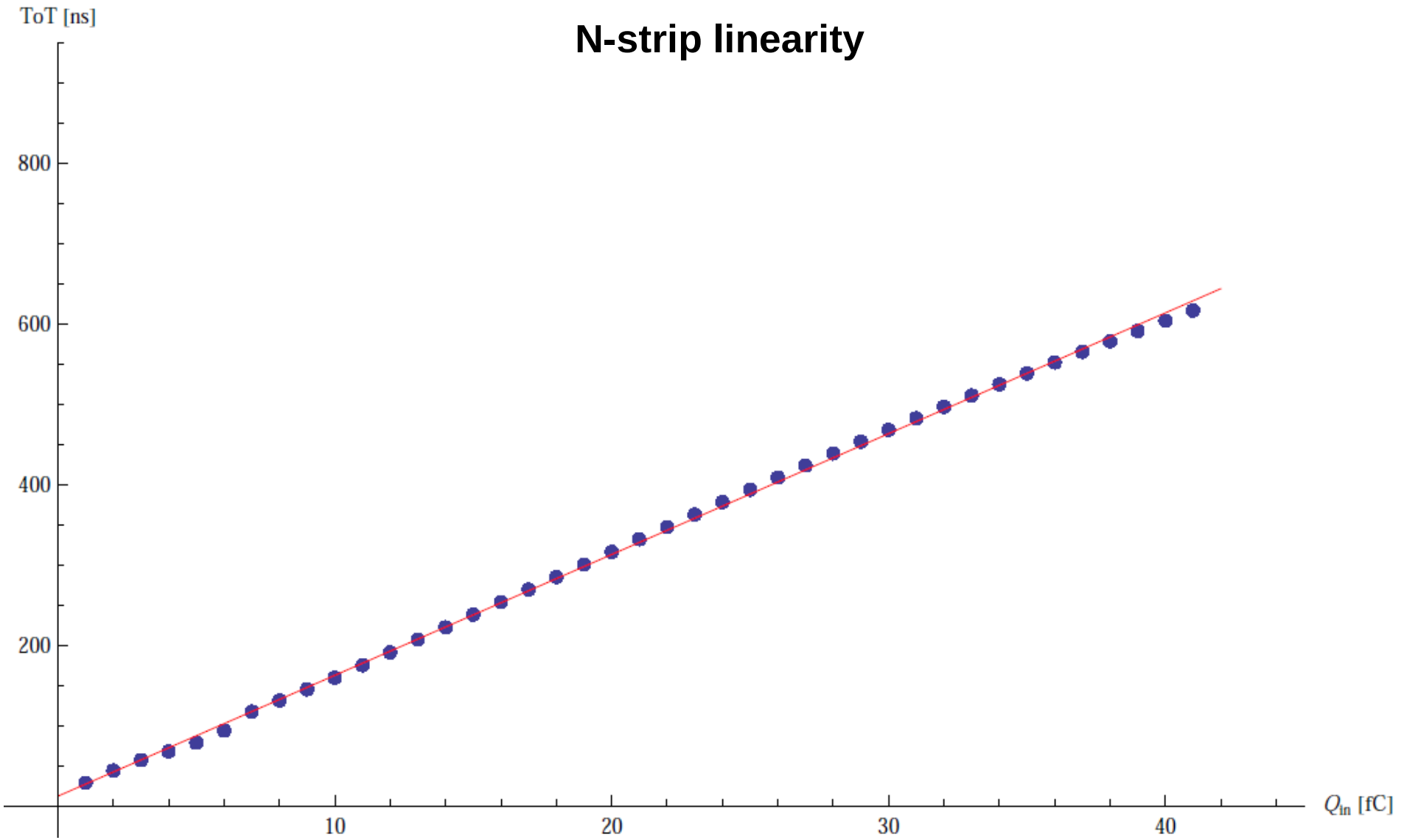
ENC p-type strips

Note: 1uA leakage current contributes additional 500 electrons



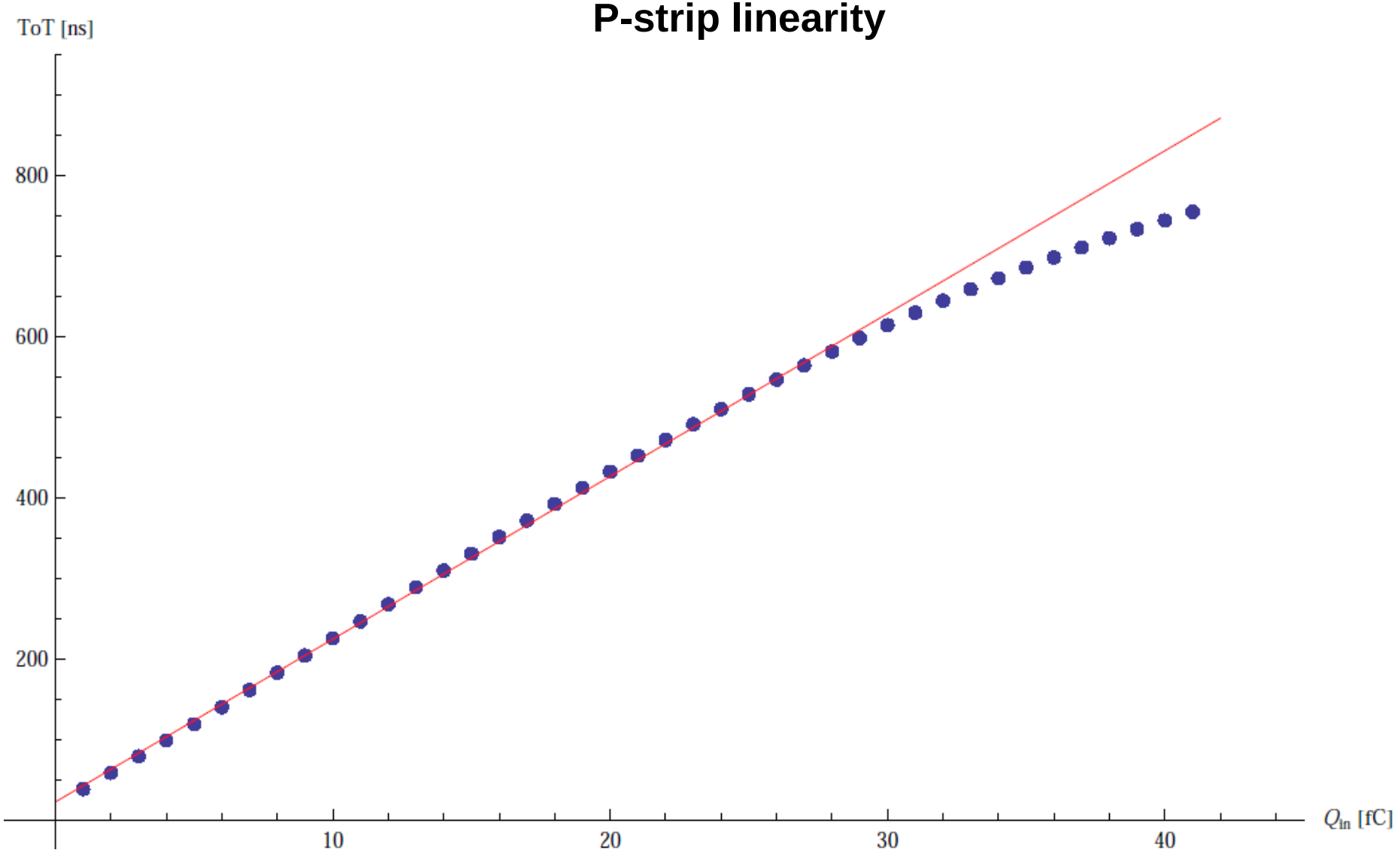
PASTA VFE performance (3)

N-strip linearity



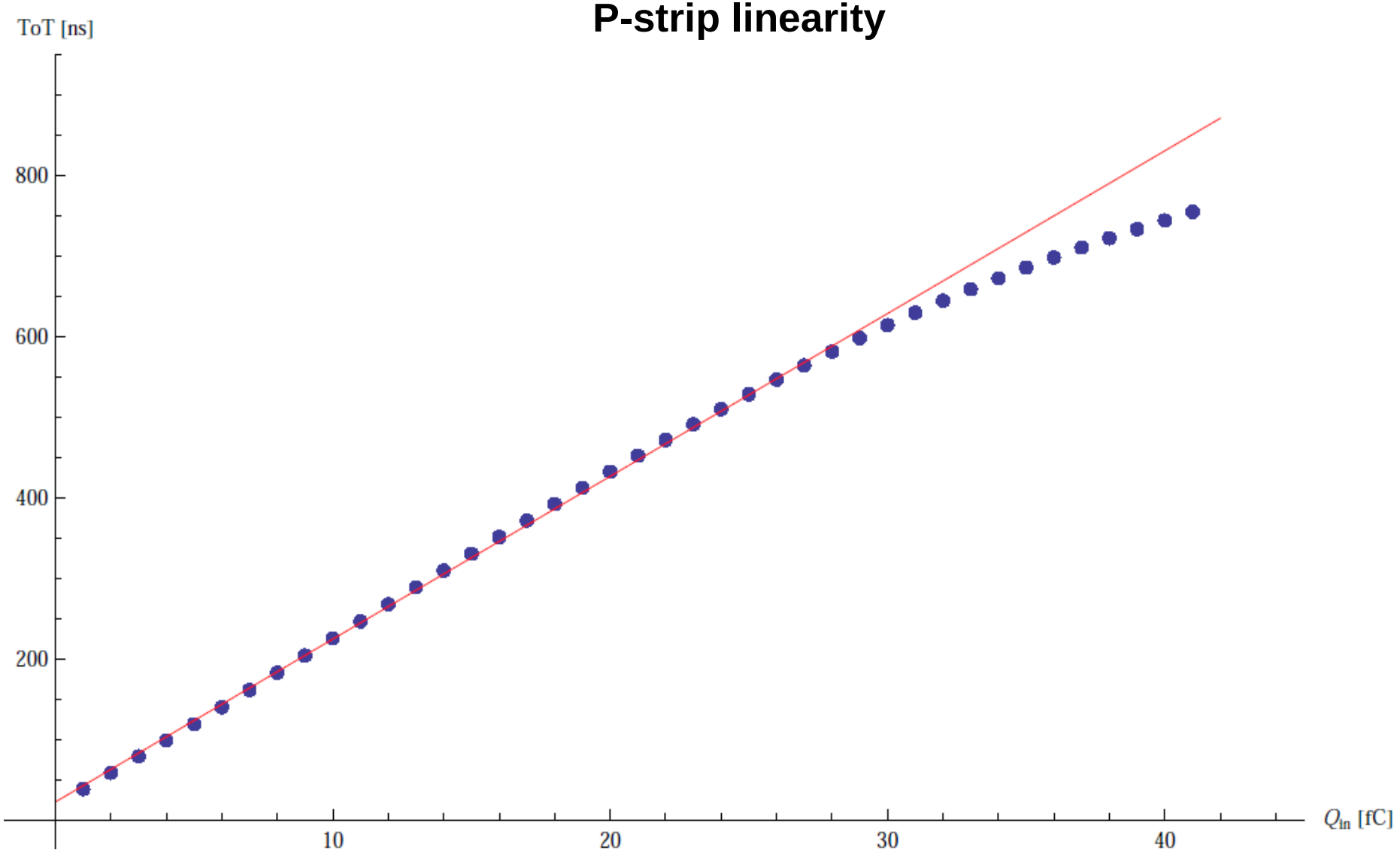
PASTA VFE performance (4)

P-strip linearity

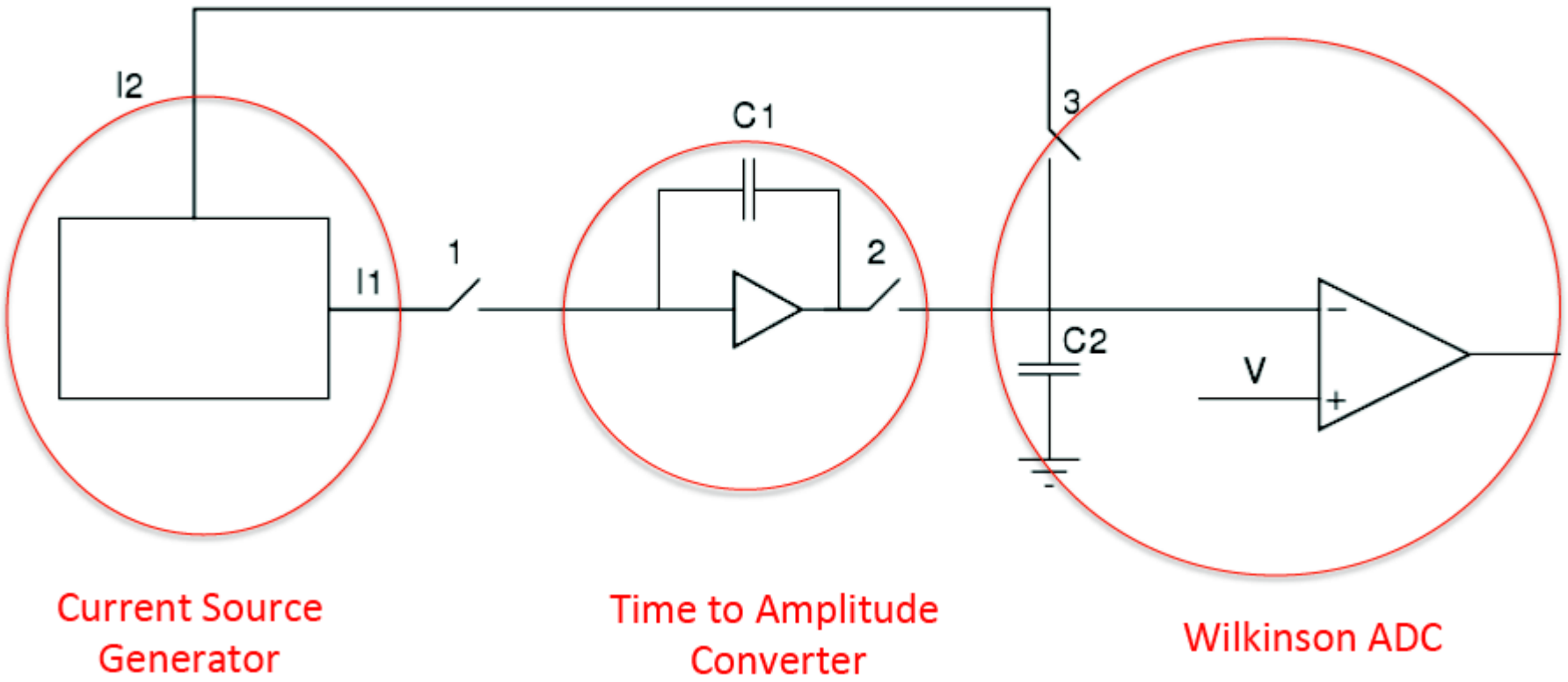


PASTA VFE performance (4)

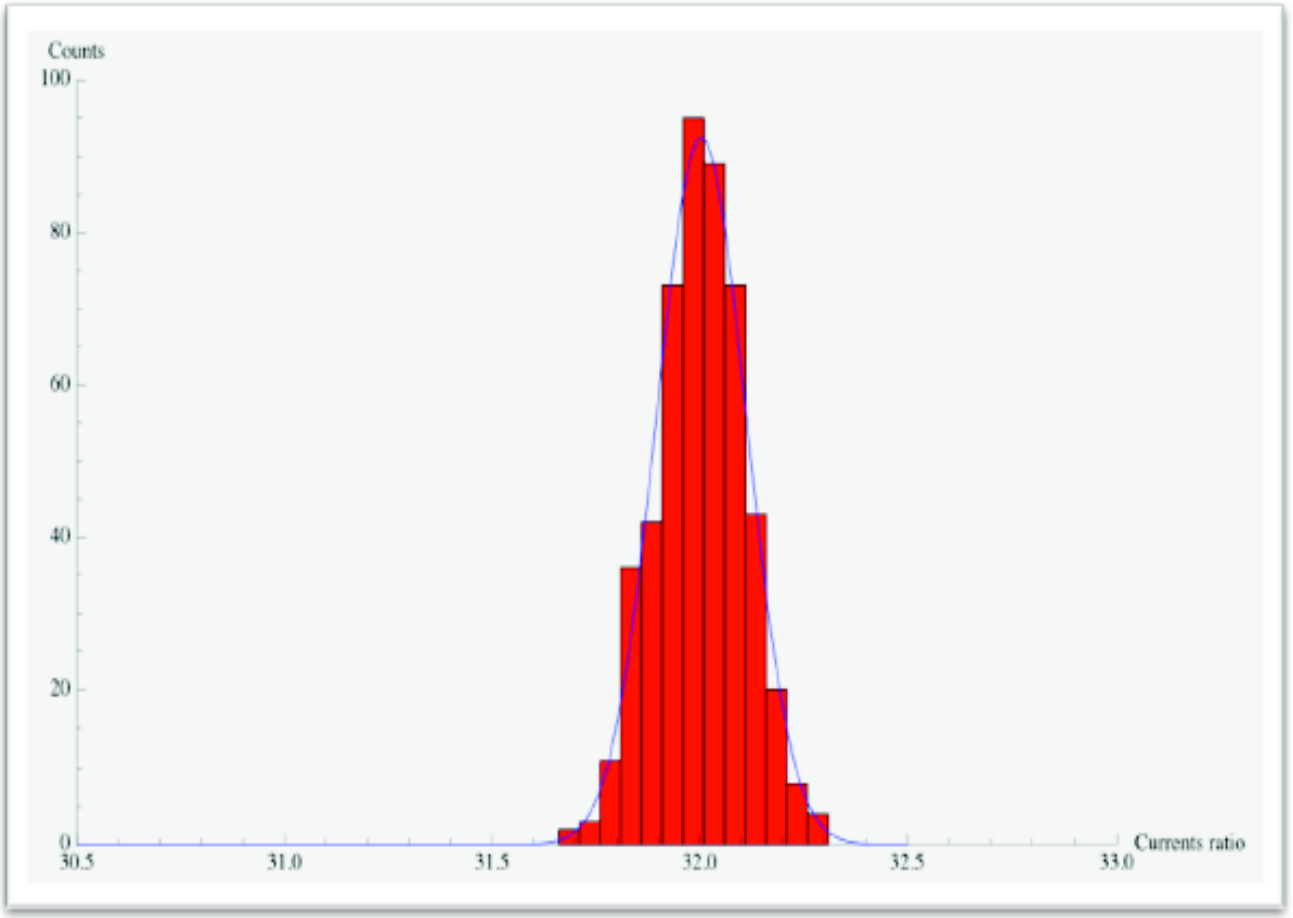
P-strip linearity



TDC design


I2
I1
1
C1
2
3
C2
V
Current Source Generator
Time to Amplitude Converter
Wilkinson ADC

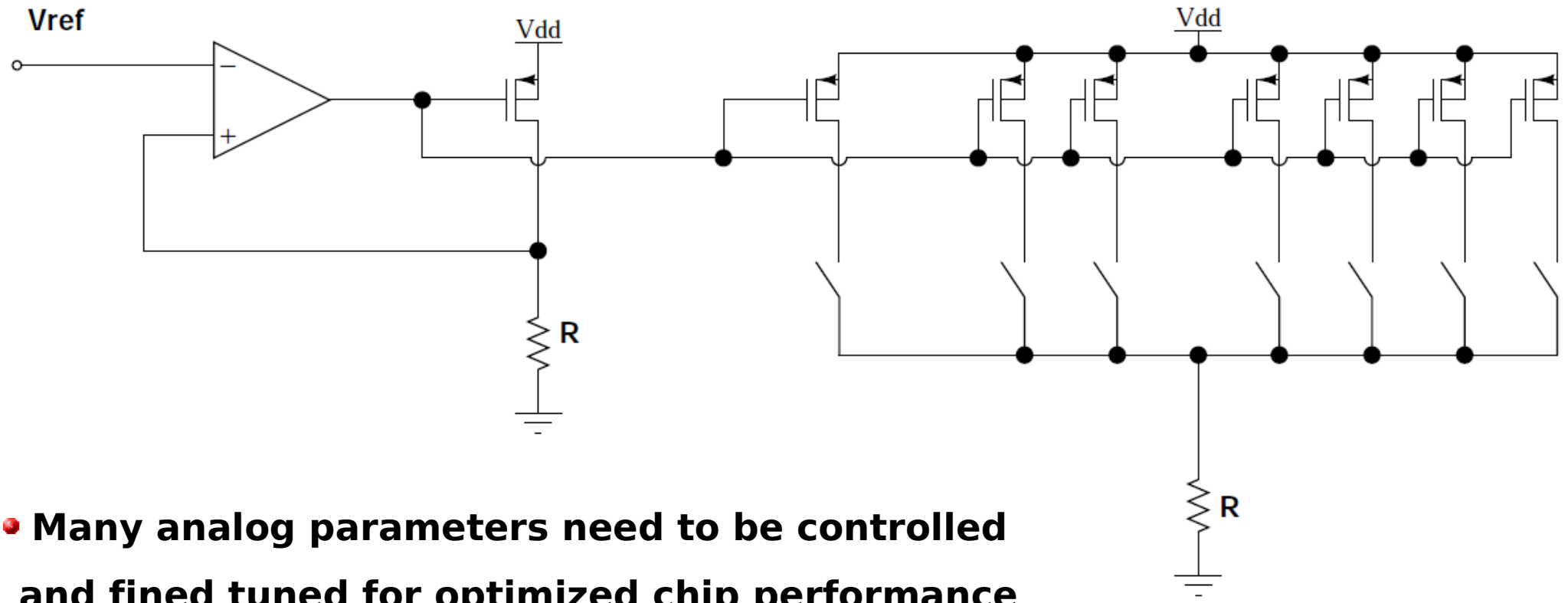
TDC design



<X> = 32.0038

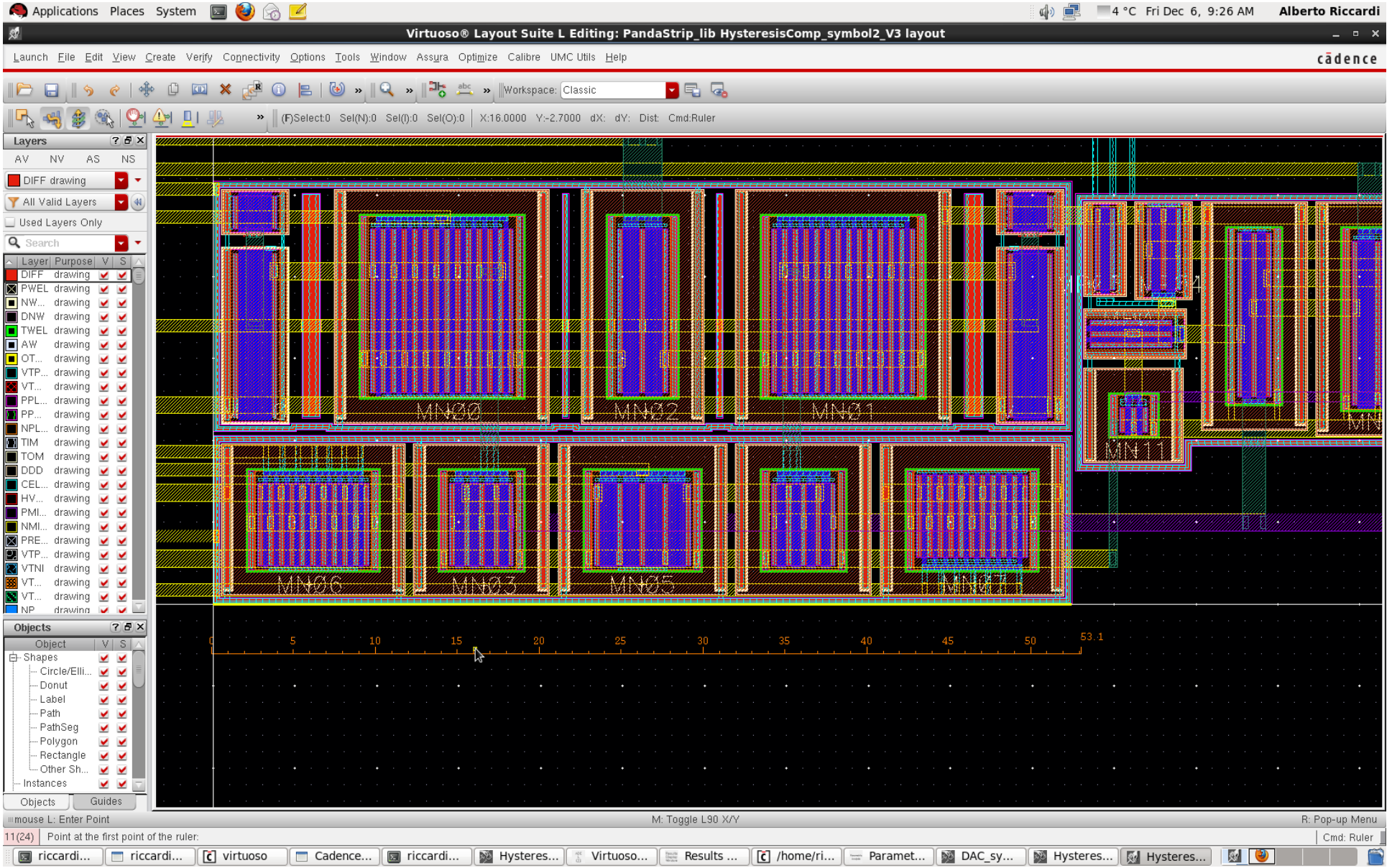
σ = 0.1079

DACs design

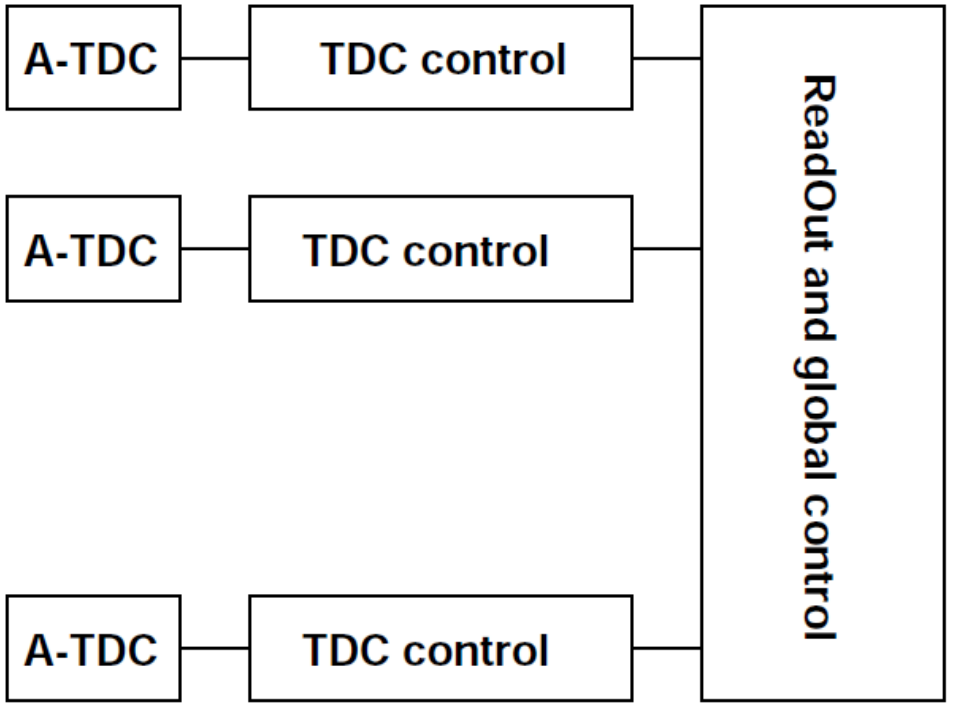


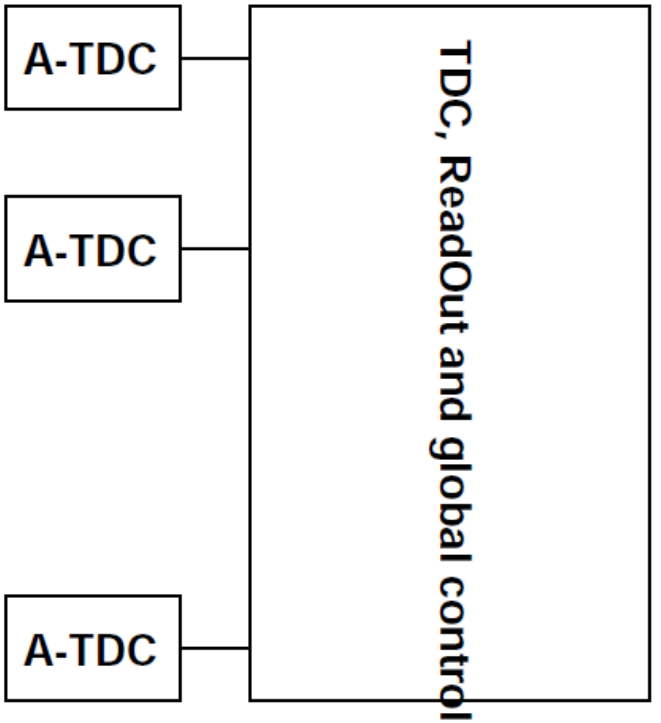
- **Many analog parameters need to be controlled and fined tuned for optimized chip performance**
- **Baseline design, but different optimization (=different layout, at least to some extent…a lot of work!)**

Layout ...


Applications Places System
Alberto Riccardi
Virtuoso® Layout Suite L Editing: PandaStrip_lib HysteresisComp_symbol2_V3 layout
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize Calibre UMC Utils Help
cadence
Workspace: Classic
Layers
DIFF drawing
All Valid Layers
Used Layers Only
Search
Objects
Shapes
Instances
MN30
MN32
MN31
MN11
MN6
MN3
MN5
MN7
mouse L: Enter Point
M: Toggle L90 X/Y
R: Pop-up Menu
Point at the first point of the ruler:
Cmd: Ruler

Digital logic





TOFPET design: two different digital designs, one for TDC control and one for readout

PASTA design: all the logic merged into a single entity:

+ Reduction of timing hazards
+ Simplification of global routing.

Other digital improvements

- **Possibility of using different clock domains**
  - Reduced clock for the core logic (max data rate 1/3 than the one of TOFPET)
  - Core logic at reduced clock, output data transmission at full speed.
- **Configurable counters introduced on a channel and global basis**
  - Possibility to count SEU and event missed due to buffer overflow
- **Work done by a summer student in Juelich on the read-out system**
  - Handling the PASTA data format (e.g. 8b/10b encoding)
  - Graphical user interface for parameter download to the chip

Overall status and outlook

- **Analog**
  - Blocks designed at the schematic level: layout (handcrafted...) underway
- **Digital**
  - New features implemented, automatic place and route being done.
- **Outstanding issues:**
  - Some analog components give head ache in the verifications
  - Issues in interfacing analog and digital design flow.
  - Problems under investigation.....

Try to submit for November 3rd....