PANDA Collaboration Meeting

Sezione di Torino

Update on the electronics for the MVD pixel detector

G. Mazza
on behalf of the Torino MVD pixel group

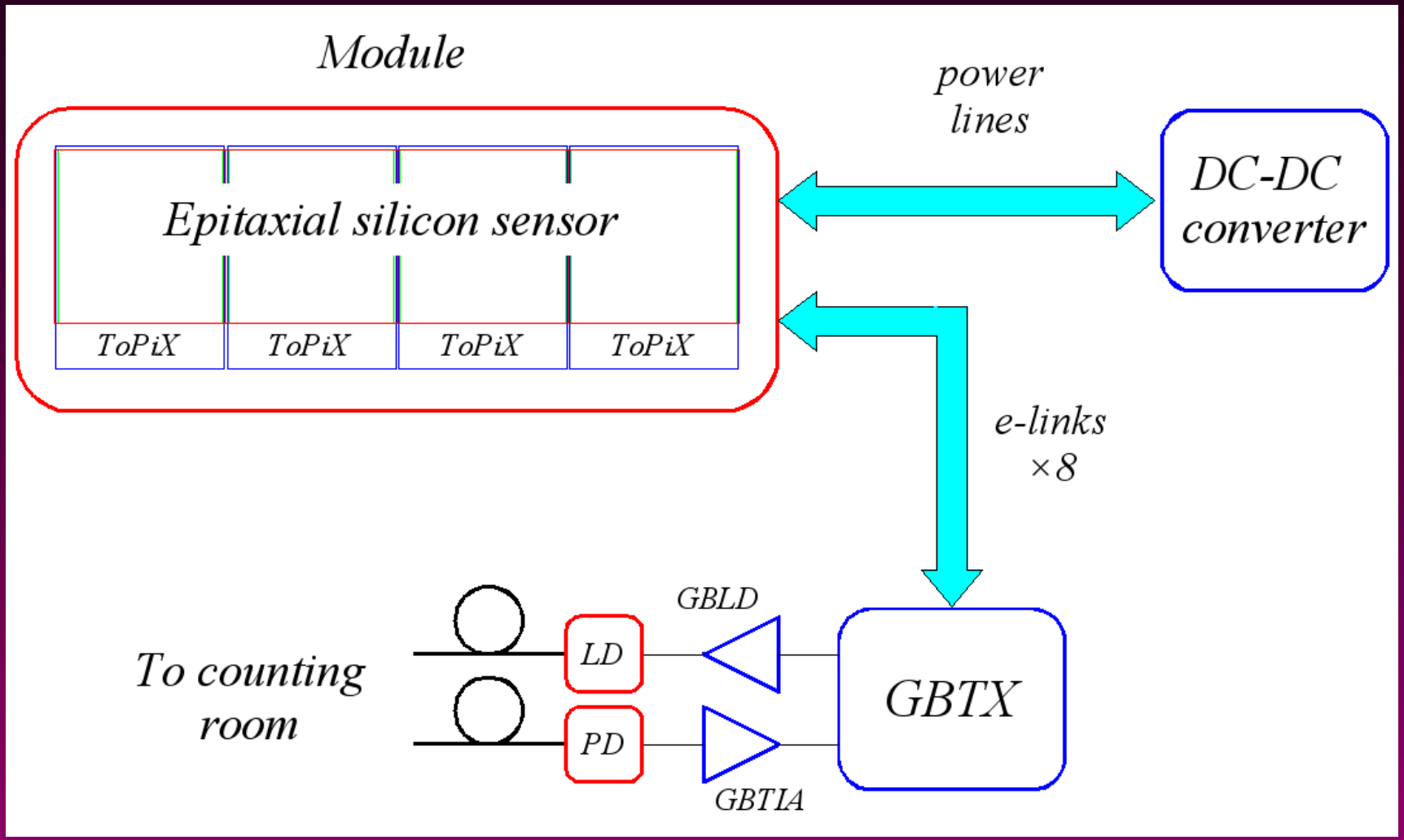
Pixel Detector

Sezione di Torino

Pixel size	$100 \times 100\ \mu m^2$
Chip active area	$11.4 \times 11.6\ mm^2$ (116 rows, 110 columns)
dE/dx measurement	ToT, 12 bits dynamic range
Max input charge	50 fC
Noise floor	<32 aC (200 e^-)
Input clock frequency	155.52 MHz
Time resolution	6.43 ns (1.86 ns r.m.s.) 12.86 ns (3.71 ns r.m.s.)
Power consumption	$< 800\ mW/cm^2$
Max event rate	$6.1 \cdot 10^6$
Total ionizing dose	< 100 kGy

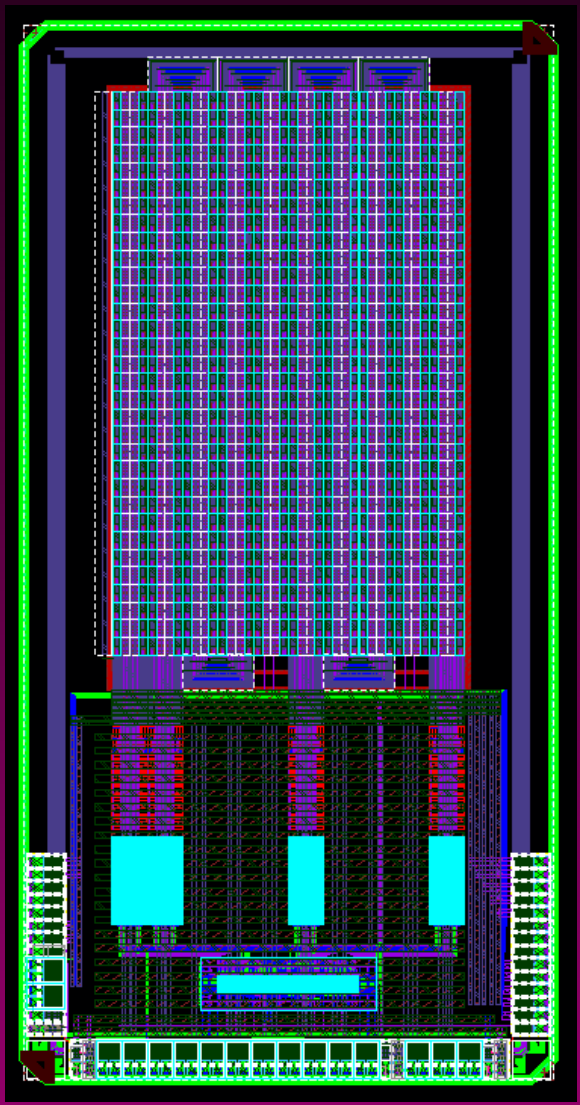
Module readout

Sezione di Torino



ToPiX v4

Sezione di Torino

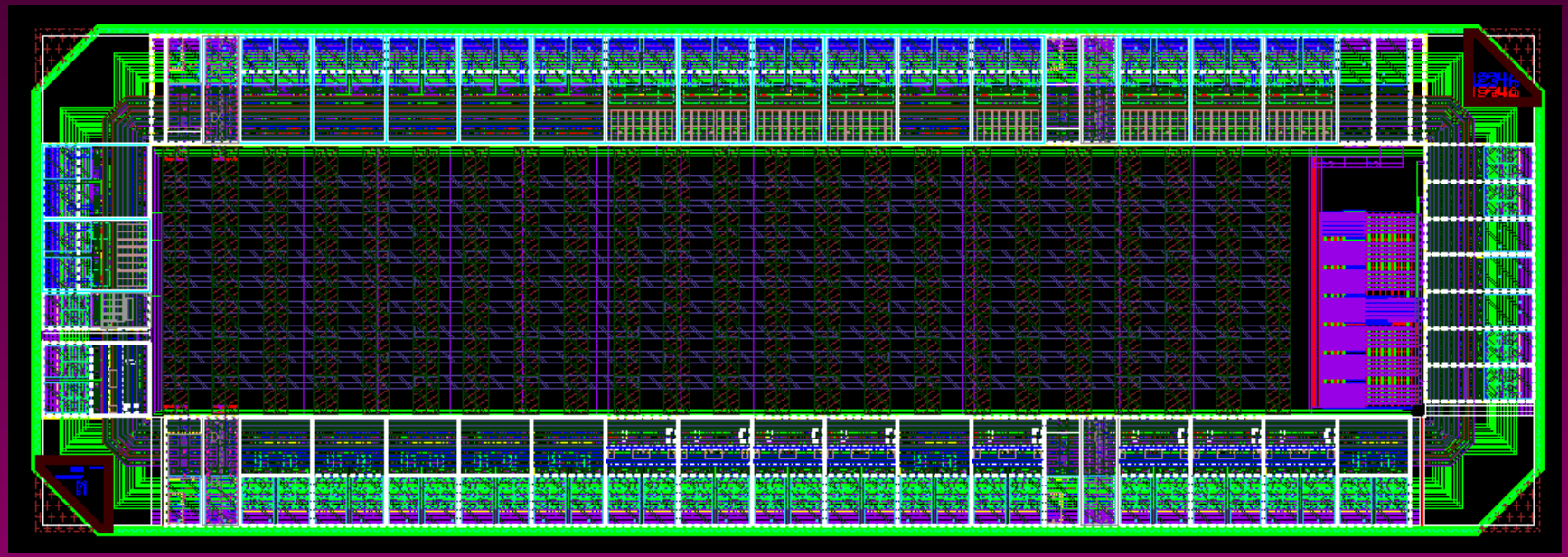


- Size : 3 mm × 6 mm
- CMOS 130 nm
- 640 pixel cells, 2×2×128 and 2×2×32 columns
- Hamming encoding and TMR pixel logic protection schemes
- Compatible with v3 sensors
- Clock frequency 160 MHz
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT-compatible SLVS I/O
- *Received on Feb 18th 2014*

LVDS - SLVS

Sezione di Torino

- Size : 3 mm × 1 mm
- CMOS 130 nm
- Pinout matches ToPiX v4 one
- 7 LVDS in – SLVS out
- 9 SLVS in – LDVS out
- *Received on Feb 18th 2014*



Changes from version 3

Sezione di Torino

Analog cell :

- Analog gain *(not ToT gain)* increase for better linearity in the sub 1 fC region
- Radiation tolerance of the clipping circuit
- Threshold control DAC linearization

Column readout @ 160 MHz

- Improved driver
- Bus capacitance reduction

System aspects :

- DDR readout
- Frame based transmission

Data format

Sezione di Torino

2	12	8	12	6	
01	Chip address	FC	Not used	ECC	*Frame header packet*

2	14	12	12	
11	Pixel address	Leading edge time	Trailing edge time	*Data packet*

2	16	16	6	
10	# of events	CRC	ECC	*Frame trailer packet*

2	38	
00	idle code (Hex 3A55AA55AA)	*Idle packet*

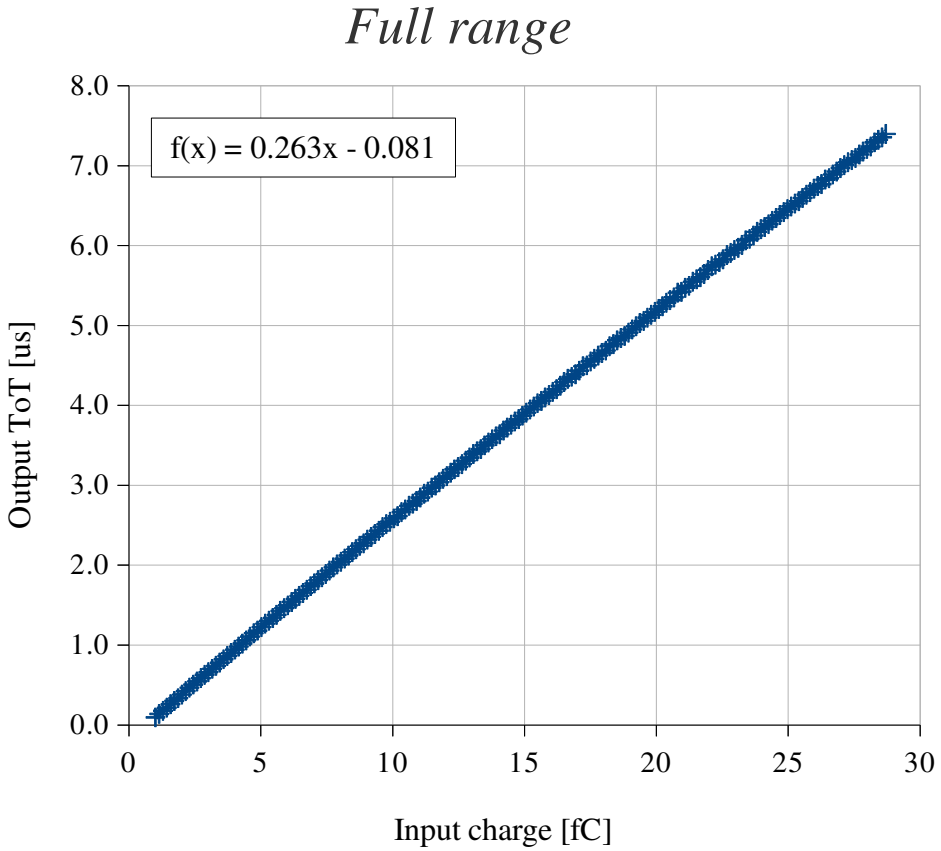
Other features

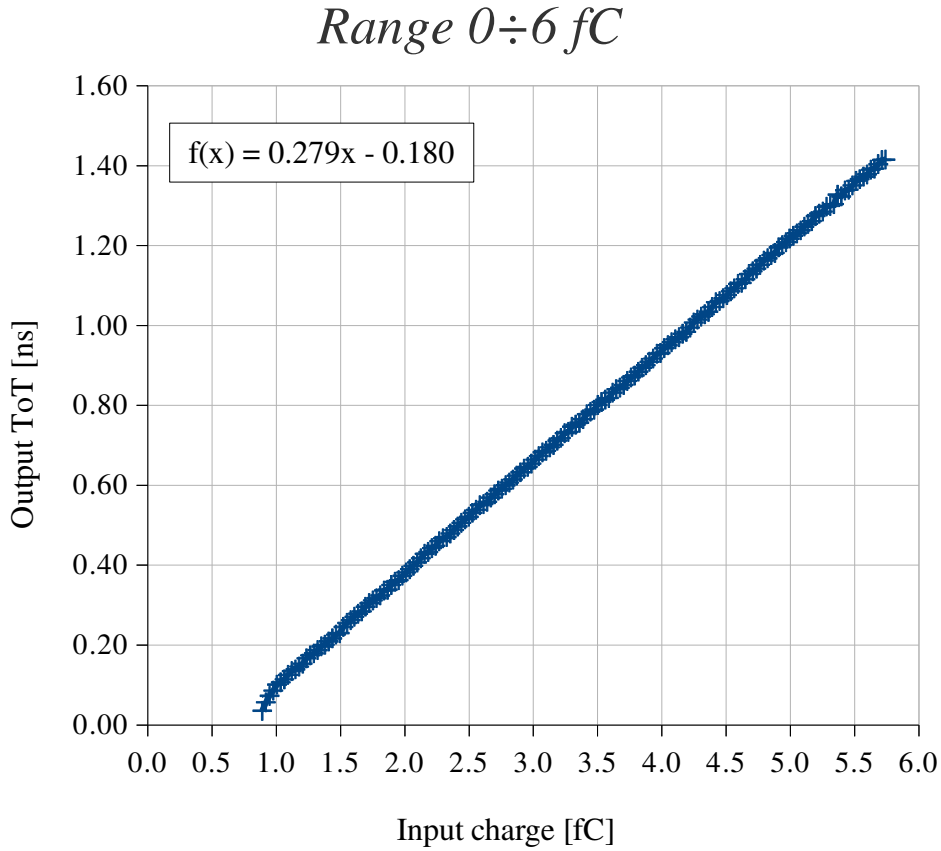
Sezione di Torino

Output frequency	*160 Mb/s*	*320 Mb/s*
Time stamp counter frequency	*160 MHz*	*80 MHz*
Time stamp mode	*Binary*	*Gray*
Idle packet	*off*	*on*
Analog timeout	*off*	*on*
Detector type	*n-type*	*p-type*
SLVS current control	*0000 (max)*	*1111 (off)*
Driver pre-emphasis	*off*	*on*

ToT measurements

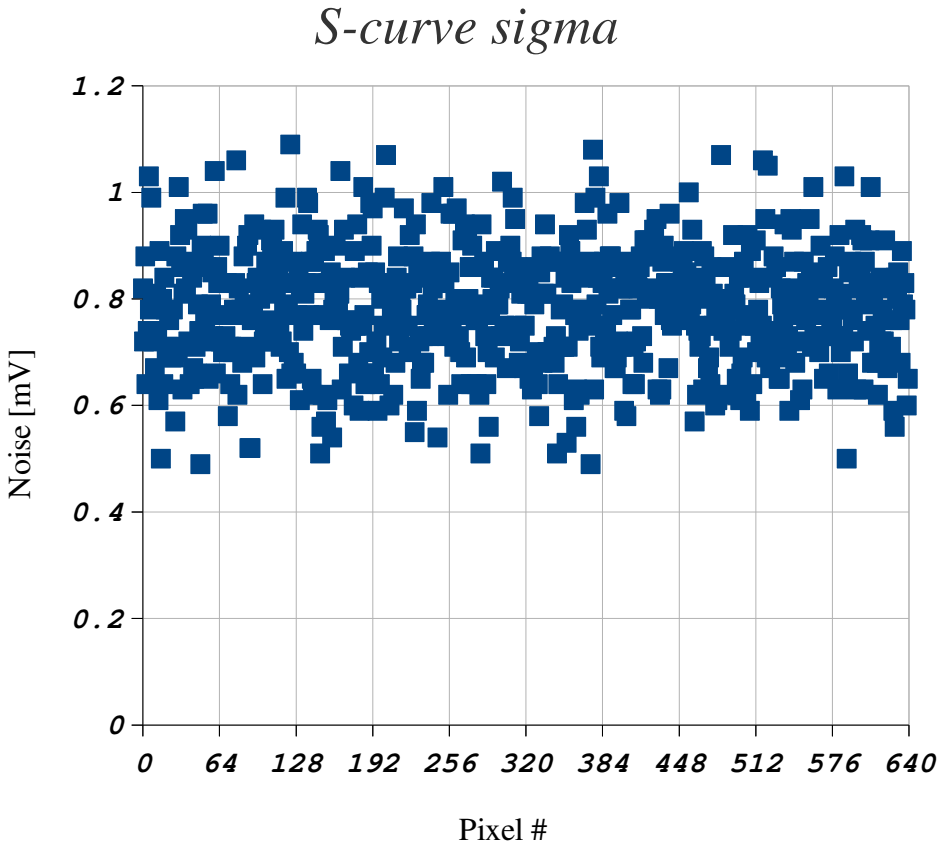
Sezione di Torino

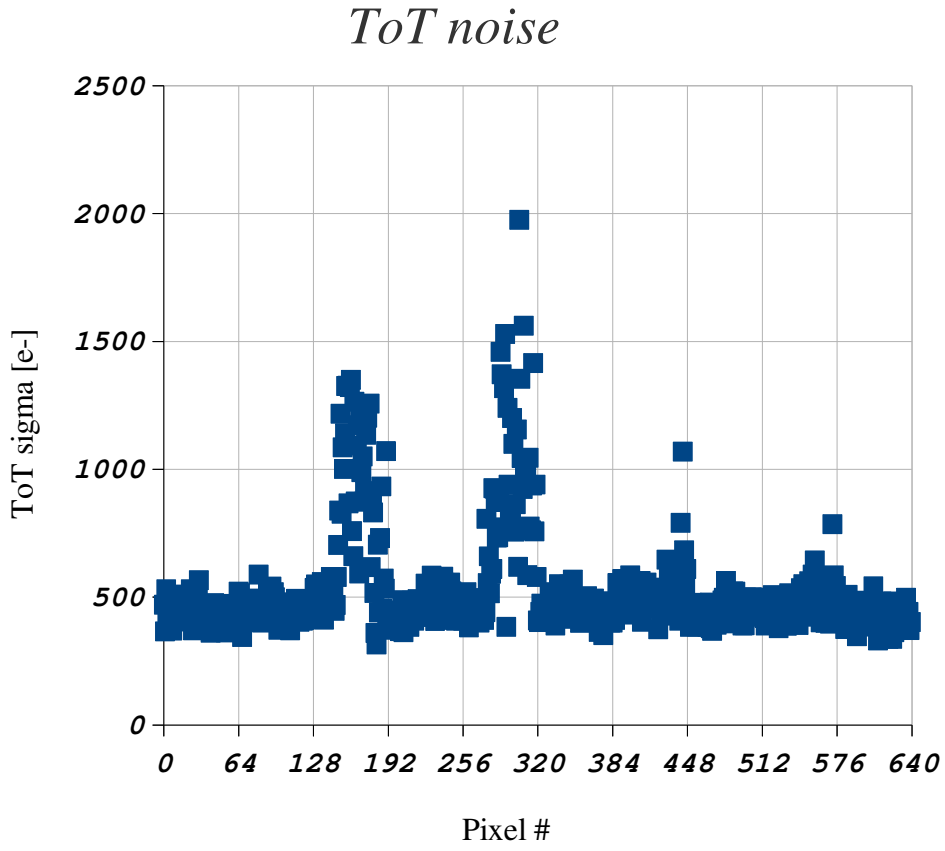




Noise measurements

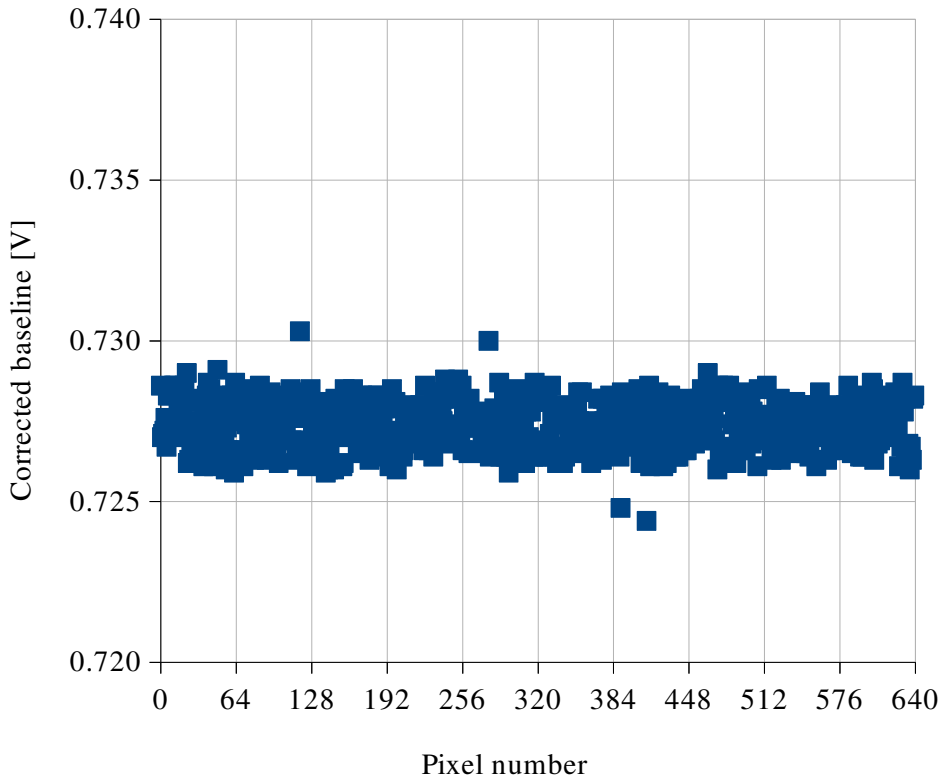
Sezione di Torino

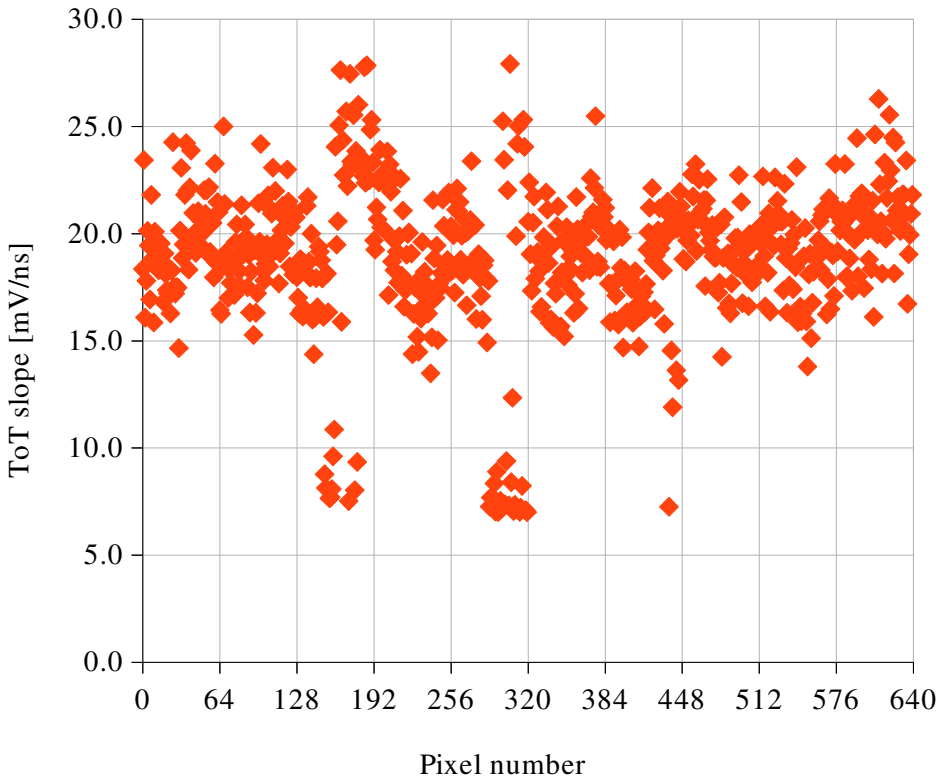




Baseline & ToT

Sezione di Torino



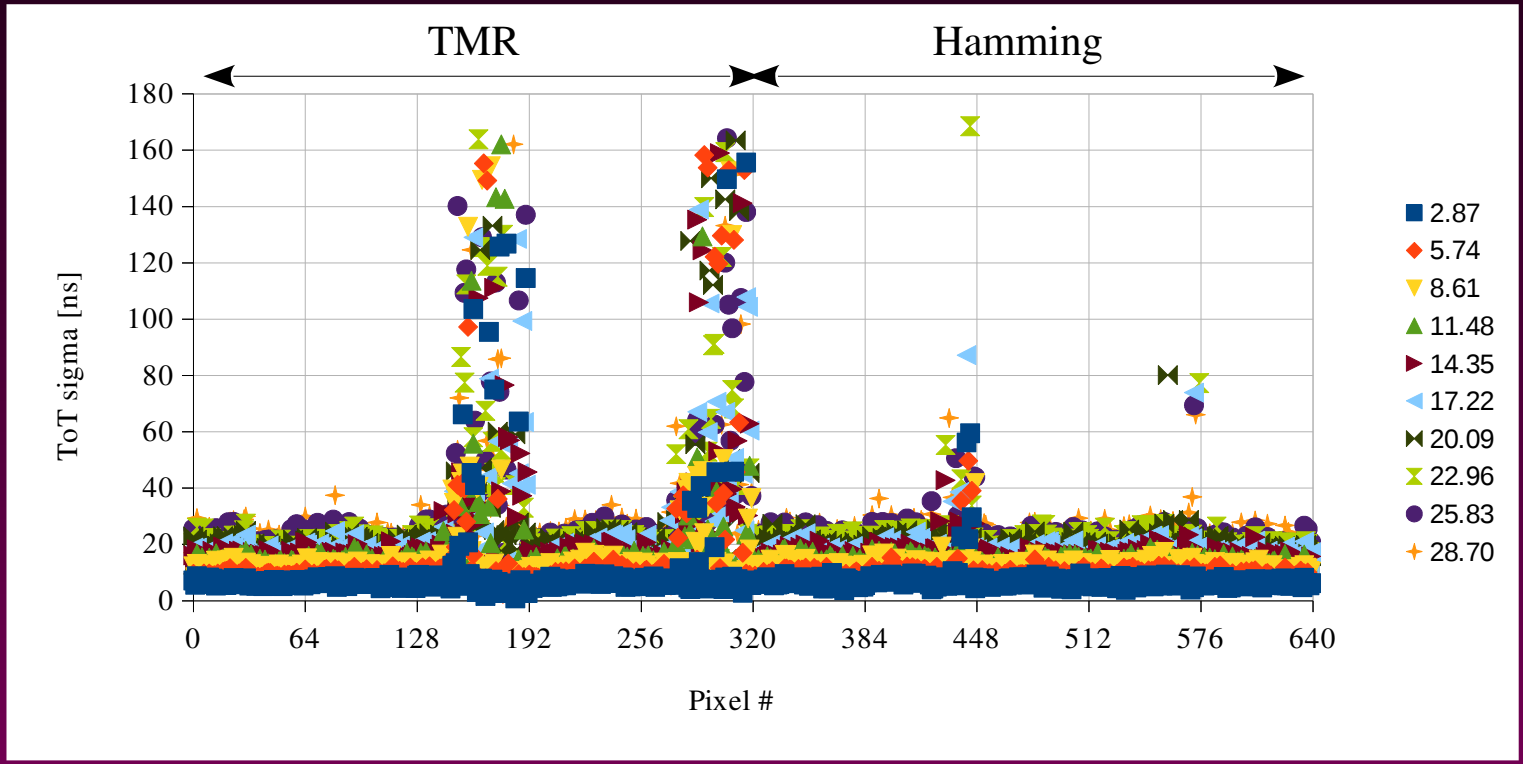


Baseline average value : 727 mV

Baseline sigma : 0.73 mV

ToT sigma

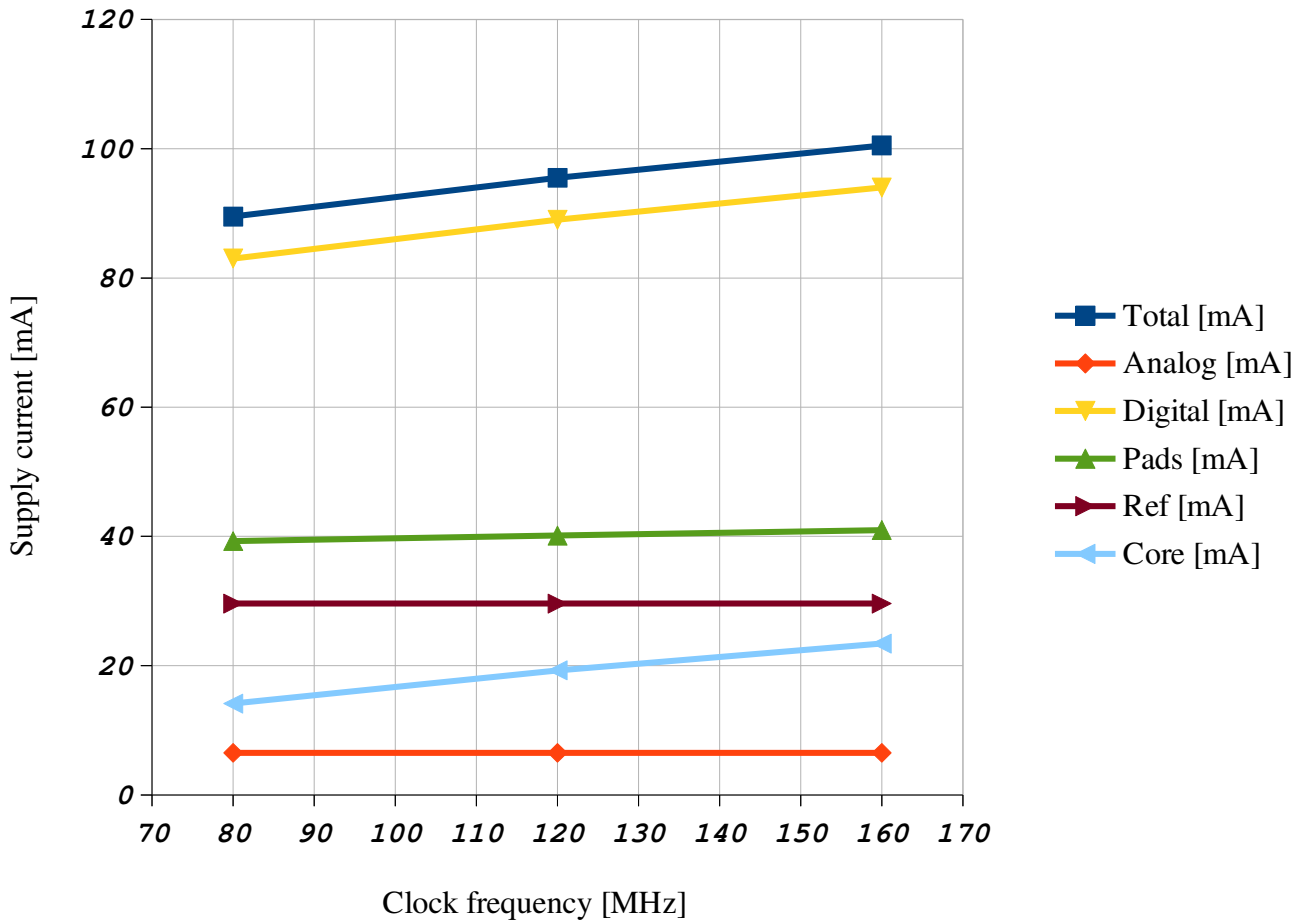
Sezione di Torino



Still some issues on the transmission of the data from the last pixels of the column
Larger spread of the ToT (LSB's '0' preferred over '1')
Increasing the power supply (from 1.2 V to 1.5 V) reduces the problem
TMR slower than Hamming

Supply current

Sezione di Torino



Estimated power density for the full size version :

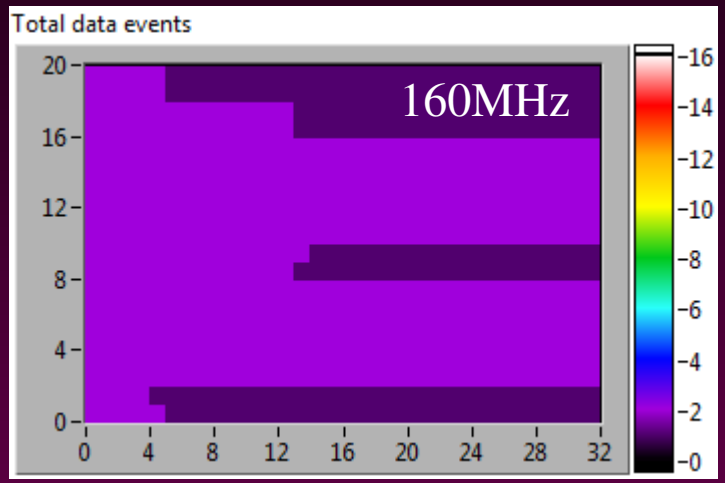
523 mW/cm^2 @ 80 MHz
666 mW/cm^2 @ 120 MHz
725 mW/cm^2 @ 160 MHz

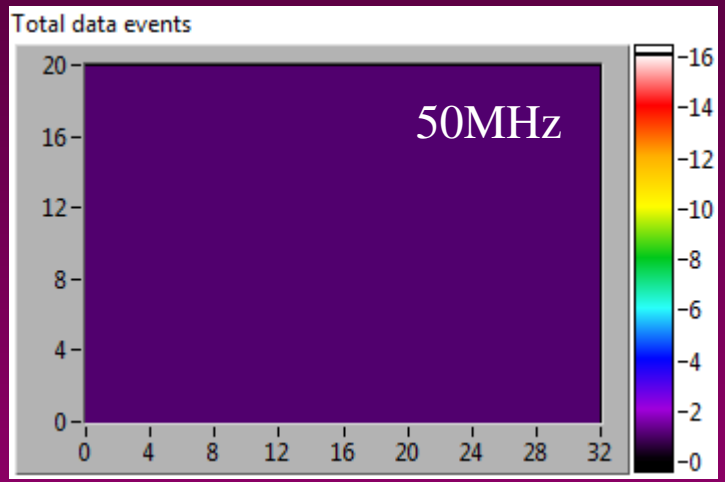
ToPiX v3 based estimate :

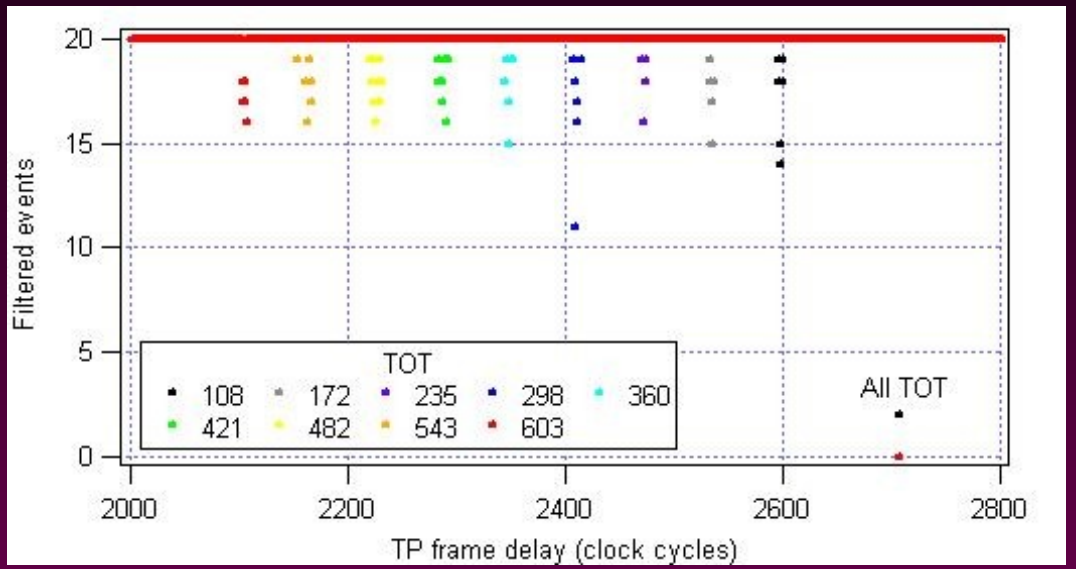
858 mW/cm^2 @ 160 MHz

Dummy events

Sezione di Torino







Dummy events are generated in many cases @ 160 MHz
Reason : busy propagation delay underestimated
To be corrected in the next version
Workaround : filter out events with LE or TE = FFF
Some loss in efficiency
Note : FFF in Gray is AAA in binary !

ToPiX v4 test overview

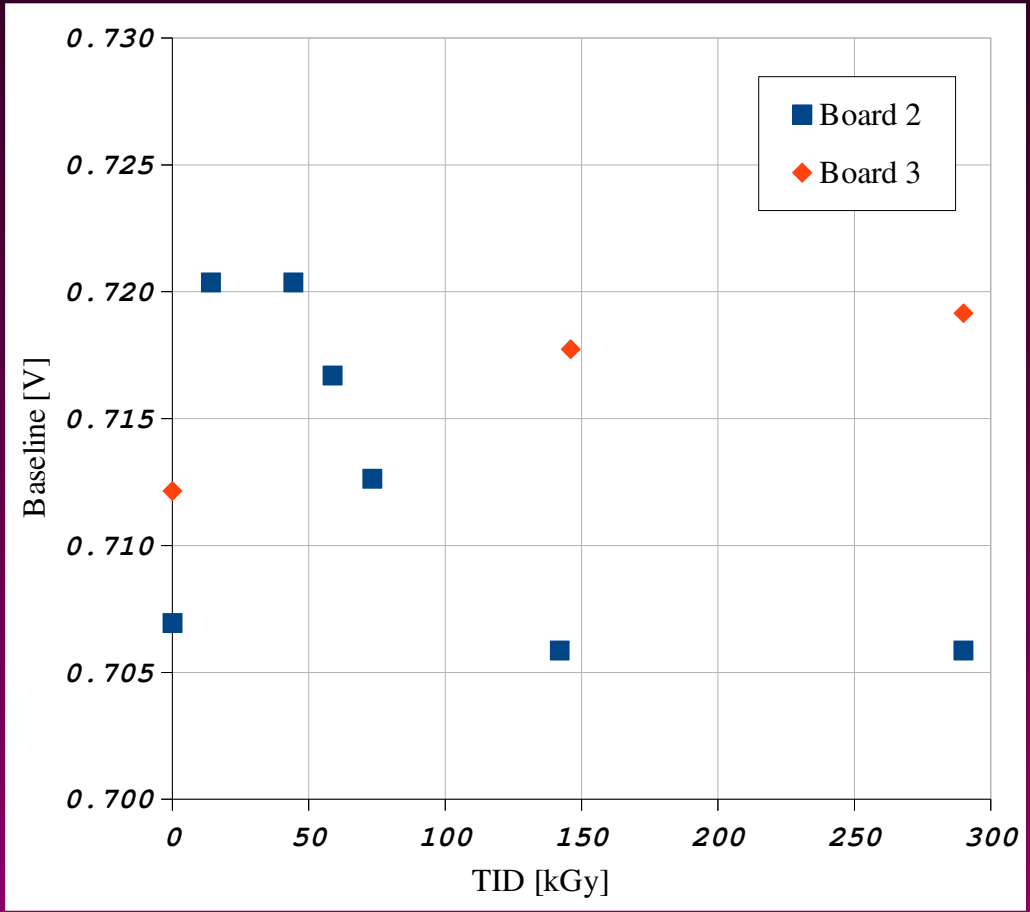
Sezione di Torino

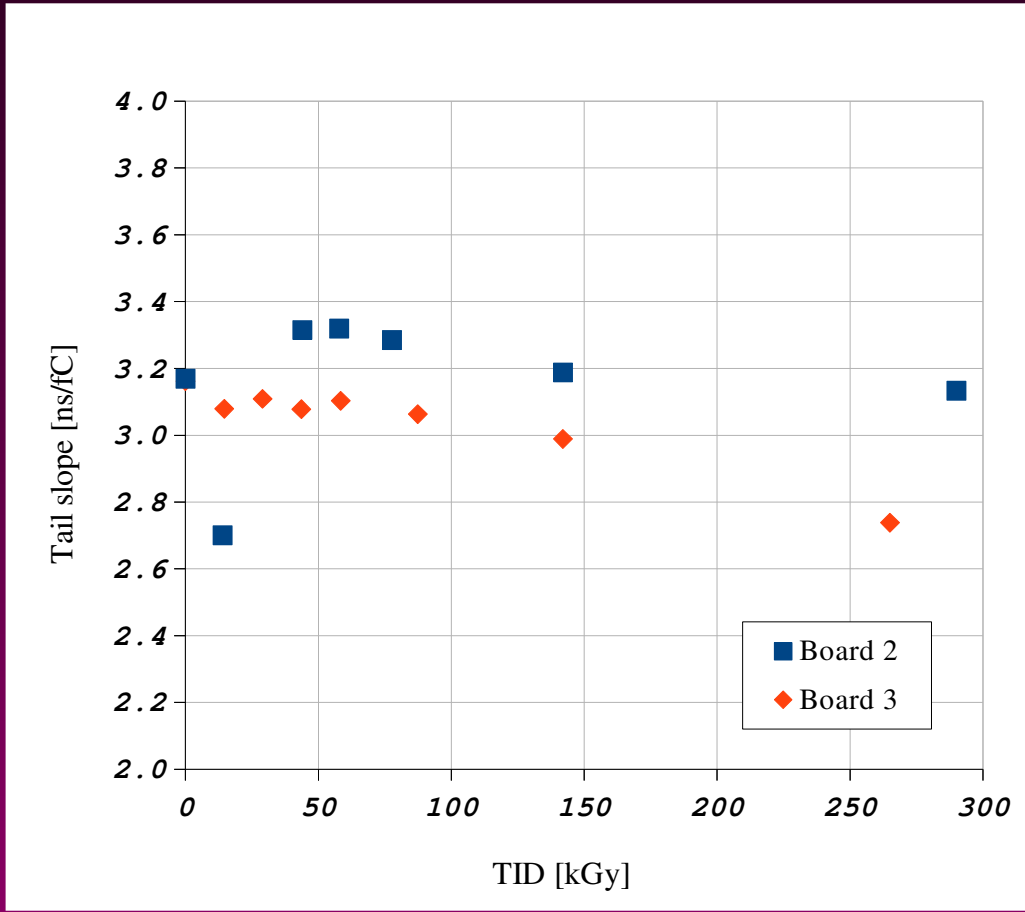
- Pre-amplifier linear range extension in the low range ok.
- Threshold voltage linearization ok.
- Time stamping and write pixel configuration @ 160 MHz ok .
- Data readout @160 MHz ok in slow readout mode only (CCR0 bit 3).
  - Note : max readout frequency in slow mode is 8.89 Mevents/(s·double column), i.e. 347 Mevents/cm^2 → *this is not a limiting factor*
- Read pixel configuration @160 MHz not ok (no slow r/o mode for config). Max frequency 80 MHz
- Dummy events are generated above 50 MHz
  - due to underestimated busy delay – should be easy to fix in the next version
  - can be filtered out with small inefficiency in the current version

TID measurements baseline – tail slope

Sezione di Torino

Preliminary results

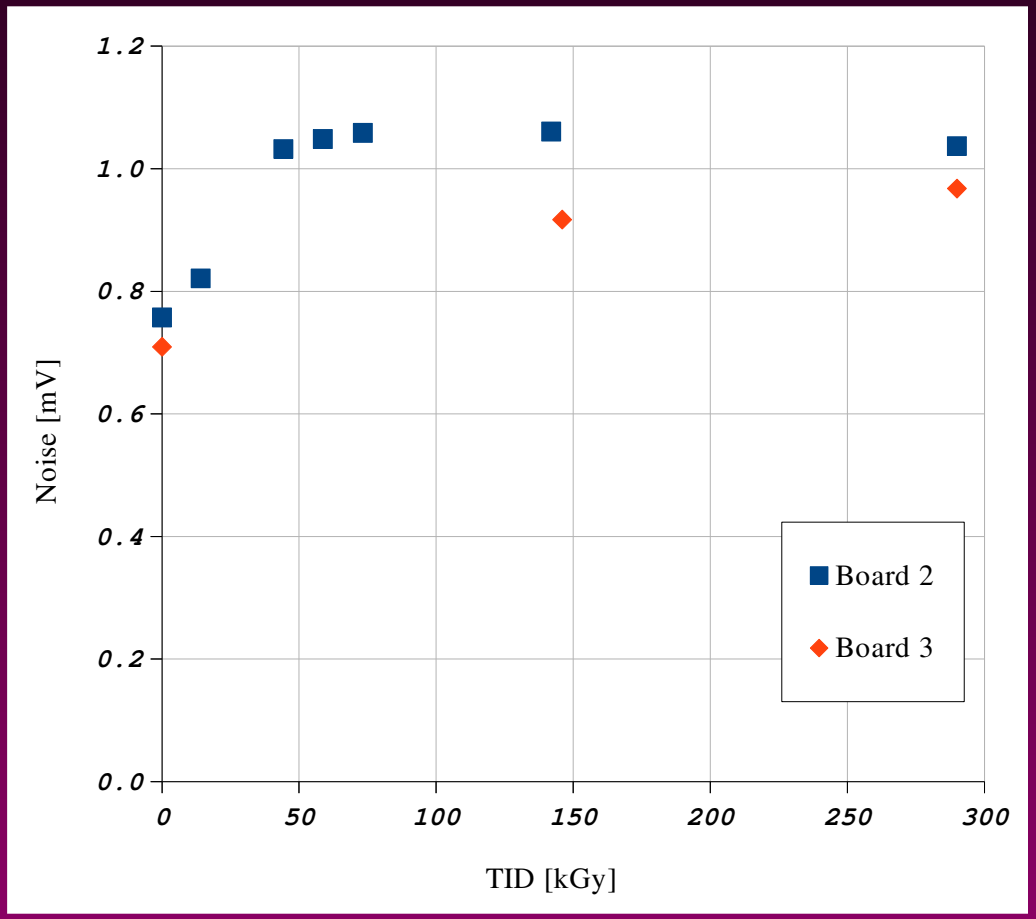




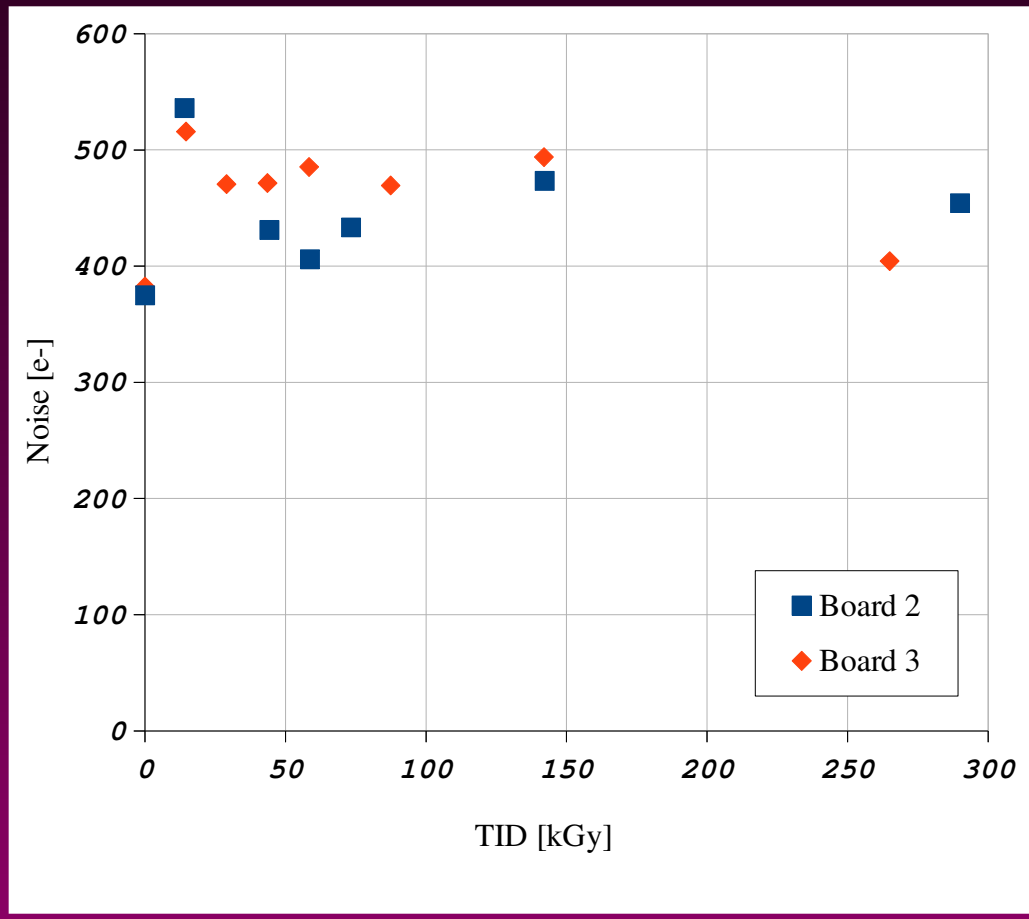
TID measurements noise

Sezione di Torino

S-curve sigma



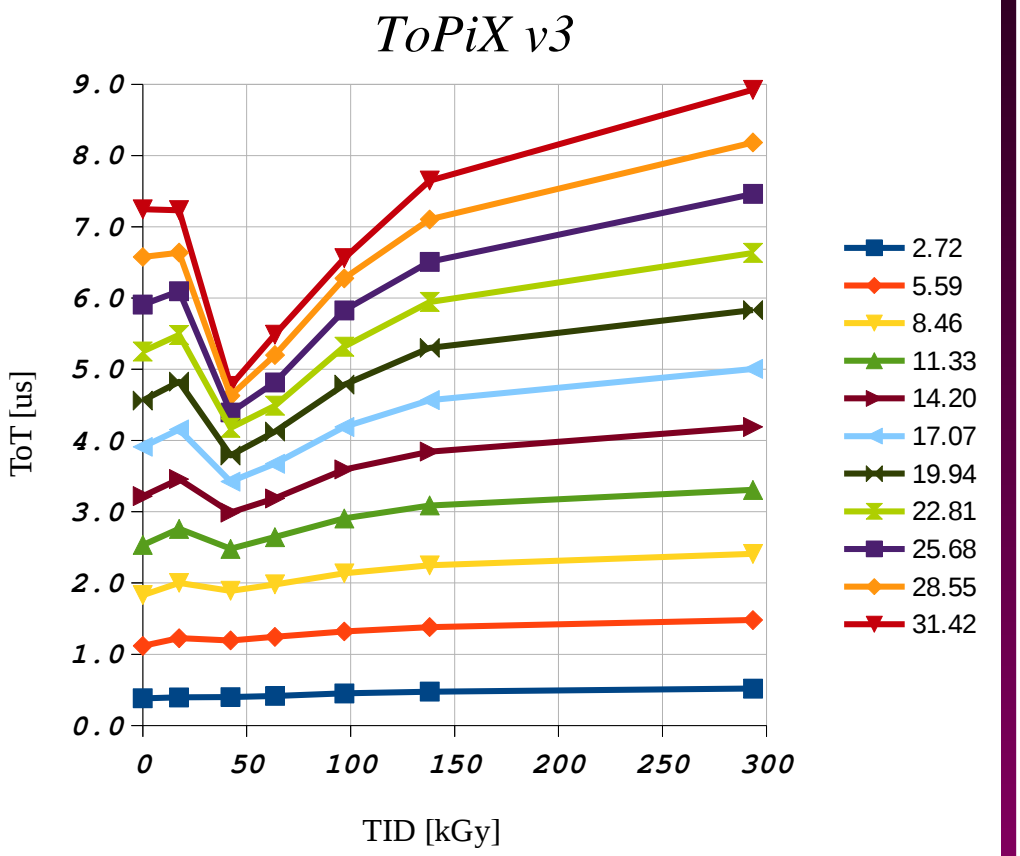
ToT noise

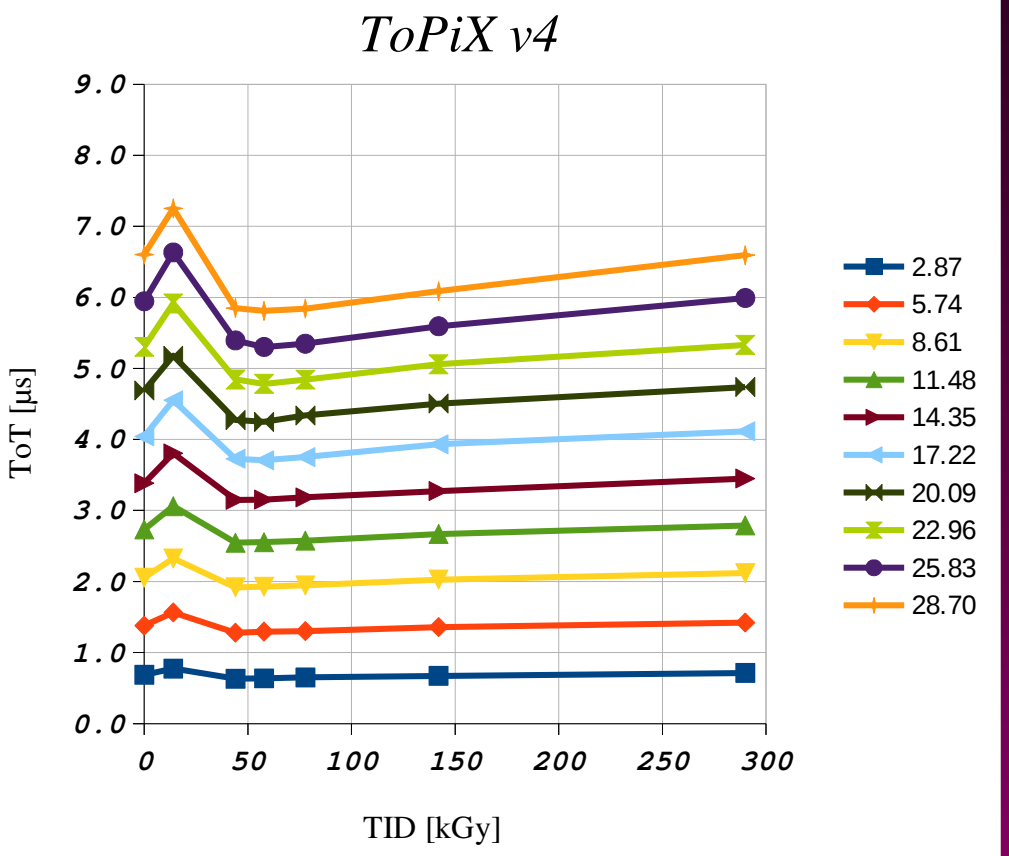


Preliminary results

TID measurements ToT

Sezione di Torino





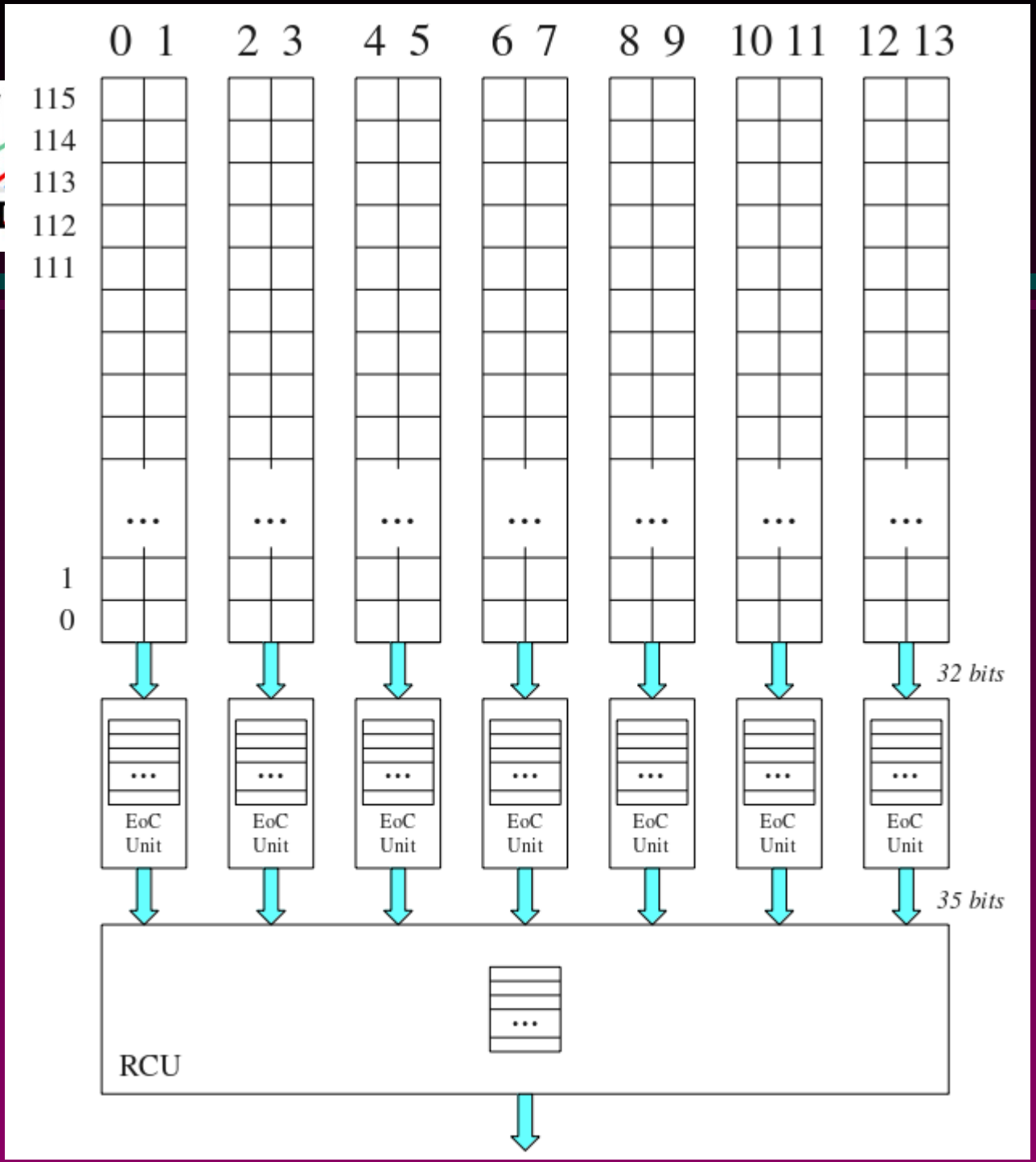
Preliminary results

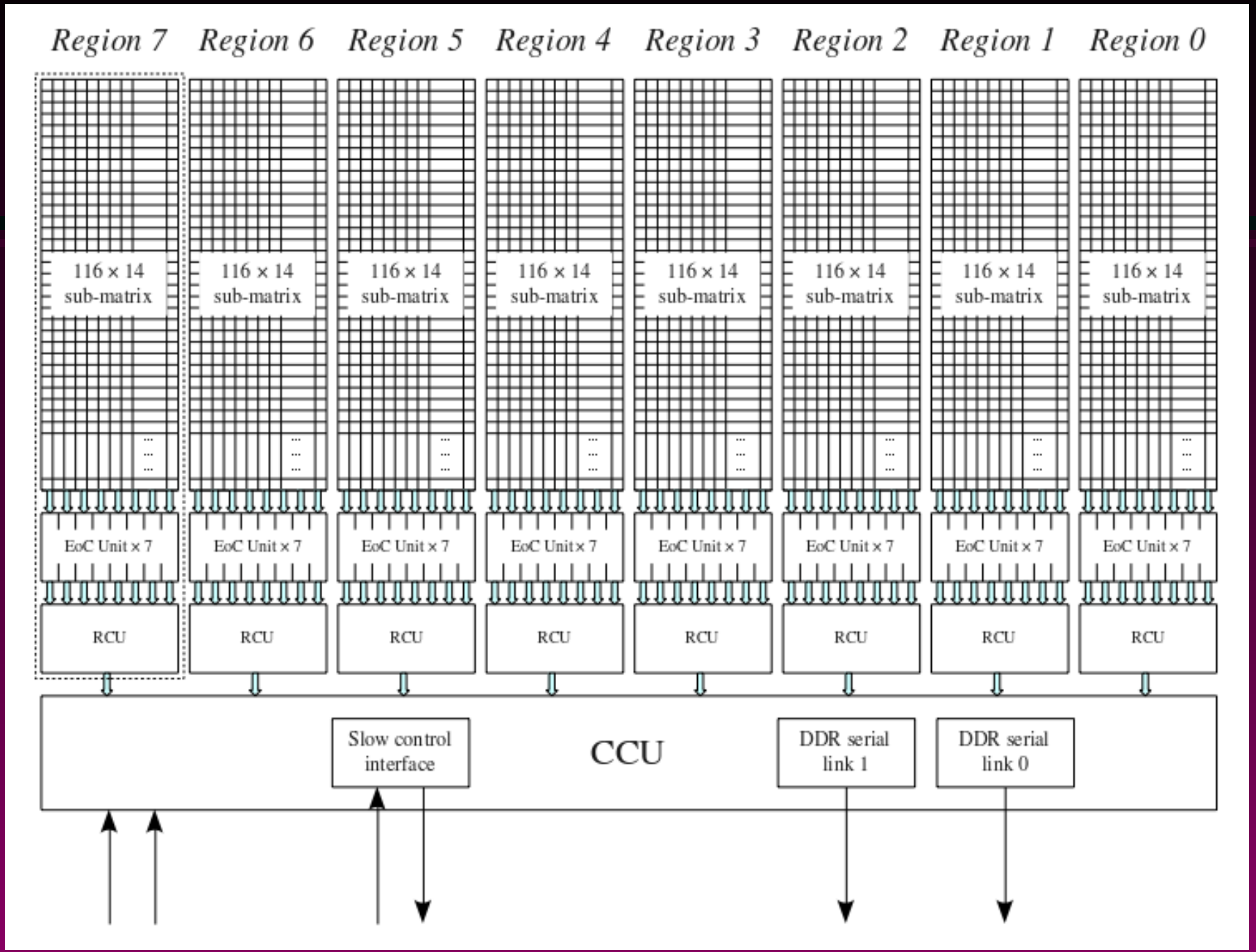
ToPiX v5

Sezione di Torino

- Full size chip design started
- Size (*preliminary*) : 11.2 mm × 14.8 mm
- Pixel matrix (*preliminary*) : 110 × 116
- Input clock : 160 MHz
- Output bandwidth (*preliminary*) : 2 × 320 Mb/s
- Supply voltage : 1.2 V
- Columns divided in 8 regions with 7 double columns each
- Double tier buffering (FIFO in the end of column and region control)

REGION


0 1
2 3
4 5
6 7
8 9
10 11
12 13
115
114
113
112
111
1
0
32 bits
EoC Unit
35 bits
RCU


Region 7
Region 6
Region 5
Region 4
Region 3
Region 2
Region 1
Region 0
116 × 14 sub-matrix
EoC Unit × 7
RCU
Slow control interface
CCU
DDR serial link 1
DDR serial link 0

Conclusions

Sezione di Torino

- ToPiX v4 has been received from foundry on on Feb 18th 2014.
- Test ongoing – correct operation @ 160 MHz albeit column data readout is at the limit – some margin has to be added.
- SEU tests performed, data analysis ongoing.
- TID test just completed, v3 problems look solved.
- Full size ToPiX submission foreseen for 4th quarter 2015
- GBT chipset in production.
- DC-DC converter ordered.

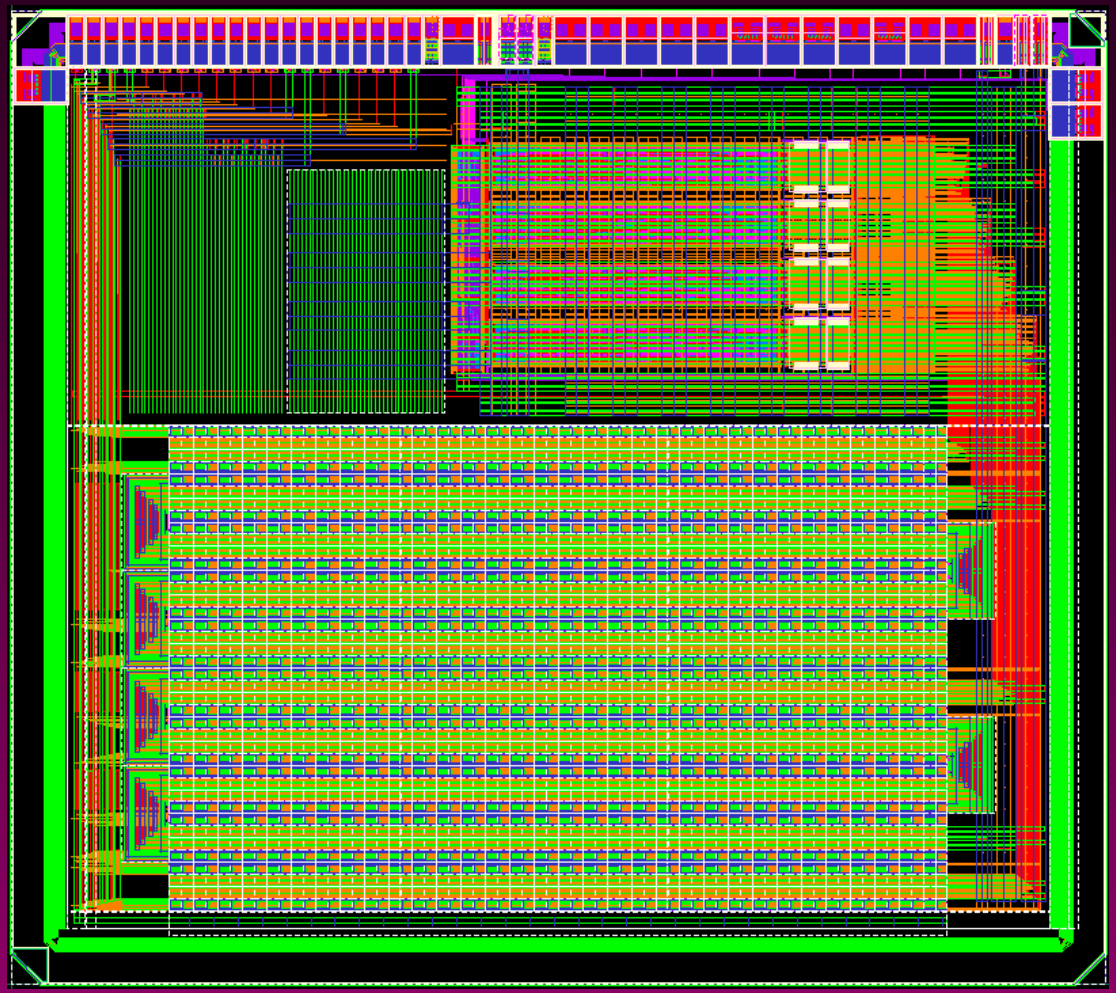
MVD Meeting

Sezione di Torino

Backup slides

ToPiX v3 layout

Sezione di Torino



- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O