JÜLICH
FORSCHUNGSZENTRUM

PASTA Status Update

Current status of analog and digital parts

André Goerres

10 June 2014

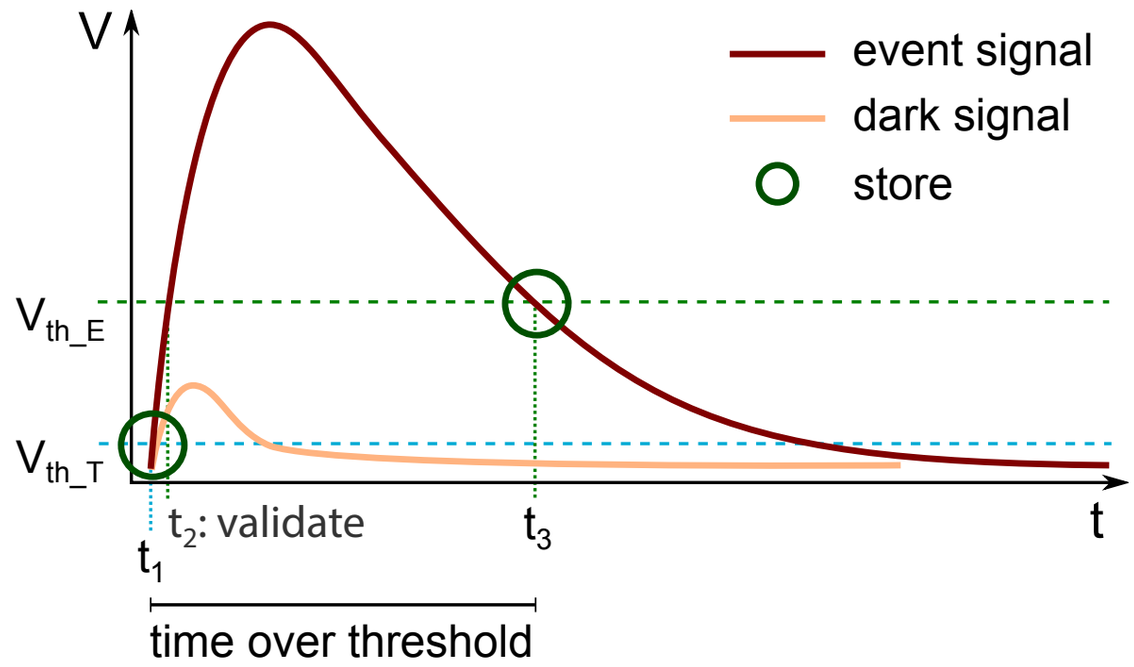
49. PANDA Meeting, MVD Session

Content

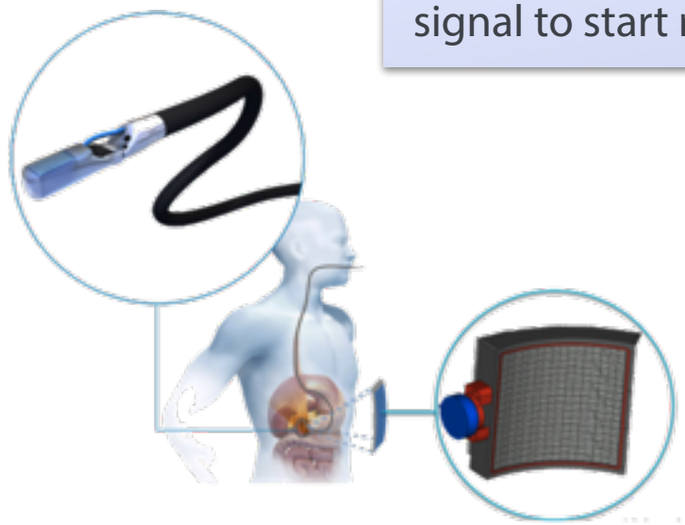
- Concept of the ASIC
- Current Status
  - Analog Front-End (*V. Di Pietro*)
  - Analog TDC (*A. Riccardi*)
  - Digital TDC & GCTRL (*A. Goerres*)
- Conclusion & Outlook

Measurement Concept

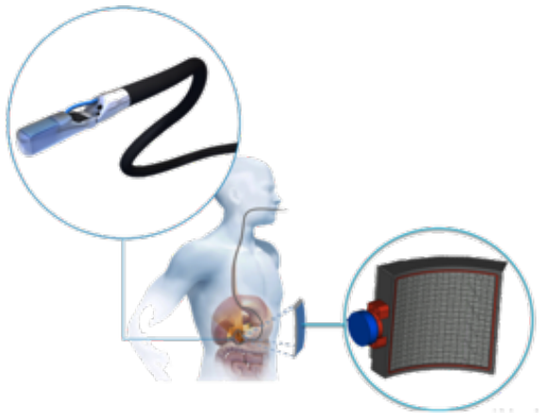
- Free-running, time-based readout
  - Timestamp (50-200 ps)
  - Time over threshold
- Two TDCs per channel
  - Time and energy branch
    (low and high threshold)
  - Energy trigger* (t_2)
    validates time trigger* (t_1)
  - Reduces susceptibility to dark counts
- Concept based on TOFPET ASIC
  - Developed for medical application
  - Readout of SiPM



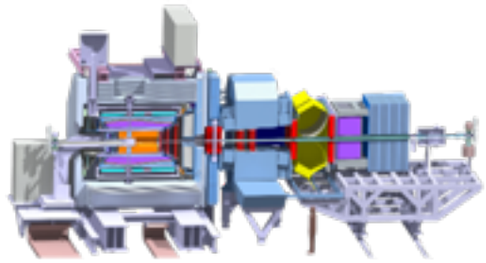
* **trigger:** ASIC internal signal to start readout



From TOFPET to PASTA



TOFPET ASIC v1



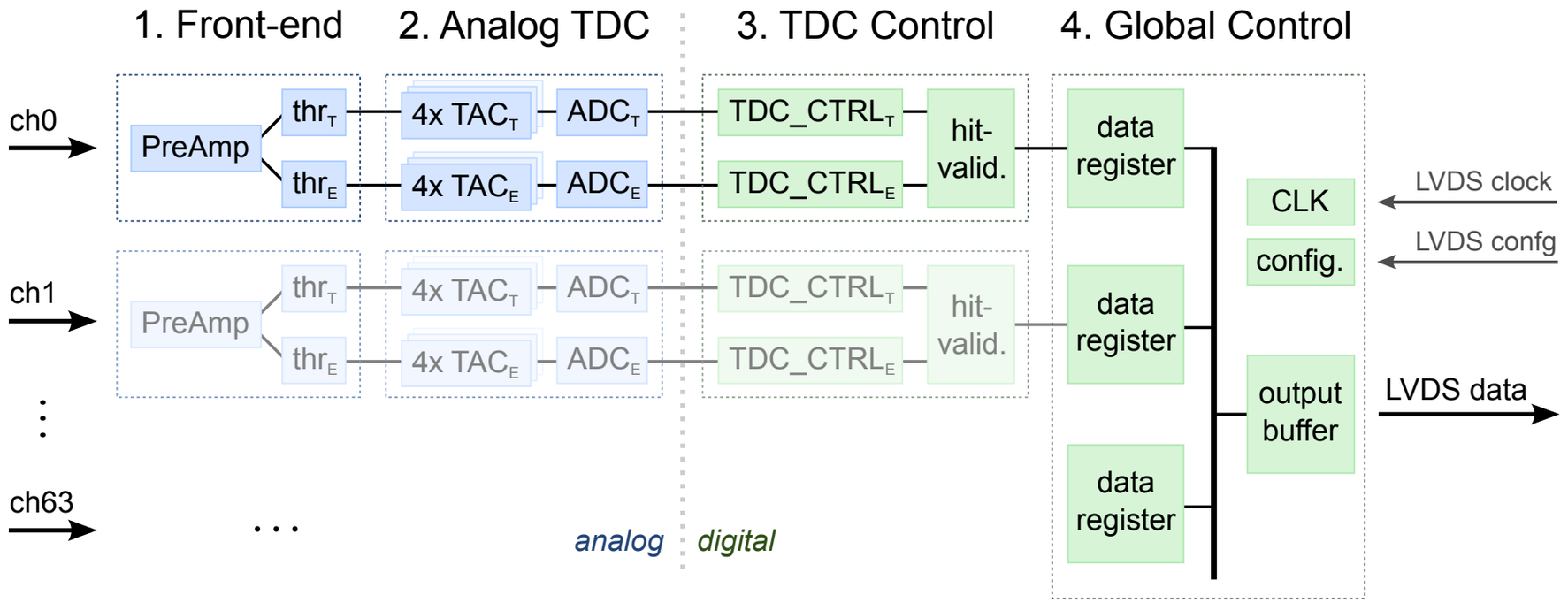
PANDA Strip ASIC

Input capacitance/charge	**SiPM** → 320 pF / 300 pC	**Si strips** → 10-25 pF / 38 fC
Power consumption	7-8 mW/ch	< 4 mW/ch
Channel pitch	104 µm	60 µm
Radiation protection	n/a	100 kGy
Efficiency gap	~ 6% event loss	no event loss
Charge resolution	less important	8 bit dyn. range

Additional changes:

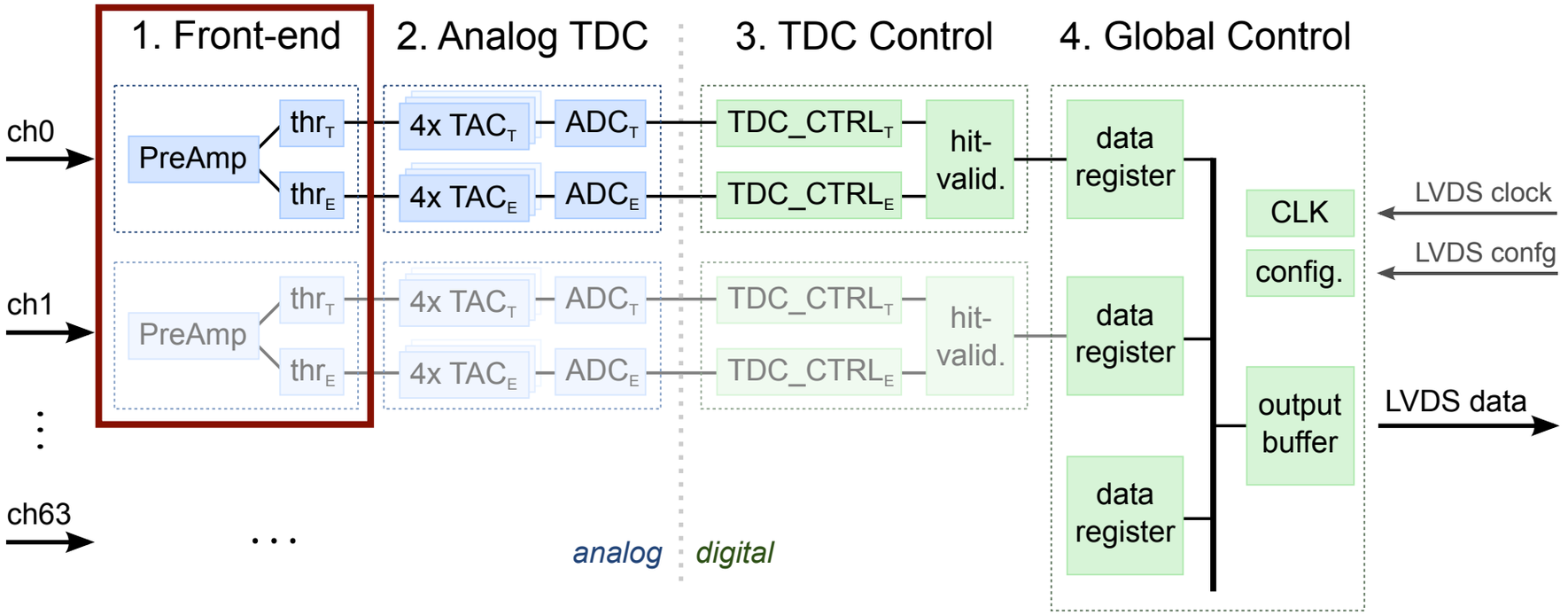
- Switch to area optimized technology
- Rewritten TDC control logic

Components in the ASIC



1. Amplification & discrimination
2. Time interpolation, Wilkinson ADC
3. Control charging & initiate storing
4. Handling configuration & channel data

Components in the ASIC



1. **Amplification & discrimination**
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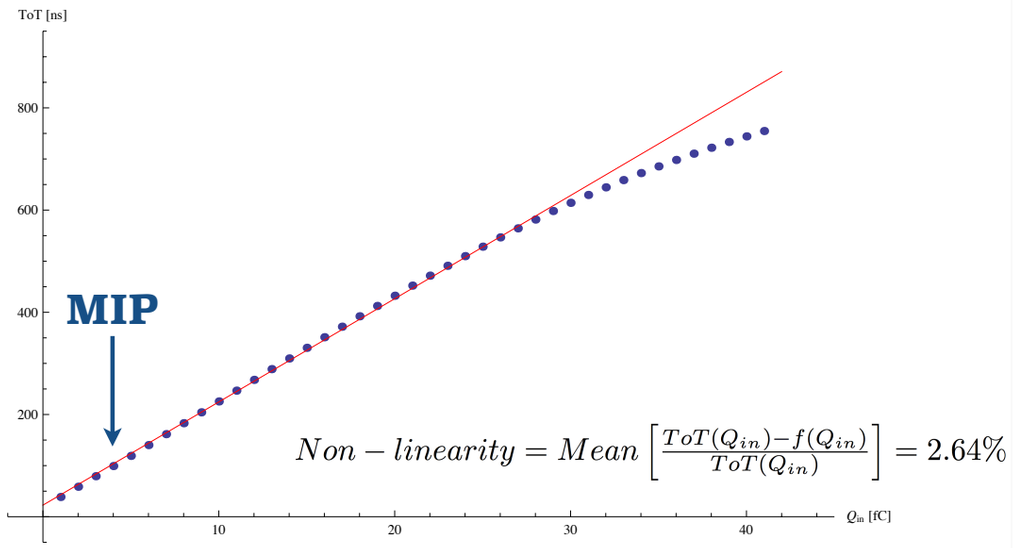
Valentino Di Pietro

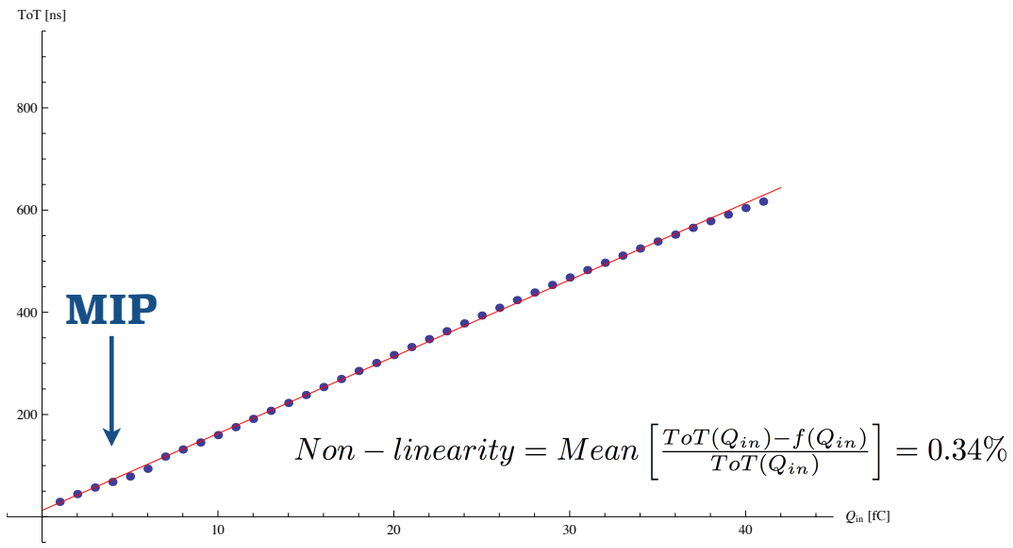
Linearity of the Front-End

pSconf*: Linearity



*pSconf: Configuration for the p-type Strips

nSconf*: Linearity

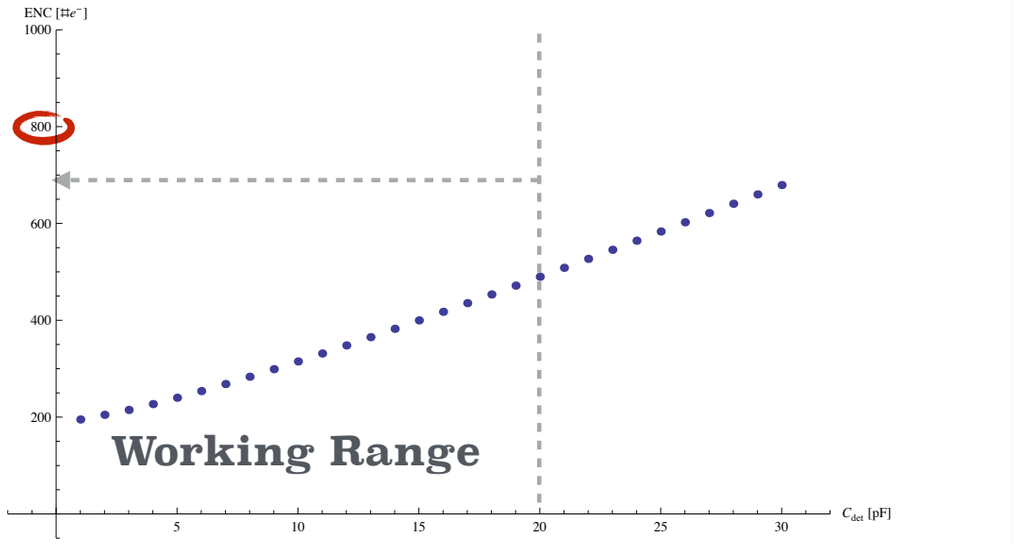


*nSconf: Configuration for the n-type Strips

TOT to charge is mostly linear, rest done with calibration

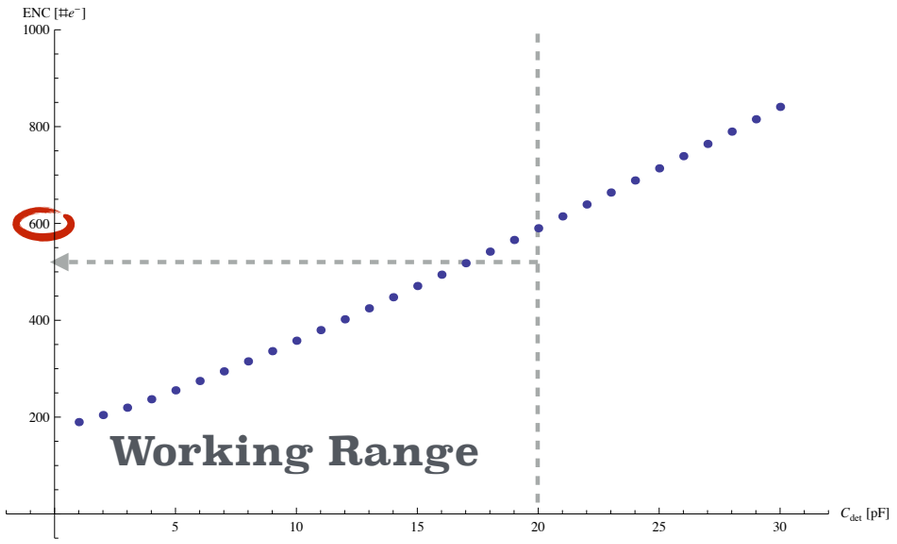
Noise Contribution of the Front-End

pSconf: ENC



Noise @ 25 pF: ~ 600 e⁻

nSconf: ENC



Noise @ 25 pF: ~ 750 e⁻

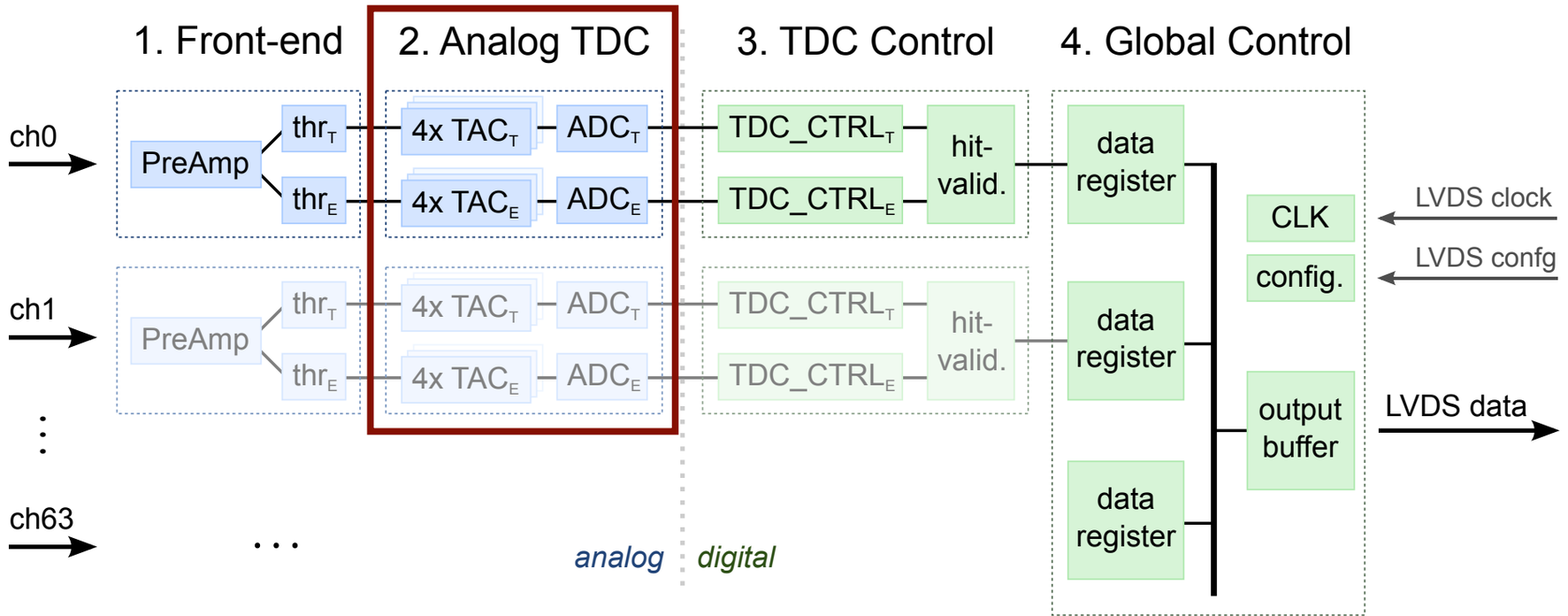
Noise well below requirements

TDR: < 1000 e⁻ @ 25 pF

More Numbers

- Peaking time: 50 ns (fixed but easily adjustable)
- Power consumption: ~ 1 mW/ch

Components in the ASIC



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Alberto Riccardi

Time Interpolation

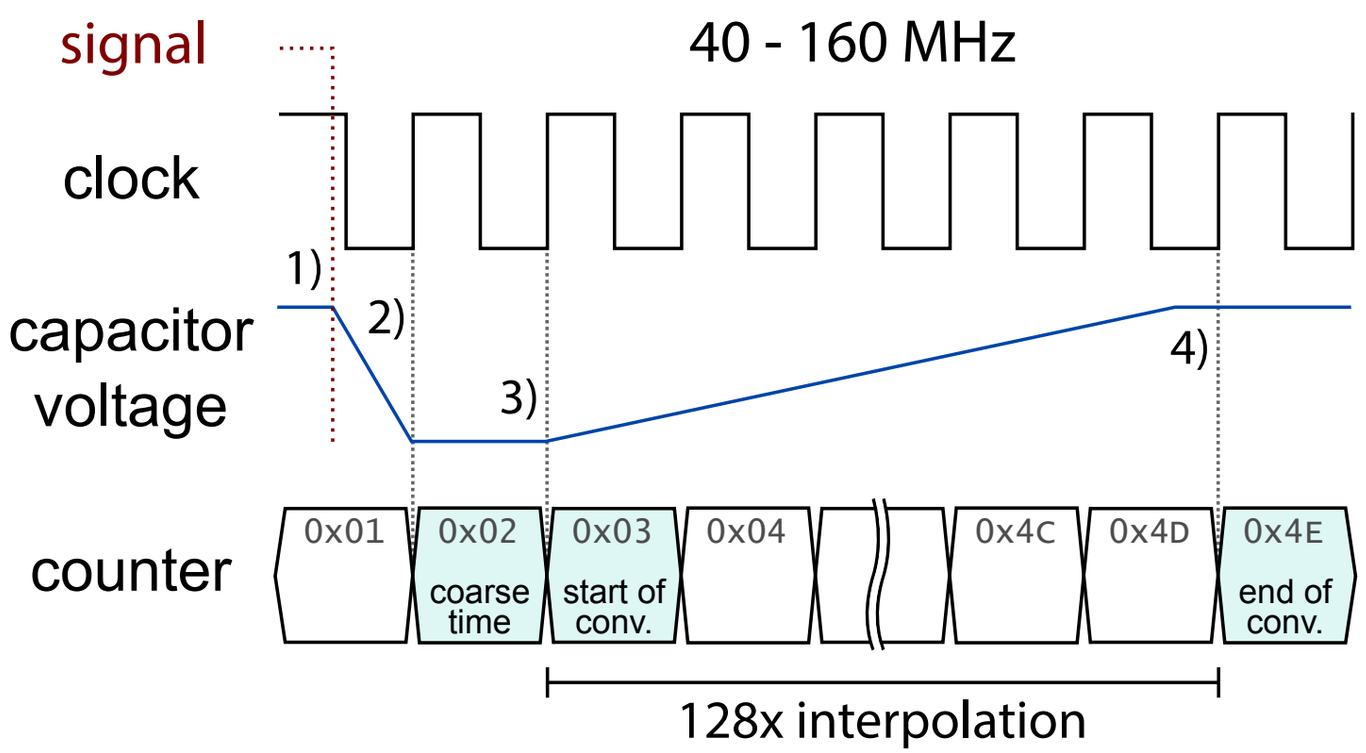
- Interpolate clock interval:

1) Trigger signal from discriminator
   Start discharging I_1

2) Synchronized trigger signal
   Stop discharging
   Store coarse time

3) Conversion logic ready
   Start recharging I_2
   Store start of conversion

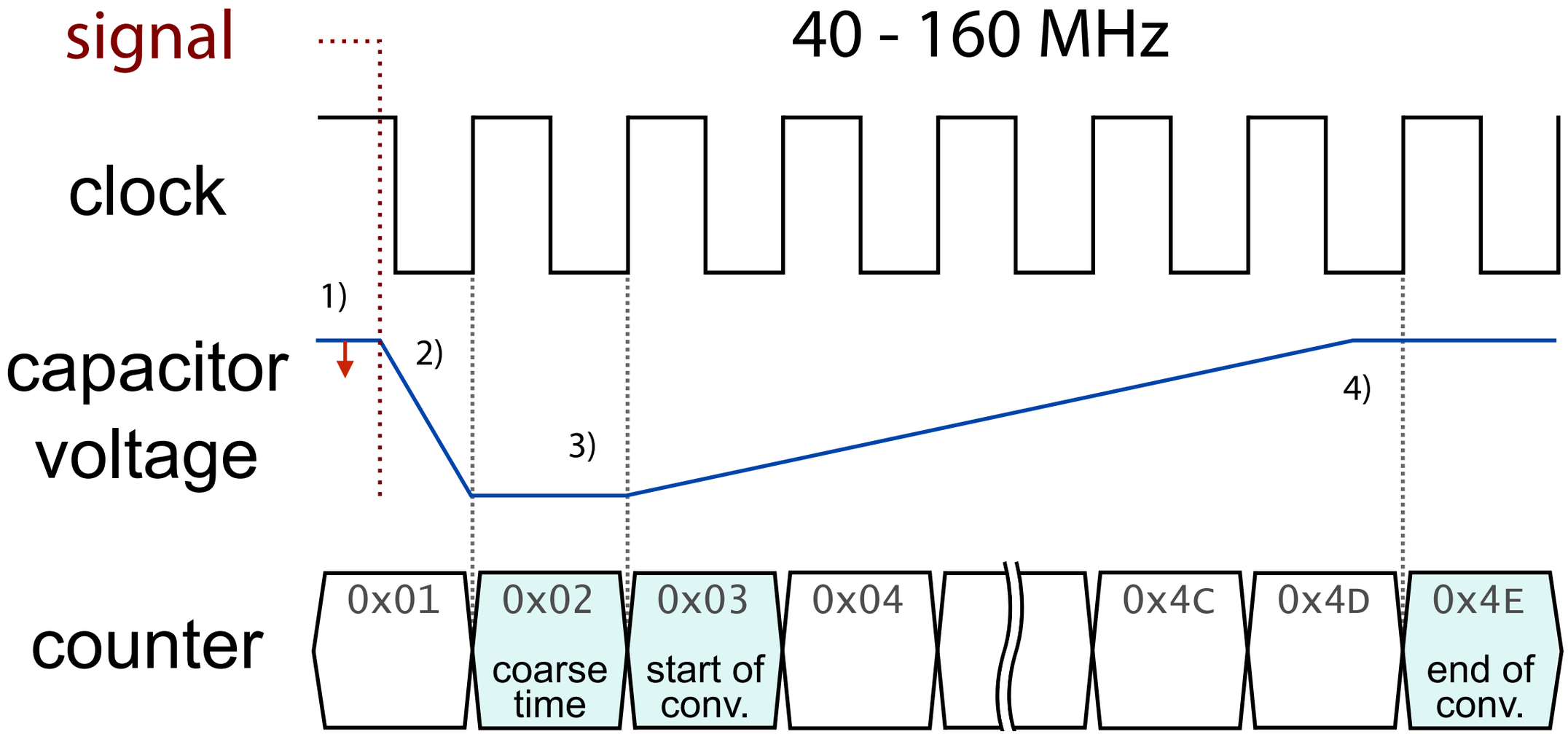
4) Voltage back to reference value
   Stop recharging
   Store end of conversion



Intermediate step 2.5
Transfer charge to 4x larger capacitor

- Yields to 128x interpolation (I_1/I_2)
  ⇒ 50 ps digital resolution at 160 MHz

Refresh Issue of TAC



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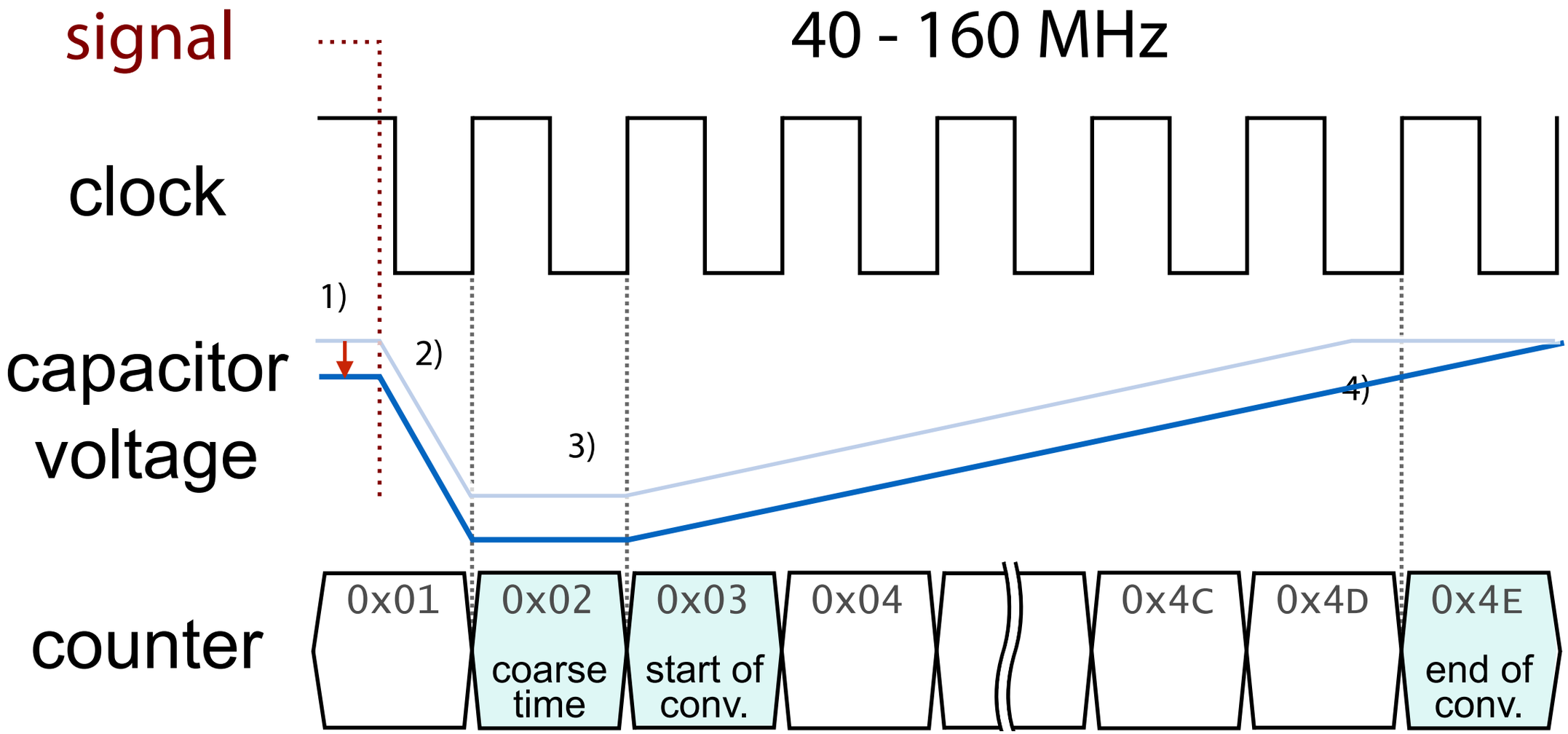

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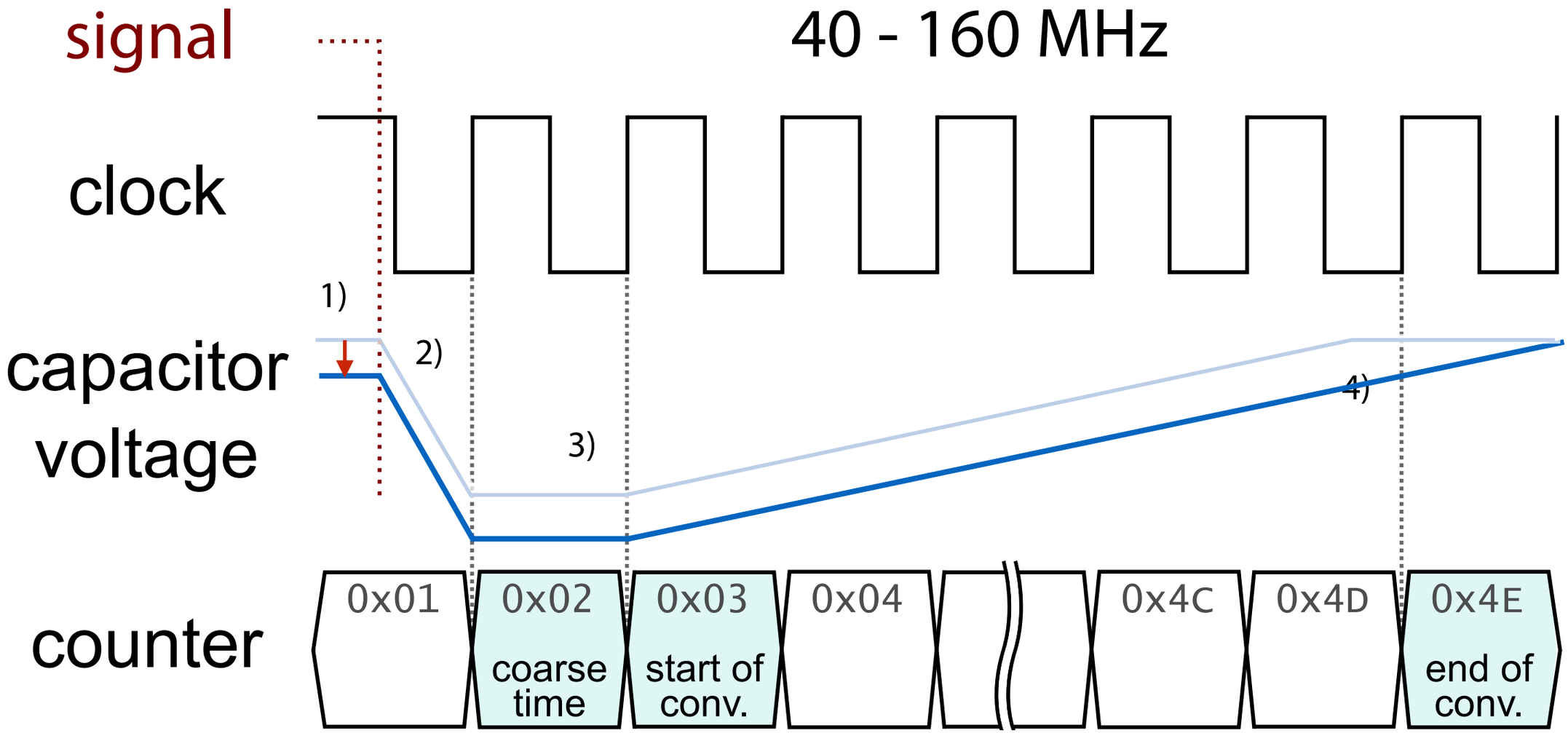
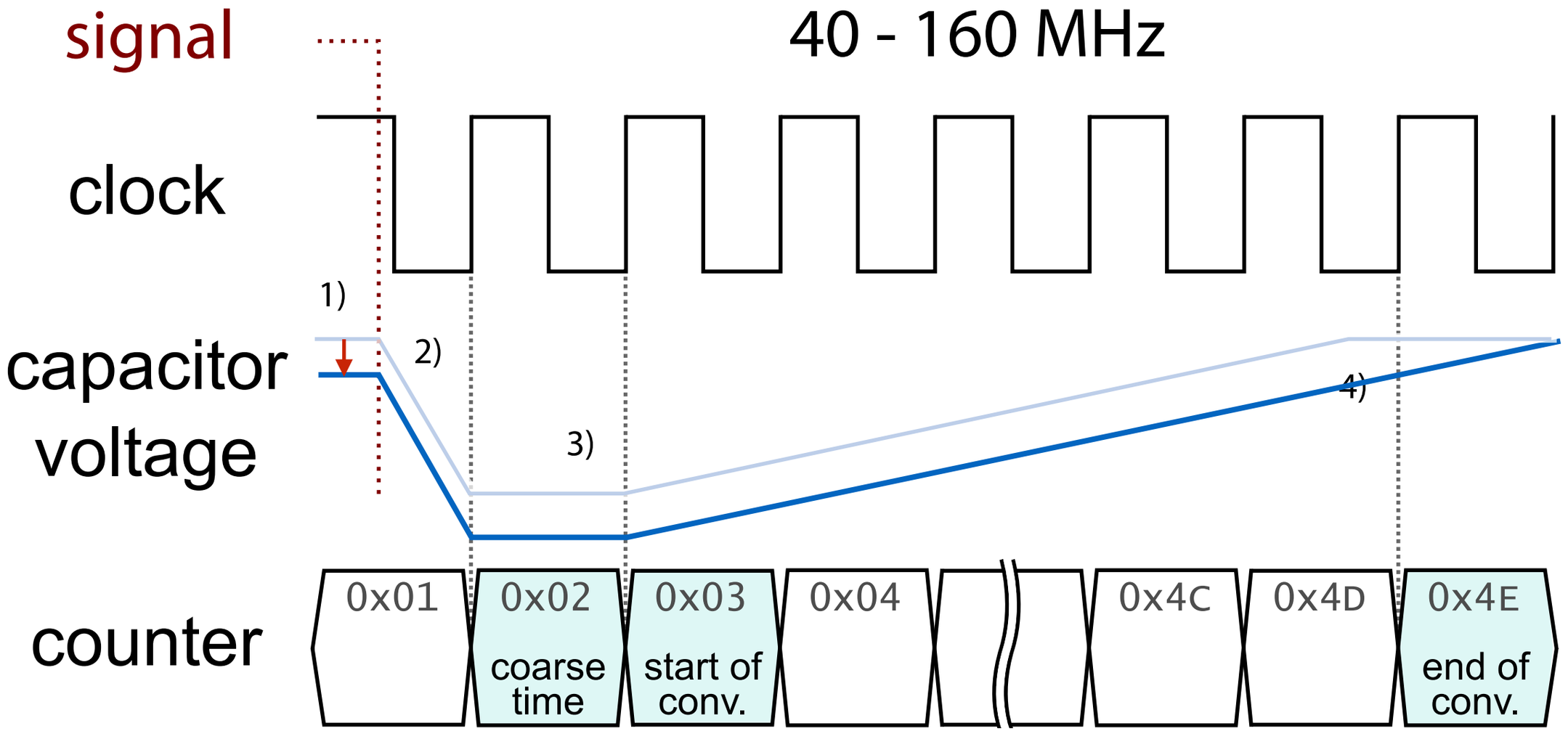


⇒ Reset TAC to ref. level after a while

Refresh Issue of TAC



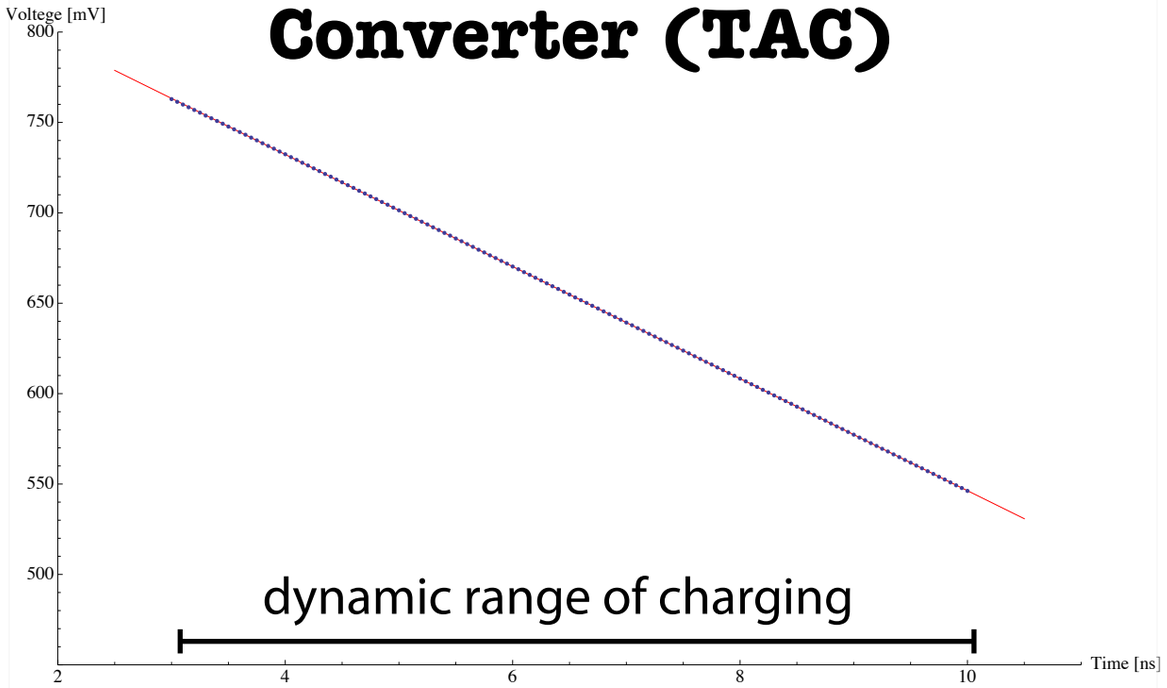
⇒ Reset TAC to ref. level after a while

improved circuit →

New TAC architecture without need of refresh

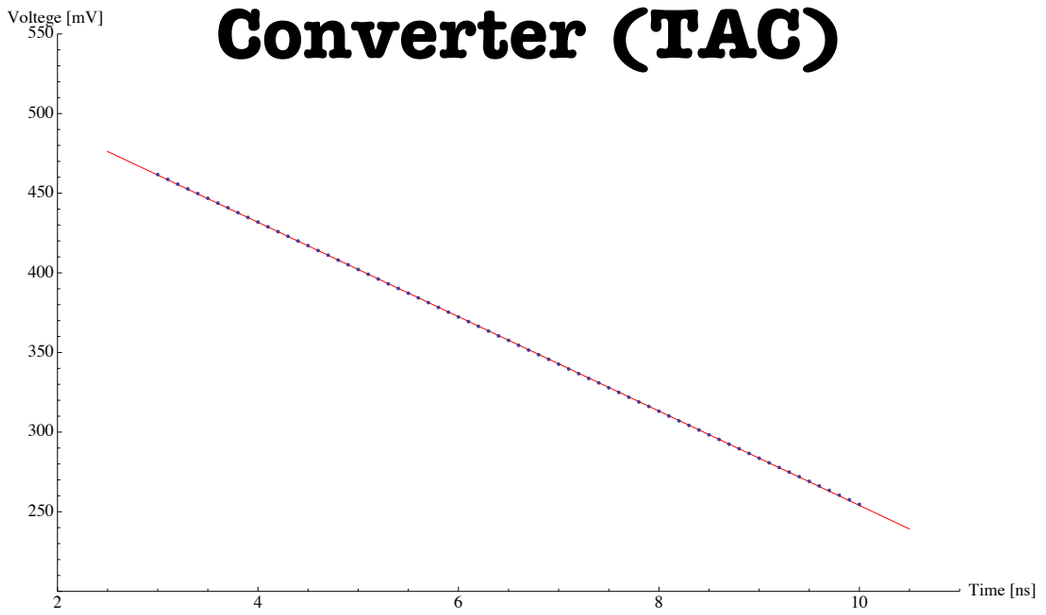
A New TAC for PASTA

Old Time to Amplitude Converter (TAC)



The worst point has 0.5‰ as non linearity

New Time to Amplitude Converter (TAC)

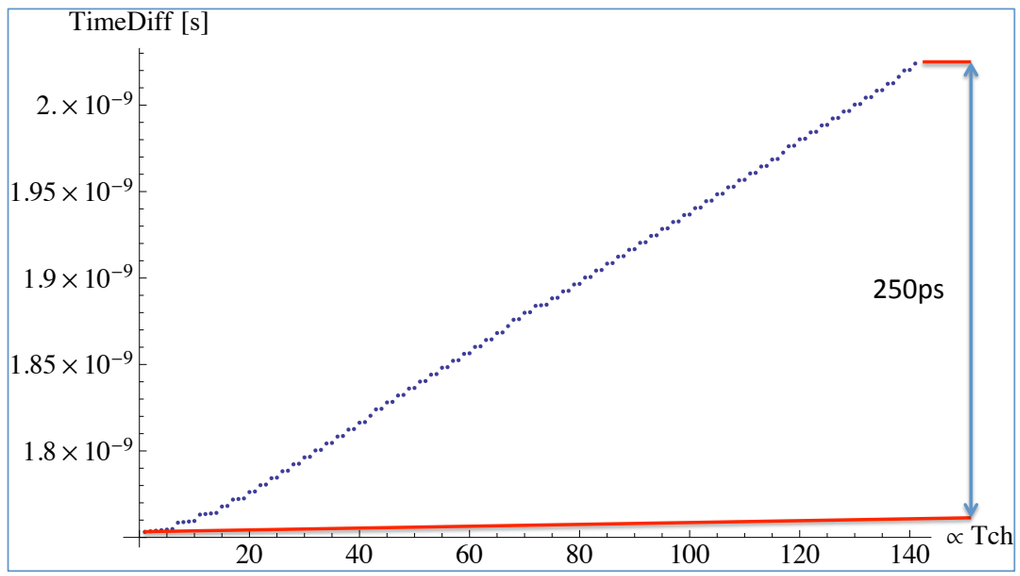


The worst point has 2.4‰ as non linearity

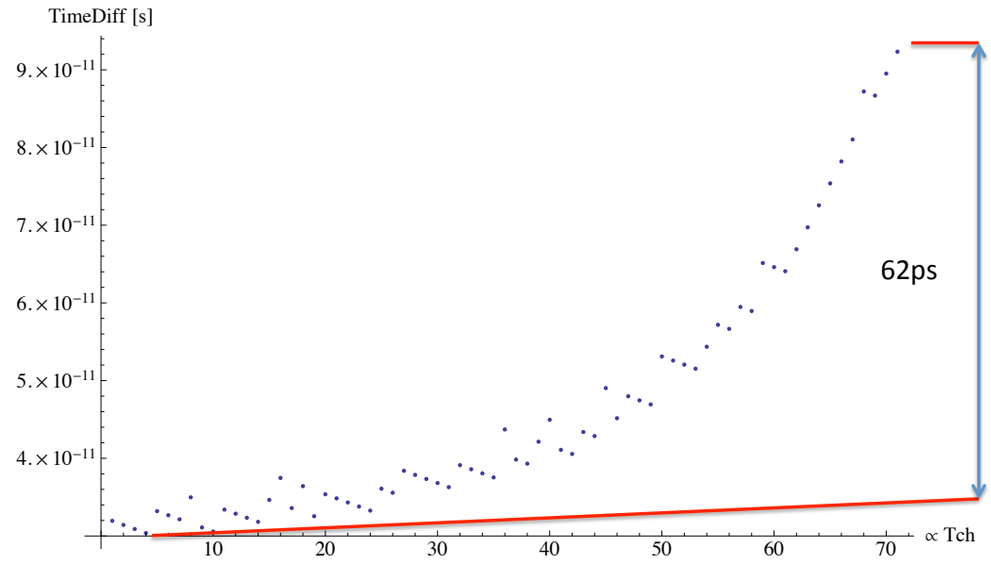
With this structure we can avoide the refresh problem

New TAC is still linear over dynamic range

Error in Time Reconstruction from TAC



In terms of the time we have 1.753ns as offset.



In terms of the time we have 30ps as offset

y axis TimeDiff [s]:
Time of switching to calculated time

x axis Tch: Point number
(left: 50 ps steps, right: 100 ps steps)

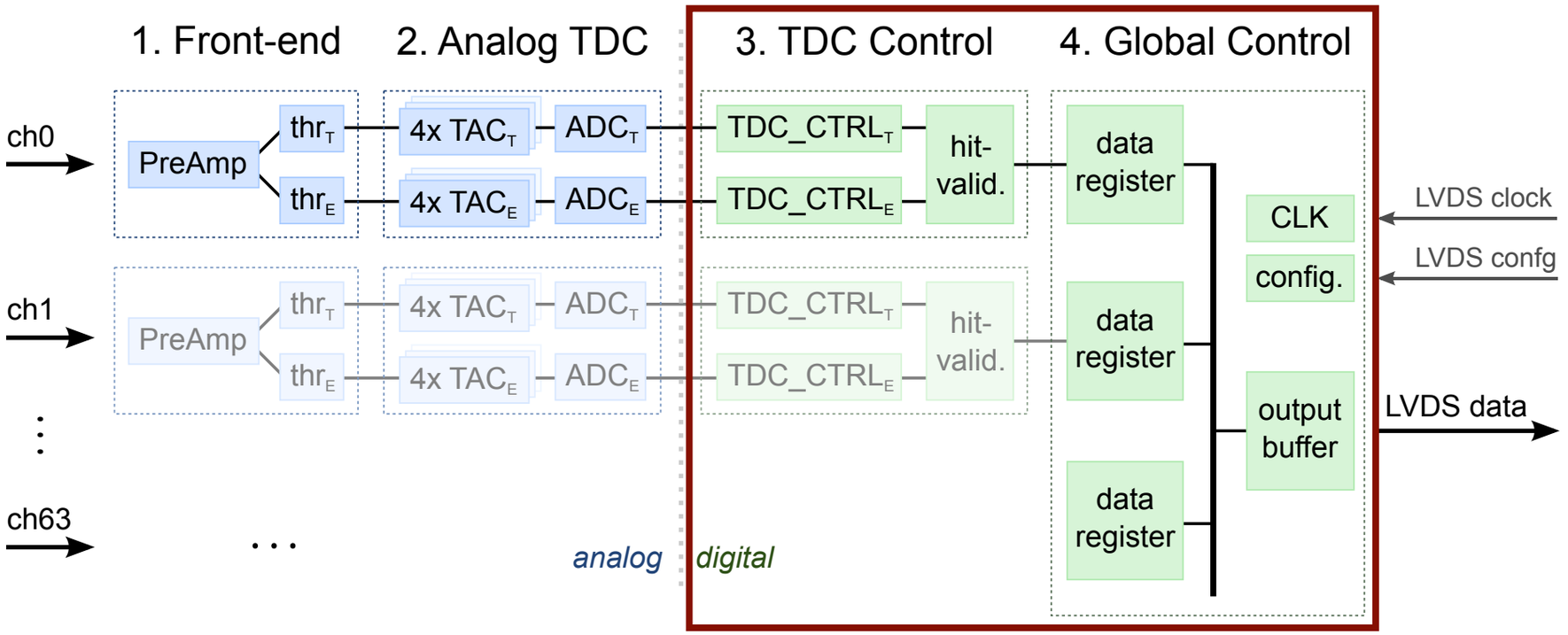
New TAC introduces less error
(250 ps → 62 ps)

More Numbers & Status

- Power consumption: ~ 1 mW/ch

- Current status for both analog parts:
  - Designs finished
  - Simulations of circuits ongoing
    - Influences of component parameters to design
    - Production tolerances of component
  - Layouting starts soon (couple of weeks)

Components in the ASIC



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André Goerres

New TDC Control

Rewritten TDC control code with major simplification:

old: 1100 x 100 µm²

new: 180 x 55 µm²

	TDC_CTRL v1 tech. A	TDC_CTRL v1 tech. B	TDC_CTRL v2 tech. B
Occupancy (1.1 x 0.1 mm	84.8 %	37.0 %	7.2 %
Cells	3155	2850	351
Power (@ 160 MHz)	1.57 mW/ch	1.78 mW/ch	0.08 mW/ch

technology change new TDC control

MVD req.
104→60 µm pitch
8→4 mW/ch

Design review: Feb 2014 ✓

General Work on Digital Part

- Single Event Upset (SEU) protection
  - TDC_CTRL: finished & tested
  - GCTRL:
    - Critical registers ~70% protected
    - Information on occurred SEU needs to be collected (counter)

- Refresh control per TAC (instead globally)
  - Issue refresh = reset without event (configurable delay)

- Combine digital blocks
  - Avoid issues with interchanged signals (timing, load)
  - Simpler merging of designs (just one block)

Generator for VHDL Test Bench

Digital part needs validation

- **Test bench**
  - Logic behavior of GCTRL and TDC_CTRL
  - Analog behavior emulated
    - Charge proportional to time, gets transferred, …
  - Input: simulated output of discriminators (text file)

- New* tool to **generate input**
  - Written in python
  - Internally: voltage input to discriminator
    - Source: analog simulation of front-end (V. Di Pietro)
  - Output:
    - Wait time for next discriminator change of state

Code available at: https://github.com/Nepomuk/ASIC_generator

* based on idea of R. Bugalho (LIP Lisbon)

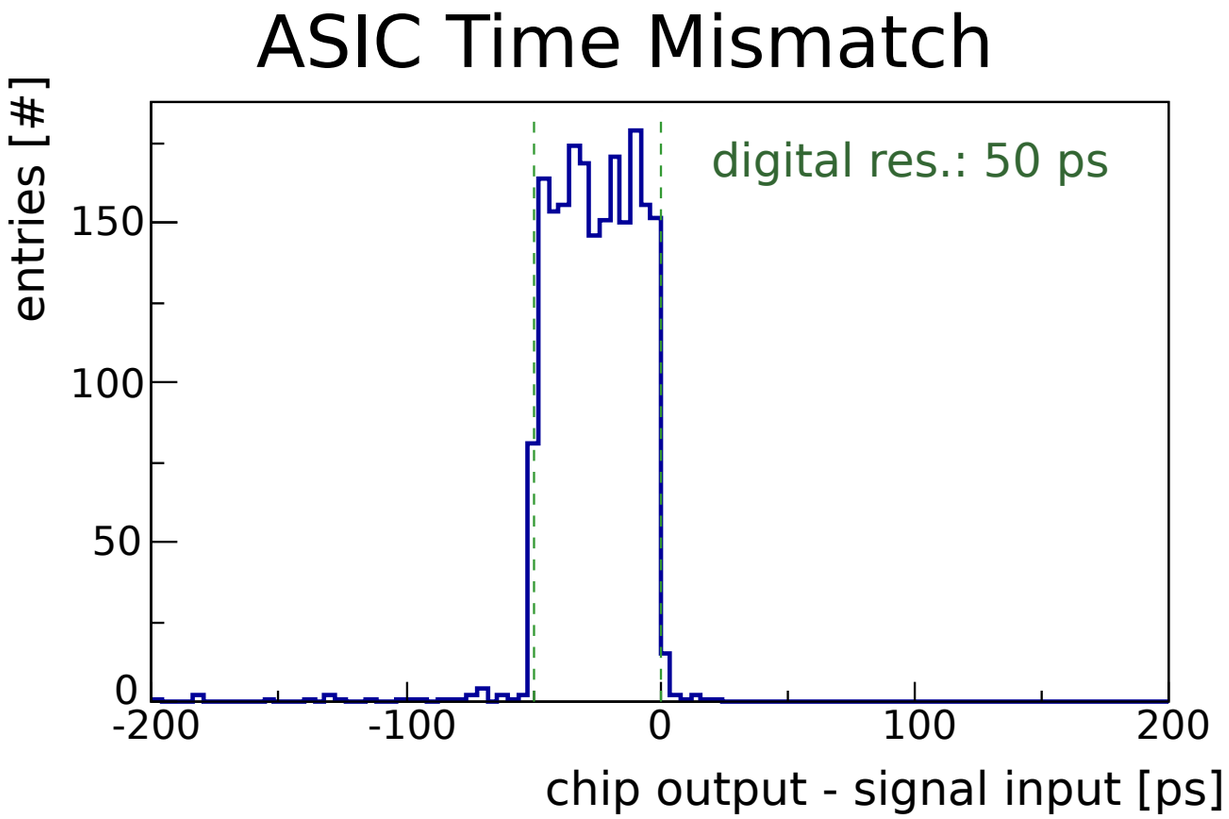
time of arrival	time over threshold
0.000006520456	0.000000101280
0.000030262739	0.000000104310
0.000035721378	0.000000081840

↓

```
000006520900
000000100830
000023641450
000000103860
000005354740
000000081430
```

Check Simulated ASIC Output

- Simulate sequence of hits
- Compare original timestamp (*signal input*) with simulation (*chip output*)
- Expected mismatch



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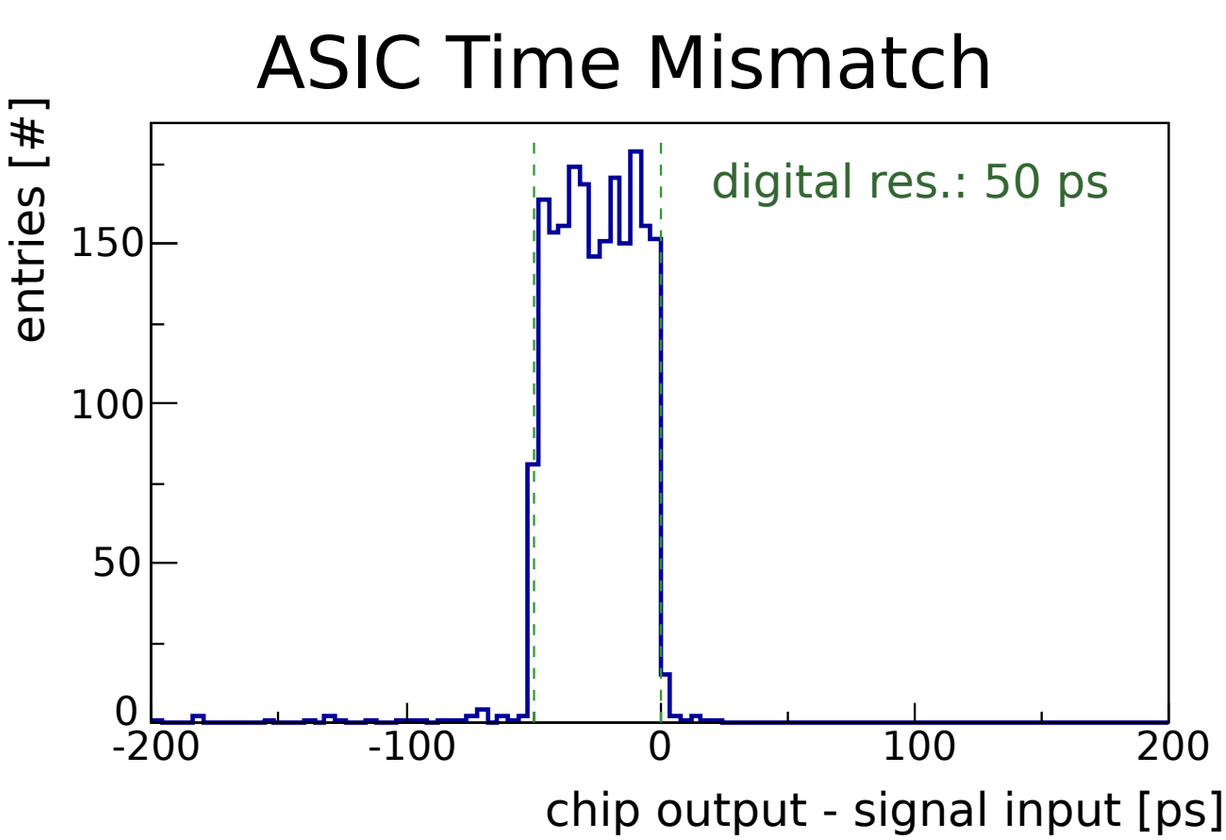
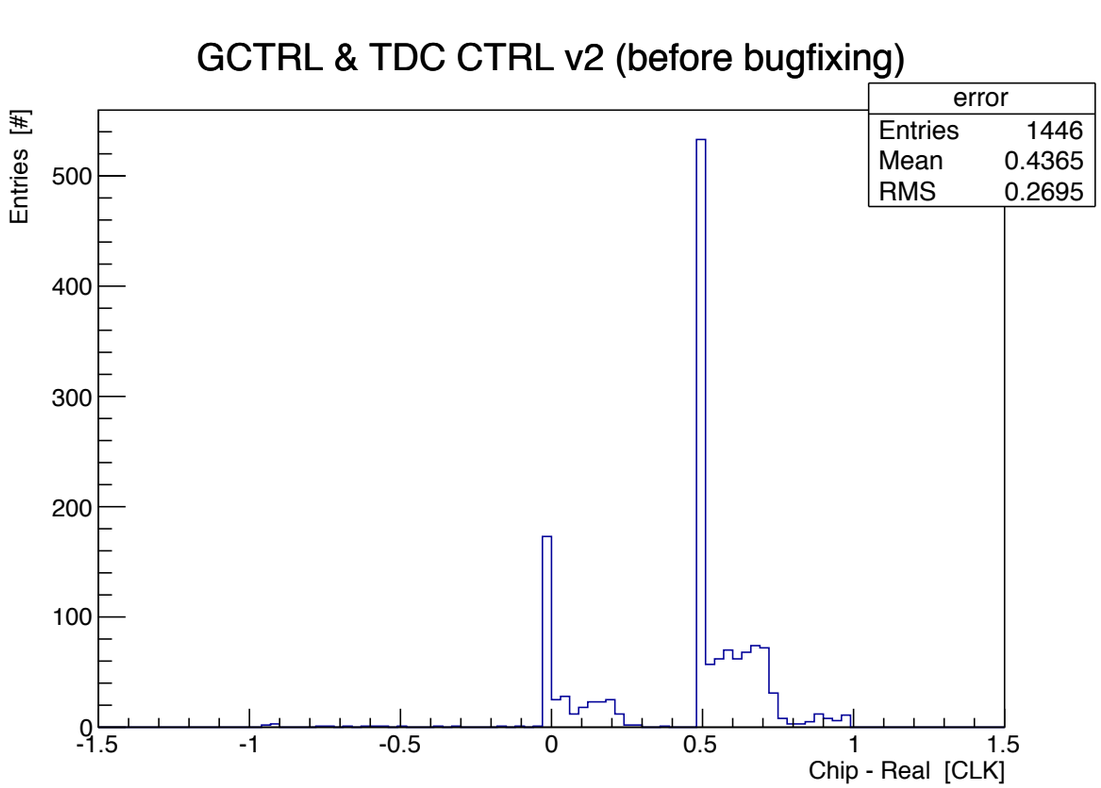
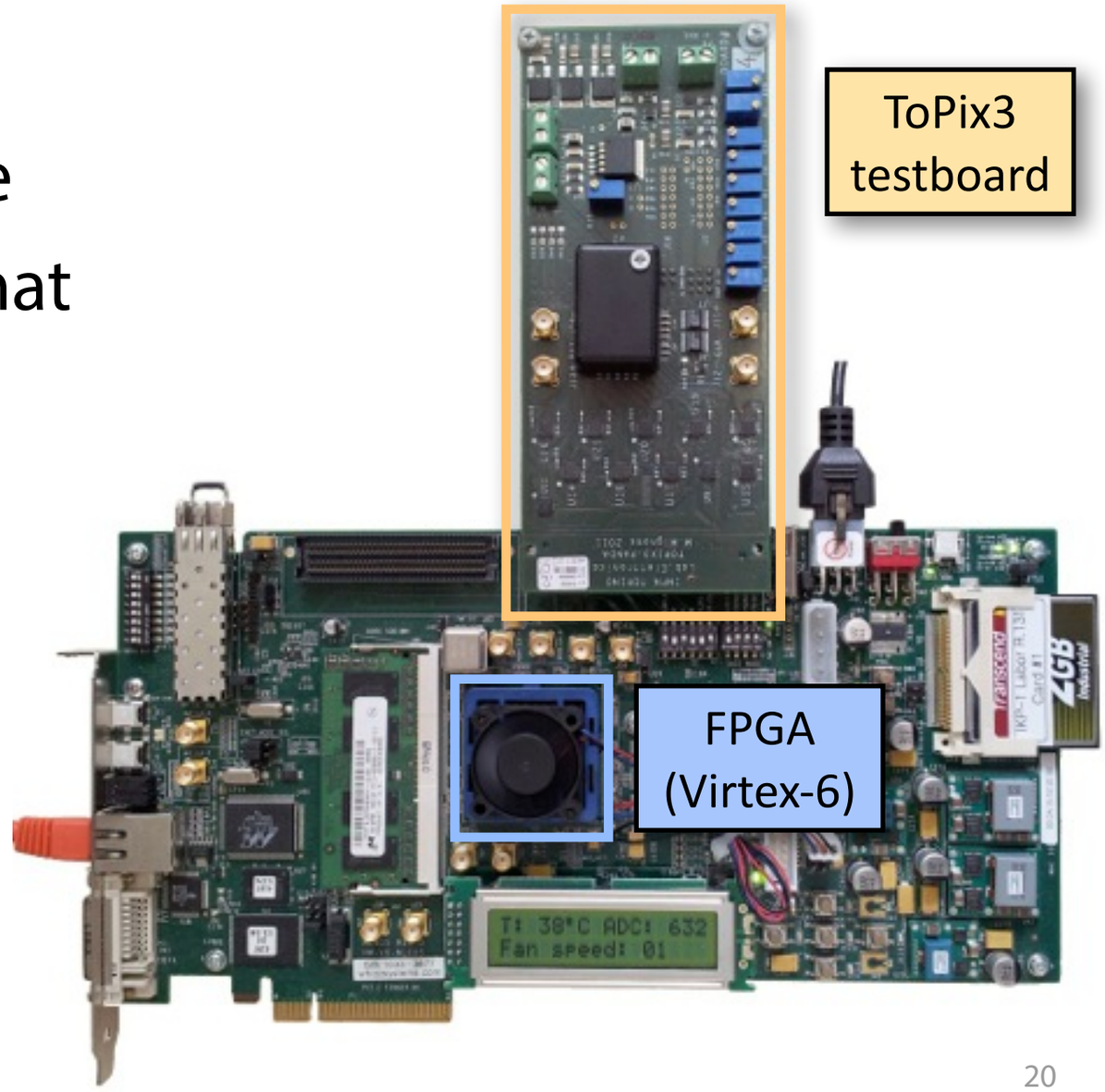




Jülich Readout System for PASTA

- Flexible readout system for front-end chips
  - Based on FPGA (Virtex-6), ML605 board from Xilinx
  - Connection to PC via Ethernet
- Preparation for PASTA starting
  - Prepare configuration interface
  - Readout with known data format
- Summer student in Jülich:
  Aaron Mahler



PC ⟷ comm. link: **UDP** over ETH ⟷ ML605 (ToPix#, PASTA)

Conclusion & Outlook

- Analog front-end meets noise req. (< 1000 e^- ENC)
- Analog TDC without refresh and less timing error
- Design of digital TDC control simplified
- Area & power consumption reduced to meet PANDA req.

- Layout analog front-end and TDC (next weeks)
- Merge designs & submit chip (this year)
- Test first PASTA version
  - Readout system in preparation

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People Involved

A. Goerres[1], A. Mahler[1], G. Mazza[2], V. Di Pietro[2,3], A. Riccardi[2,3], J. Ritman[1], A. Rivetti[2], M. D. Rolo[2,4], R. Schnell[3], T. Stockmanns[1], H.G. Zaunick[3]

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Thank you!

a.goerres@fz-juelich.de

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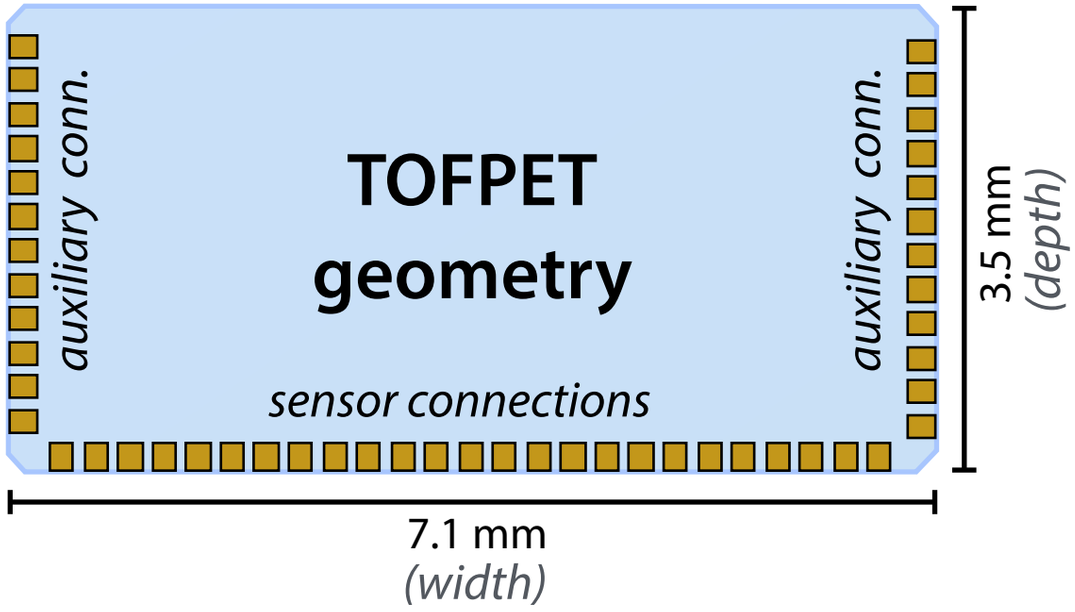
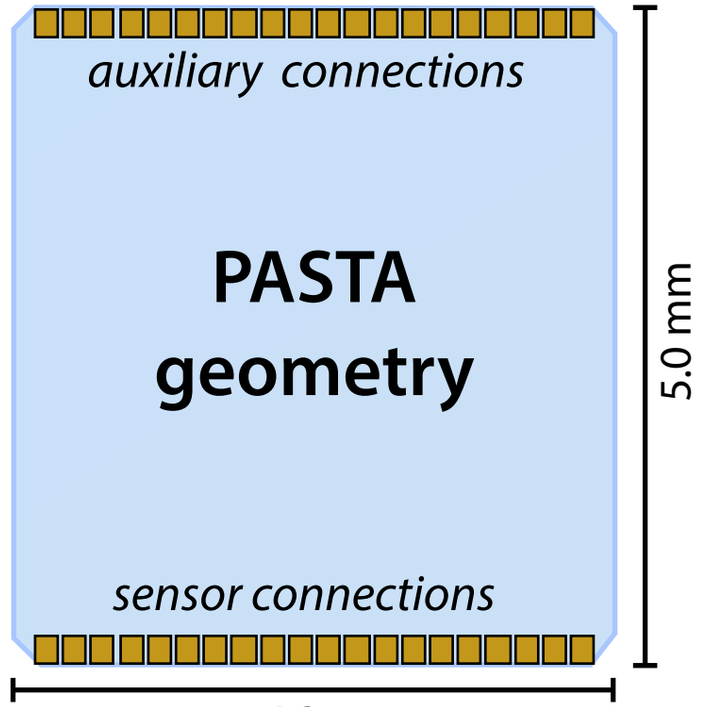
BACKUP

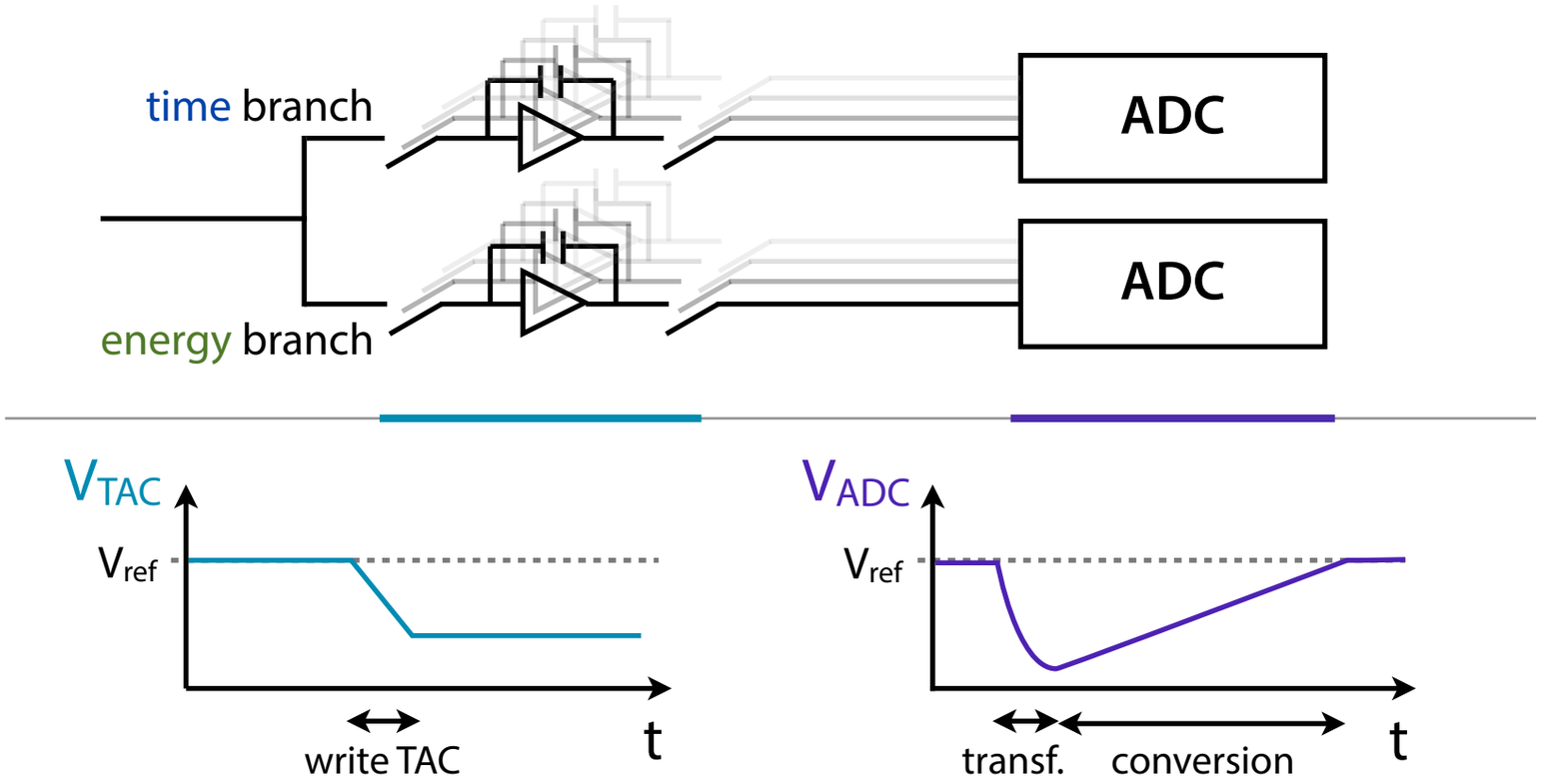
Geometrical Boundaries





- Footprint: $7.1 \times 3.5\ mm^2 \rightarrow 4.2 \times 5.0\ mm^2$
  ($25\ mm^2 \rightarrow 21\ mm^2$)
- Smaller channel pitch: 102 µm → 60 µm
- Position of bonding pads: front, sides → front, back

Time-to-Digital Converter



- Two stages: buffer and convert signal
  - Buffering: discharge a capacitor (TAC)
    - **Start**: threshold; **End**: next edge of clock*
  - Transfer to **4x** larger capacitor, linearly recharge with **32x** smaller current (*Wilkinson ADC*)
- Time interpolation by factor **128** (50 ps @ 160 MHz)
  - Conversion takes ~ 3 µs → TAC buffer **multiplicity of 4**

ADC: Analog to Digital Converter
TAC: Time to Analog Converter

*: Dynamic range 0-2.5 clock cycles

stage 1
front-end

stage 2
analogue TDC

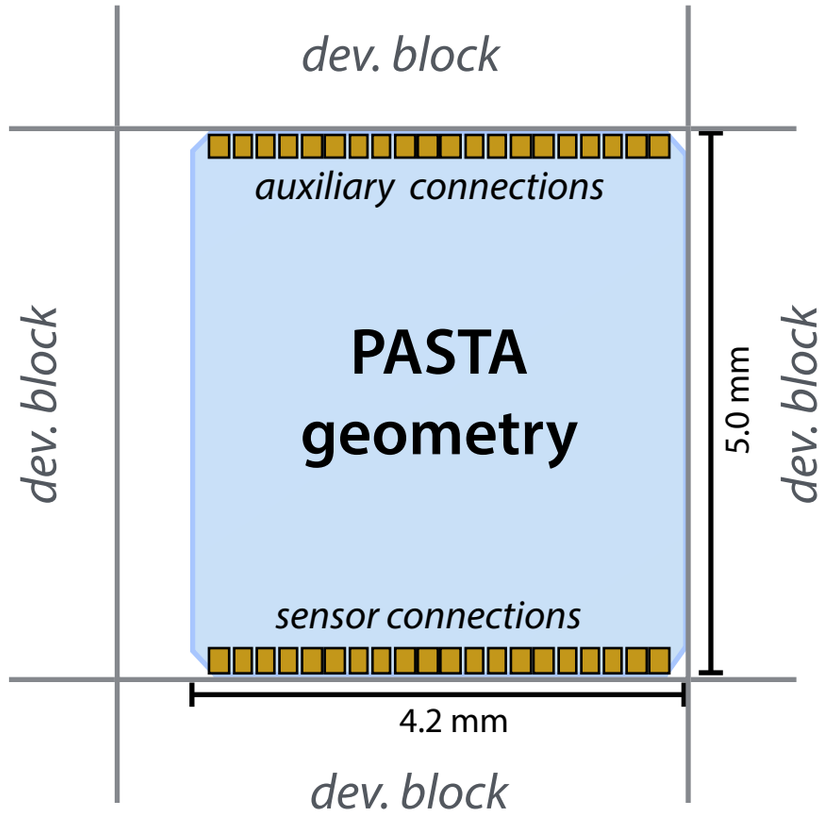
stage 3
TDC CTRL

stage 4
global CTRL

Change of Technology

- Switch towards area optimized technology (tech. B)
  - Supports the reduction of the pitch
  - Structure size: 130 nm, tech. A → 110 nm, tech. B
  - Less development costs
    - Shared wafer instead of full engineering run

- Typical changes in digital project
  - Area occupation: ↘ 30-50 %
  - Power consumption: ↗ 10-20 %



Situation for Wedged Sensors

- Original design:
  - 512 channels per sensor, 67.5 µm pitch
  - readout every channel

⇒ 8 ASICs with < 50 µm input pitch

- New concept:
  - 768 channels per sensor, 45 µm pitch
  - readout every second channel

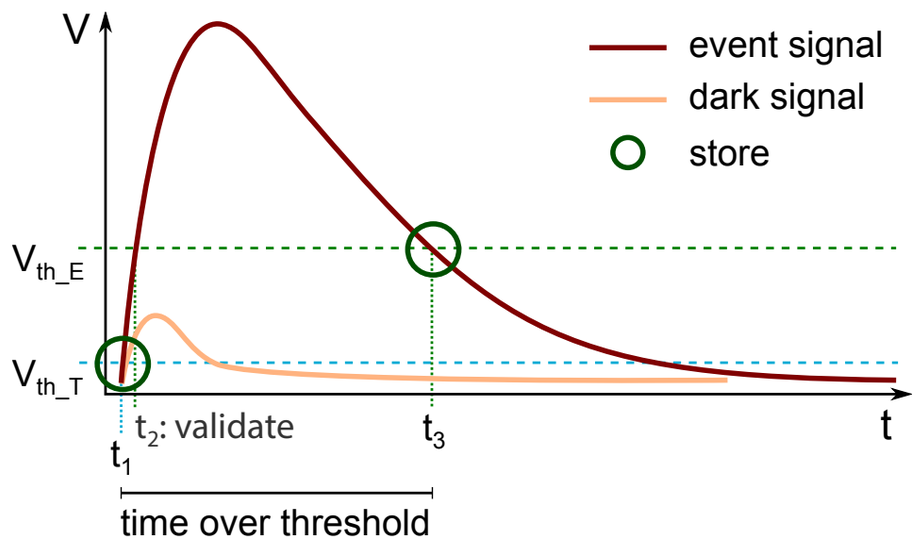
⇒ 6 ASICs with 60 µm input pitch

- Simulations (H.-G. Zaunick)
  - Spatial resolution of floating channel to direct readout: Worse by ~20 %

r/o pitch (µm)	worst RMS resolution $\frac{p}{\sqrt{12}}$ (µm)	nr. of intermediate strips	SNR	spacial resolution RMS (µm)
65	18.8	0	10	16.09 ± 0.02
			16	13.08 ± 0.02
			25	10.63 ± 0.01
130	37.5	0	10	34.70 ± 0.05
			16	31.64 ± 0.04
			25	29.28 ± 0.04
130	37.5	1	10	24.92 ± 0.03
			16	16.13 ± 0.02
			25	12.11 ± 0.02

Further Small Improvements

- Internal clock divider (1, ½, ¼)
  - Reduce power consumption
  - Digital resolution: 50–200 ps
- Refresh control per TAC (instead globally)
  - TAC capacitors lose charge due to leakage
    - → Fine time measurement distorted
  - Issue refresh = reset without event (configurable delay)
- More flexible readout initialization
  - Rising + falling edge
  - Both rising edge
  - Test pulse
  - …



WRITE_CTRL – trigger_select

Purpose: get a trigger to start TDC

Generate Different Trigger

- Rising edge of DOT
- Rising edge of DOE
- Falling edge of DOE
- Rising edge of Test Pulse
- Falling edge of Test Pulse

→

Select Trigger

Multiplexer to get:

- TRIG_T (default: re_DOT)
- TRIG_E (default: fe_DOE)

3 bit config. multiplexer

↓

Start charging of TAC

→

Create Synchronous Signal

Take TRIG_x and feed it to synchronization chain

Output: TRIG_xS

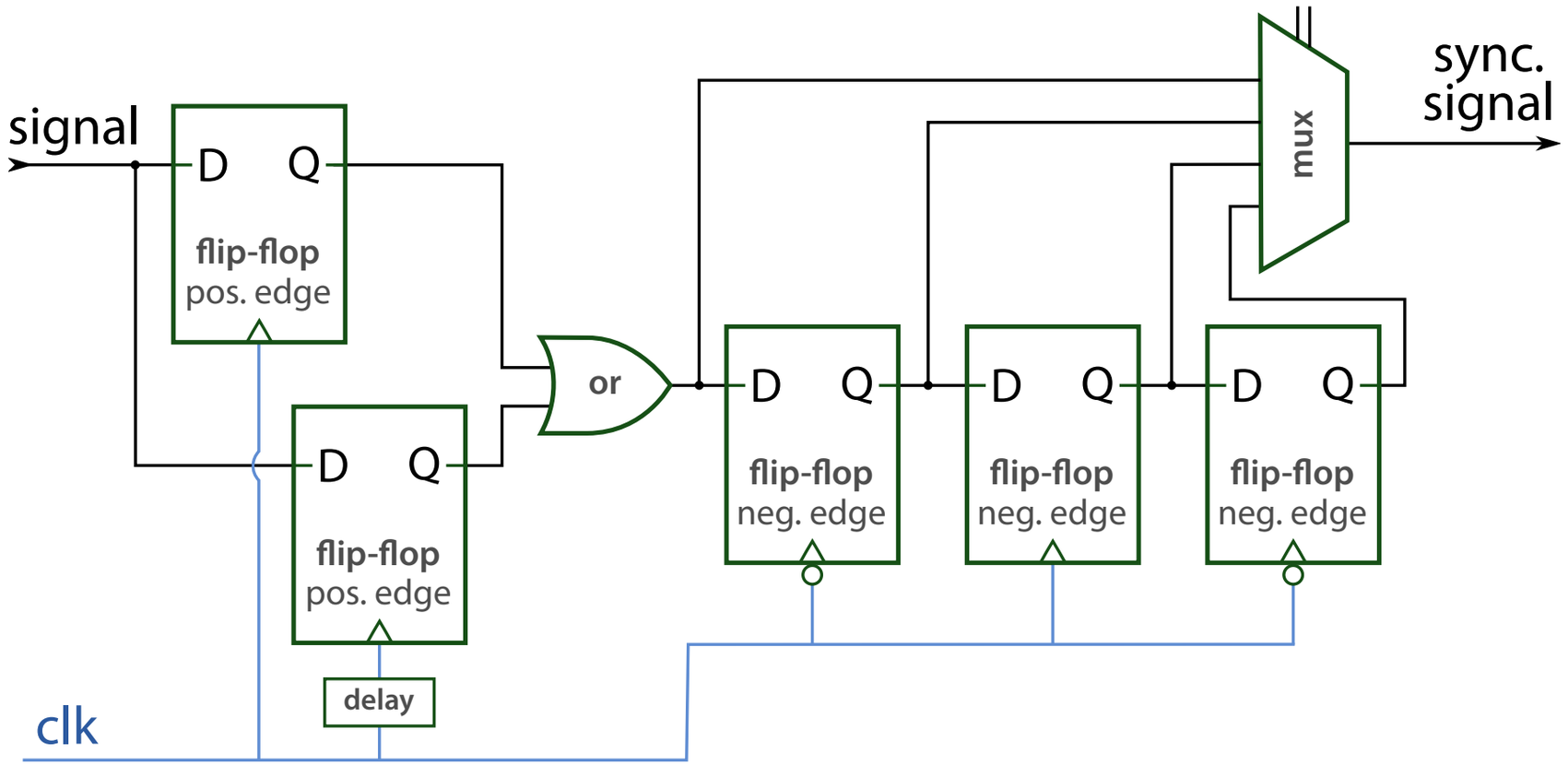
↓

Stop charging of TAC

Latch coarse time

Switch TAC if finished (TAC_SELECTOR)

Synchronization Chain



- Asynchronous → synchronous signal
- Chain lowers probability of metastable output
- Two input flip-flops removes timing violation

Parameter Comparison

TOFPET

Parameter	Value
Number of channels	64
Clock frequency	80 – 160 MHz
Dynamic range of input charge	**300 pC**
SNR (Q_{in} = 100 fC)	> 20-25 dB
Amplifier noise (in total jitter)	< 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. ampli
Power	**< 10 mW per channel**

MVD TDR

Parameter	Value	Remarks
Geometry		
Width	≤ 8 mm	
Depth	≤ 8 mm	
Input pad pitch	≈ 50 µm	
Pad configuration	lateral pads occupied only for diagnostic functions, should be left unconnected for final setup	
Channels per front-end	$2^6 \ldots 2^8$	default: 128 channels
Input Compliance		
Sensor capacitances, Fully depleted sensor		
	< 10 pF	rect. short strips
	< 50 pF	rect. long strips (with ganging)
	< 20 pF	trapezoidal sensor
Input polarity	either	selectable via slow control
Input ENC	< 800 e^-	$C_{sensor} = 10$ pF
	< 1,000 e^-	$C_{sensor} = 25$ pF
Signal		
Fynamic range	240 ke$^-$ (≈38.5 fC)	
Min. SNR for MIPS	12	22,500 e^- for MIPs in 300 µm silicon, guaranteed within lifetime
Peaking time	≈ 5 . . . 25 ns	typical Si drift times
Digitisation resolution	≥ 8 bits	
Power		
Overall power dissipation	< 1 W	assuming 128 channels per front-end
Dynamical		
Trigger	internally generated	when charge pulse exceeds adjustable threshold value
Time stamp resolution	< 20 ns	
Dead time / ch	< 6 µs	baseline restored to 1%
Overshoot recovery time / ch	< 25 µs	
Average hit rates / ch		derived from simulations at a beam momentum of 15 GeV/c
(poissonian mean)		
Hot spots	9,000 s^{-1}	$\bar{p}p$
	40,000 s^{-1}	$\bar{p}Au$
Average occupancy	6,000 s^{-1}	$\bar{p}p$
	30,000 s^{-1}	$\bar{p}Au$
Interface		
Slow control	any	low pin count, e.g. I^2C
Data	sparsified data	

Hamming Code

- Bit positions 2^x: parity bits
  - Rest: data bits
- Parity bits cover data bits, which have bit pos. 2^p set

Bit position		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Encoded data bits		**p1**	**p2**	**d1**	**p4**	**d2**	**d3**	**d4**	**p8**	**d5**	**d6**	**d7**	**d8**	**d9**	**d10**	**d11**
Parity bits	**p1**	X		X		X		X		X		X		X		X
	p2		X	X			X	X			X	X			X	X
	p4				X	X	X	X					X	X	X	X
	p8								X	X	X	X	X	X	X	X