Data Acquisition and Event Filtering



PANDA Physics

- HADRON SPECTROSCOPY
 - CHARMONIUM
 - GLUONIC EXCITATIONS
 - OPEN CHARM
 - STRANGE AND CHARMED BARYONS
- NUCLEON STRUCTURE
 - GENERALIZED
 DISTRIBUTION
 AMPLITUDES (GDA)
 - DRELL-YAN
 - ELECTROMAGNETIC FORM FACTORS
- HYPERNUCLEAR PHYSICS
- HADRONS IN THE NUCLEAR MEDIUM

FAIR/PANDA/Physics Book

Physics Performance Report for:

PANDA

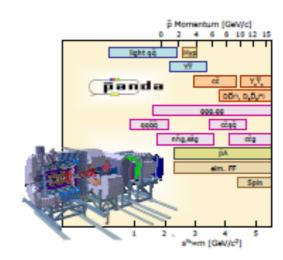
(AntiProton Annihilations at Darmstadt)

Strong Interaction Studies with Antiprotons

PANDA Collaboration

To study fundamental questions of hadron and nuclear physics in interactions of antiprotons with nucleons and nuclei, the universal PANDA detector will be build. Gluonic excitations, the physics of strange and charm quarks and nucleon structure studies will be performed with unprecedented accuracy thereby allowing high-precision tests of the strong interaction. The proposed PANDA detector is a state-of-theart internal target detector at the HESR at FAIR allowing the detection and identification of neutral and charged particles generated within the relevant angular and energy range.

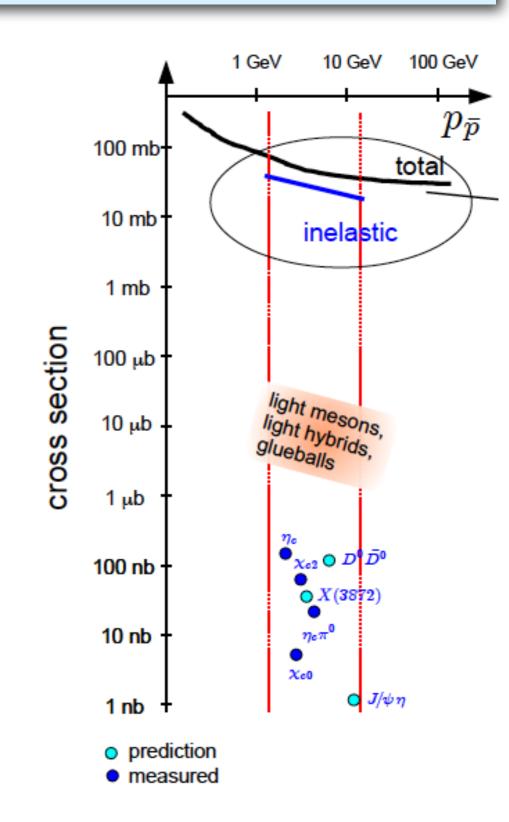
This report presents a summary of the physics accessible at PANDA and what performance can be expected.



ArXiV:0903.3905

Panda Physics, Data Acquisition and Event Filtering

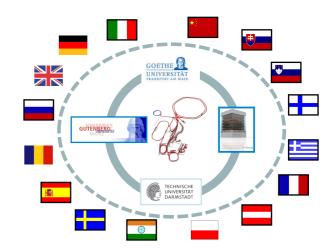
- Problem: finding the needle in the haystack
- total inelastic cross section
 - 50 mb
- Interesting physics
 - many channels < 100 nb
- 2×10⁶ interactions /s
- Data rate after FEE reduction: 200 GBytes/s
 - 17 PBytes/day
- Goal for online event filtering:
 - reduce "background" by factor of 1000



FAIR Tier 0 Data Center

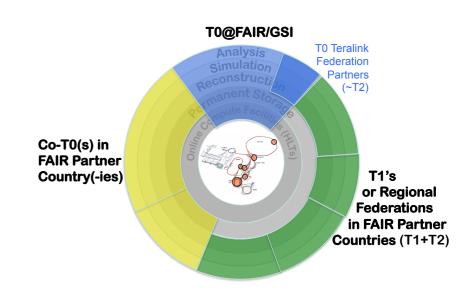
Estimated total for full FAIR FAIR Tier 0

- 300,000 CPU-cores
- 35 PByte/year Online-Storage (HDD)
- 30 Pbyte/year Permanent-Storage (Tape)
 Comparable resources in FAIR
 partner countries



Key Points

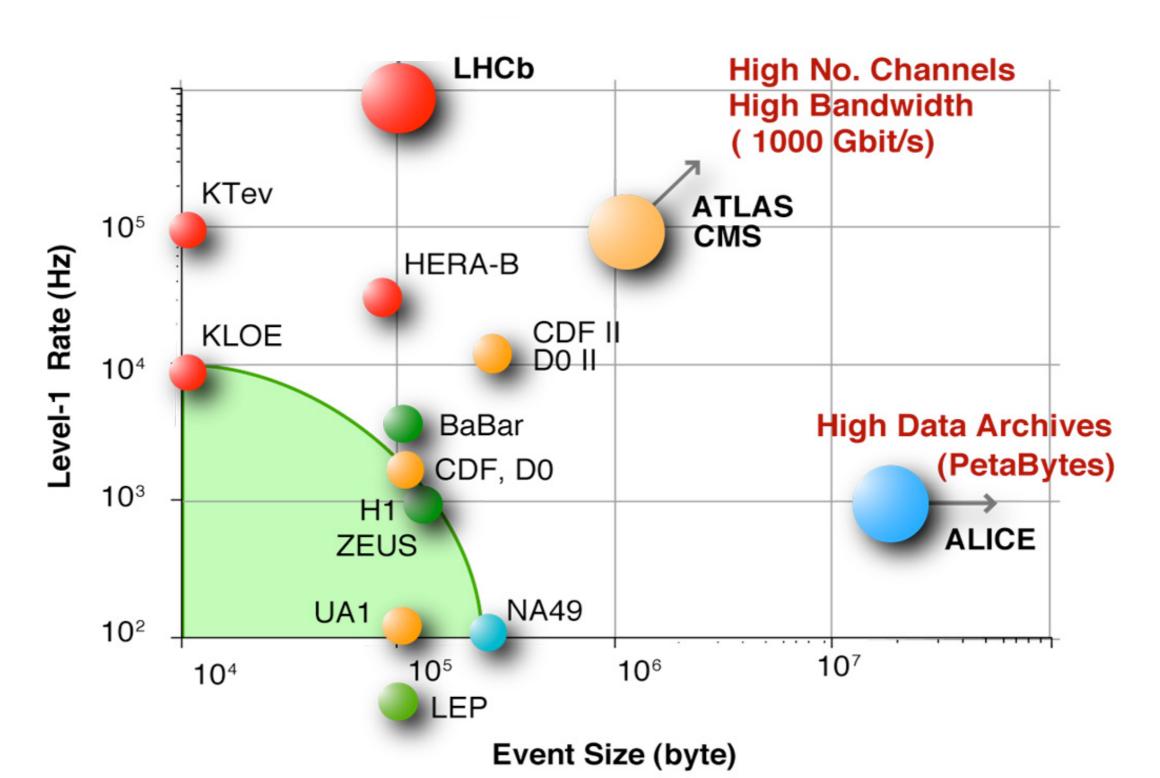
- Few big, highly efficient data centers
- Further partner connected via regional federations





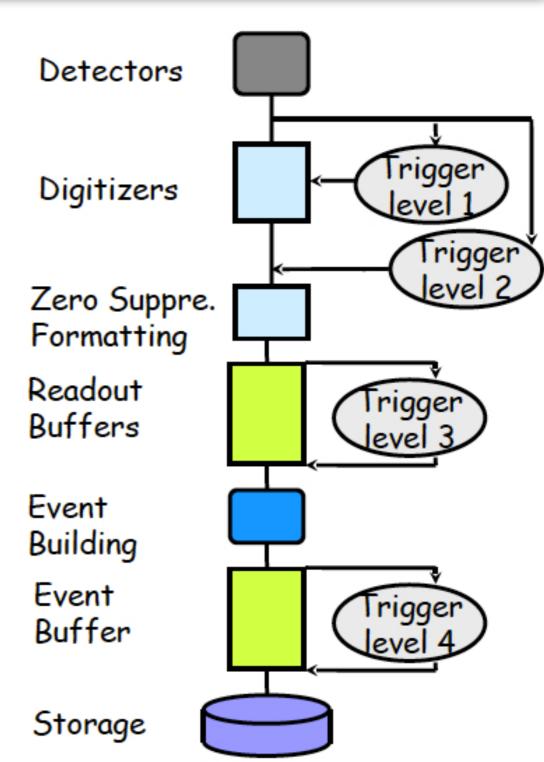
The PANDA DAQ Challenge





Conventional Approach

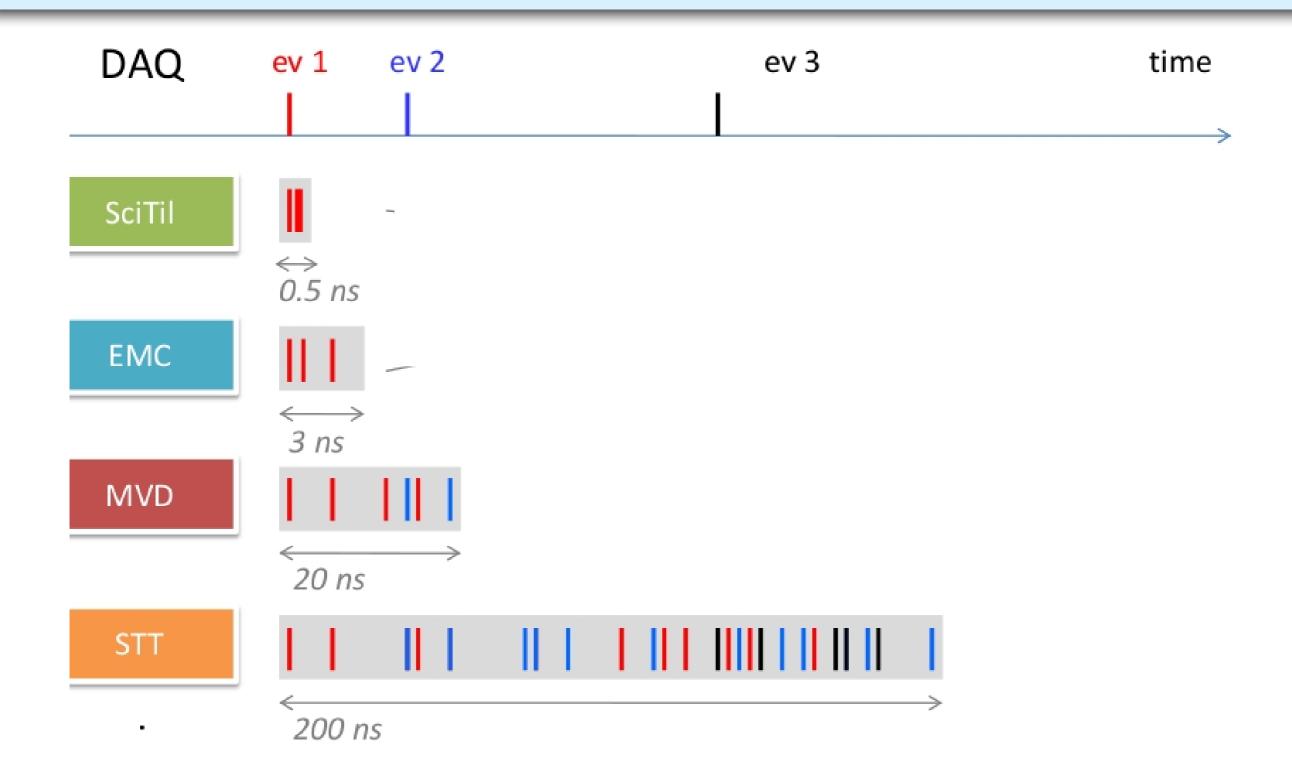
- Multi-level hardware trigger
 - Buffering at each level until trigger decisions are taken
- Works well, if physics provides clear and simple trigger signatures
 - ATLAS / CMS :
 - missing Et, high pt muons, jets, etc
- For some experiments, there are no such simple selection criteria
 - LHCb: look for B decays (secondary vertices)
 - PANDA: exclusive kinematic reconstruction of complete events (all reaction products measured)



PANDA Approach

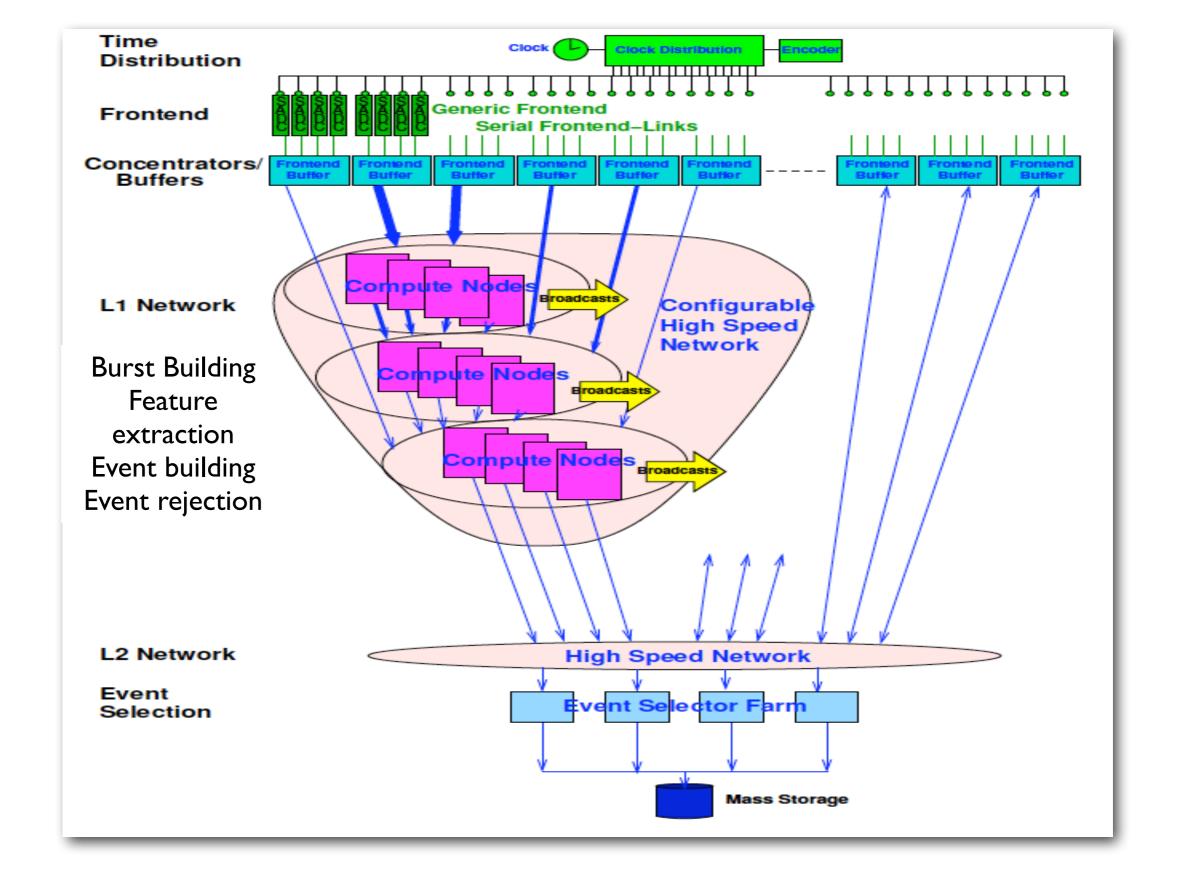
- Freely streaming data: "Trigger less"
 - No hardware triggers
 - However, there will be event filtering, we do not record everything !!
- Autonomous FEE, sampling ADCs with local feature extraction
- Time-stamping (SODA)
 - Data fragments can be correlated for event building
- Caveat: the high-rate capability implies overlapping events !!!
 - average time between two events can be smaller than typical detector time scales
 - This "pile-up" has to be treated and disentangled
 - Real-time event selection in this environment is very challenging and requires a lot of studies

Overlapping Events (Time-based simulations)



Challenges

- How much can we reduce the primary data rate?
 - Software trigger group (principal physics simulations)
 - Answer: maybe up to factor 1000, some loss of efficiency
- Caveat: event based estimate, but overlapping data @ 20 MHz
 - A priori, there are no "events", there is just a stream of "data" from each sub-system
 - Worst case: if we cannot assemble events online, we have to store everything, because we cannot reject anything!
 - 200 GB/s -> 17 PB/day, compare to 30 PB mass storage/year @ FAIR Tier 0
 - Impossible!
 - Even running at 200 KHz only would exceed the available yearly storage capacity
- The PANDA physics program is not feasible without effective filtering, reducing the event rate by more than 2 orders of magnitude
- This works only if we are able to reconstruct most of the raw data in realtime. Massive challenge!
 - We need full time-based simulation and reconstruction software to judge feasibility and determine required resources (work in progress !!!)

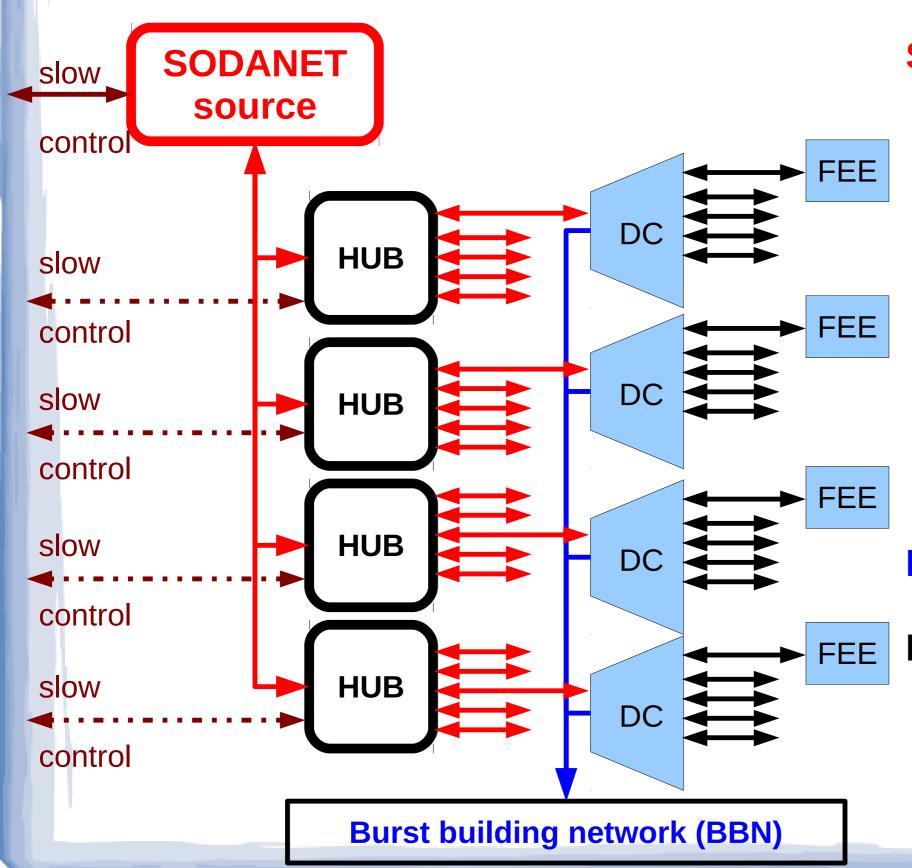


PANDA DAQ / Event Filter









SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
 - source → DC: synchronization information and FEE configuration
 - DC → source: slow control, used for time calibration

Data link (DC → BBN):

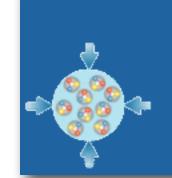
Unidirectional

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

Next steps

 Discussion with CBM about common "FAIRnet" protocol and other common developments



Joint CBM / Panda DAQ developments - "Kick-off" meeting

chaired by Jan Michel (IKF, Universität Frankfurt)

from Thursday, February 19, 2015 at 12:30 to Friday, February 20, 2015 at 15:00 (Europe/Berlin) at GSI (KBW small lecture hall (Thursday), KBW 2.27 (Friday))

- New hardware (TRB4) based on Kintex 7, suitable for all sub-systems not using radiation hard GBT links
- TRB3 > TRB4 for all other sub-systems
 - Design by Pavel Maciniewski (Uppsala)







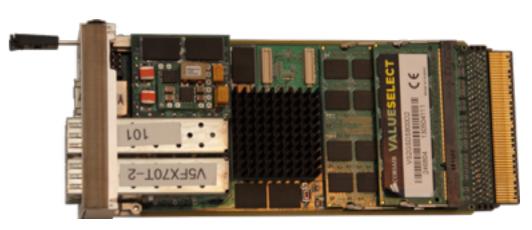
SODANET provides:

- synchronization of the FEE
- Continuous monitoring of the DC/FEE functionality
- Rough (initial) time calibration of the propagation time of the synchronization signal
- Transfer of a slow-control (FEE configuration/status) information: low priority, transmission of a slow-control package can be interrupted at any time by a synchronization package

Compute Nodes (L1 network)

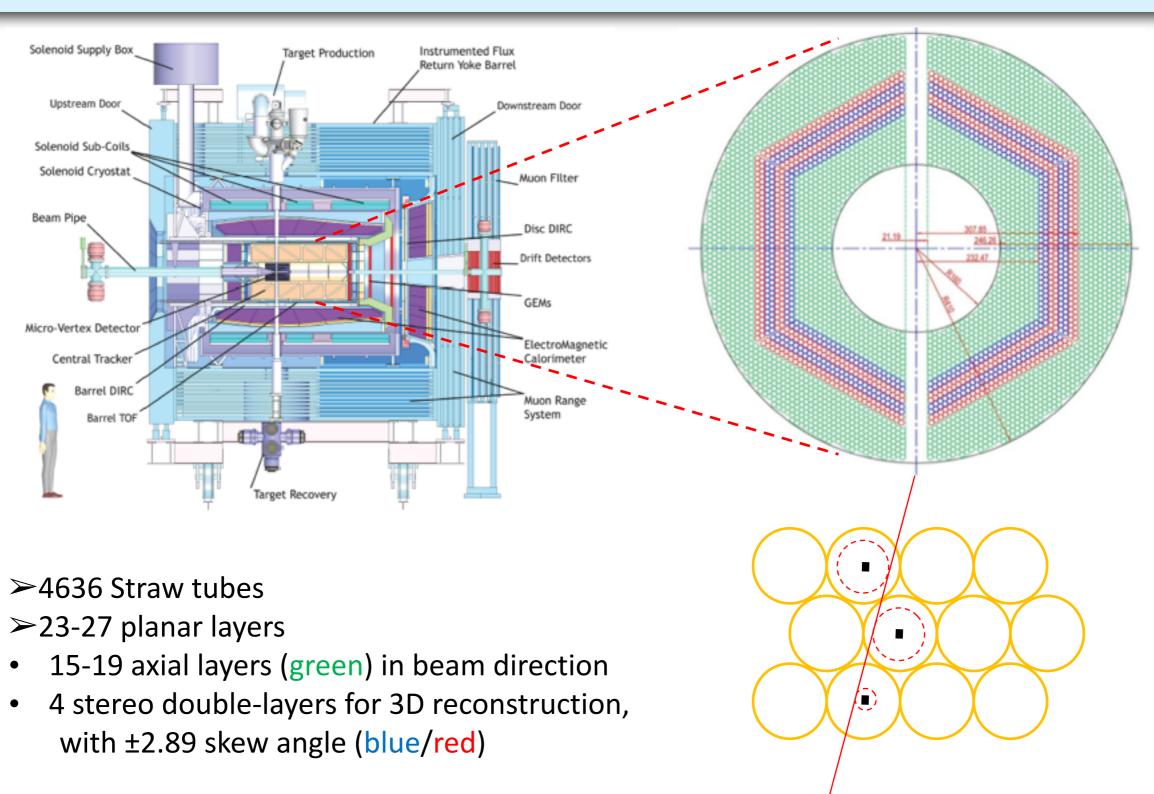
- Burst building, event building, first stage of event rejection based on kinematical event reconstruction
 - FPGA based Compute Nodes (CN)
 - ATCA standard, full mesh backplane
- 4 FPGA Virtex5 70FXT + I Virtex 4
 - 16 optical links, GbE
 - 18 GBytes DDR2
- Next steps, design currently under discussion (xFP card)
 - ATCA -> uTCA.4?
 - Virtex 5 -> Kintex 7
 - 4 GB DDR2 -> 8 GB DDR3
 - Gb Ethernet -> 10 Gb Ethernet ?
 - 4 SFP optical links -> 12 uPOD links







Application Example: Tracking for STT (Yutie Liang)



From STT: Wire position + drift time

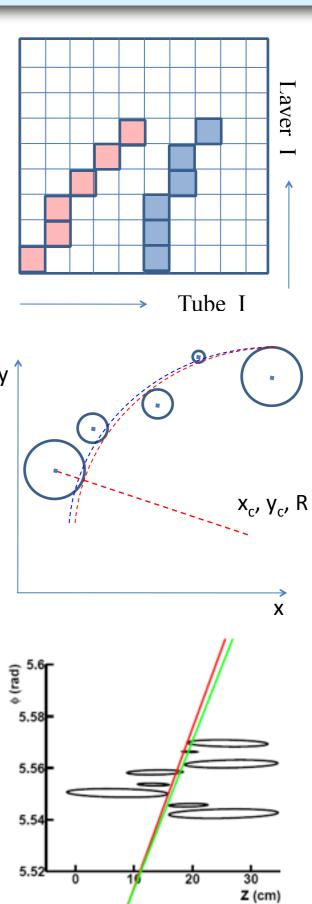
Tracking algorithm

"Road" search

• Helix parameter determination

• Transverse momentum

Longitudinal momentum

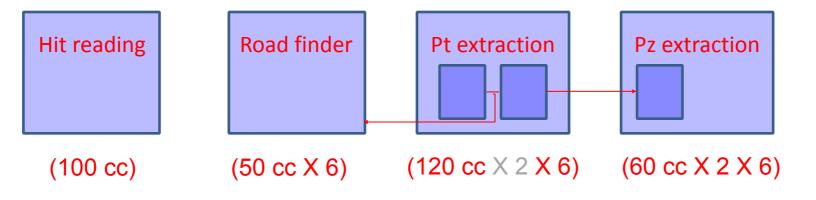


Results (VHDL implementation)

Momentum resolution 3% @ I GeV/c

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	25,022	50,560	49%
DCM autocalibration logic	14	25,022	1%
Number of 4 input LUTs	33,120	50,560	65%
DCM autocalibration logic	8	33,120	1%
Number of occupied Slices	21,563	25,280	85%

For one event with 100 hits (6 tracks): 7 μs



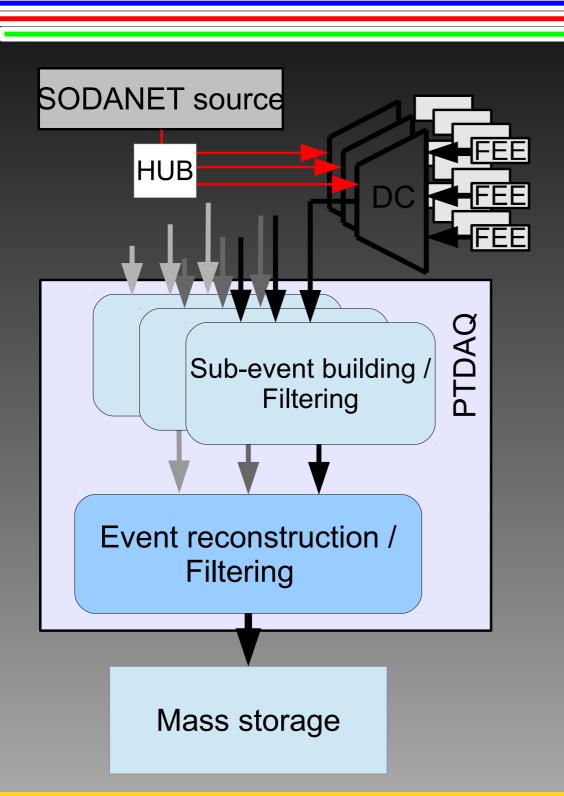
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Current Activities

- Hardware
 - Set up toy DAQ system (PTDAQ) with scaled down architecture for detector prototype tests in realistic DAQ environment
 - Freely streaming, FEE feature extraction, event building, high level feature extraction on FPGA, L2 network processing with small farm for final event selection
 - Time-based simulations for full PANDA setup and critical benchmark channels
 - Determine realistic rejection rates at high luminosity
 - Define required bandwidth, computing resources and partitioning for L1/L2 networks
- Crucial input for DAQ TDR

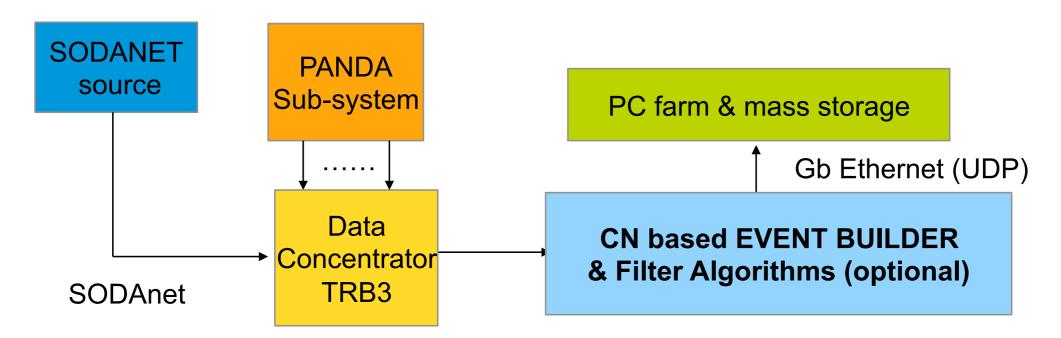
Prototype Trigger-less Data Acquisition (PTDAQ)



Functionality:

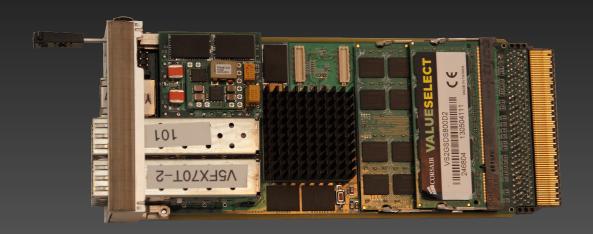
- Digitalized data front end electronic synchronized at data concentrator
- Sub-event building and first filter algorithm
- Event reconstruction and second stage of filter algorithm

Initial Setup (Toy DAQ) for Test Beams



- uTCA shelf with I to 4 xFP cards
- Supports up to 9 optical connections to data concentrators
 - Basic configuration with single xFP: 4 optical inputs
 - Extended configuration with 3 xFP for data input and 1 xFP for event building
 - Tracking, EMC shower handling, filtering etc. as an option
- Output rate limited by Gb Ethernet : (< I20 GB / s)
- Basic slow control functionality via Ethernet/EPICS (start/stop DAQ, file handling, event counters etc.)

Hardware Components



xFP board:

- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
 - 6.25 Gbit optical
- 1 Gb Ethernet

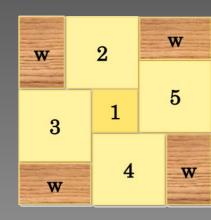


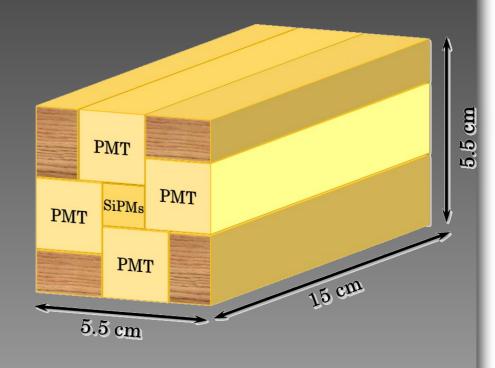
Micro TCA shelf:

- Up to 4 xFP
- Up to 9 data concentrators

MAMI Test Setup

- Beam parameter:
 - 210 MeV electrons
 - 0.003 2 MHz event rate
- Detector:
 - 1 mini PWO crystal
 - 2 HAMAMATSU SI-PM
 - 4 PANDA crystals



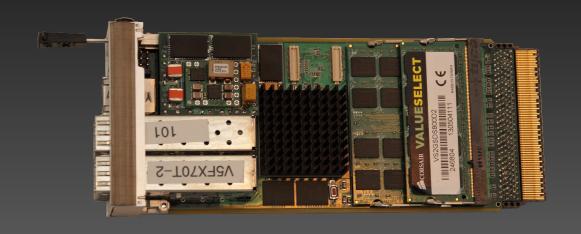


Used Hardware



Sampling ADC (Uppsalla)

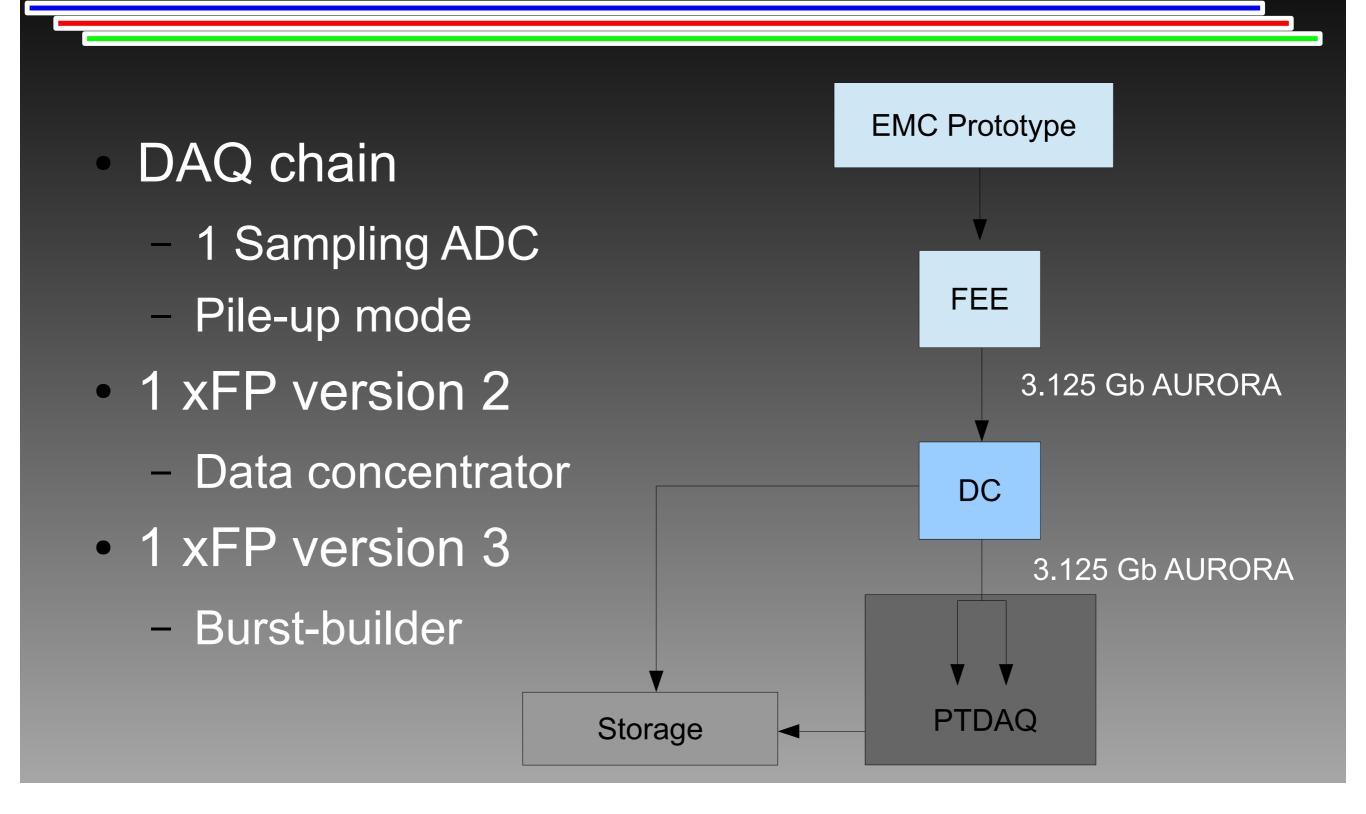
- Version 2011
- 16-ch, 14-bit
- 125 MSPS
- Virtex-5LX50



xFP board:

- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
 - 6.25 Gbit optical
- 1 Gb Ethernet

MAMI Test Setup

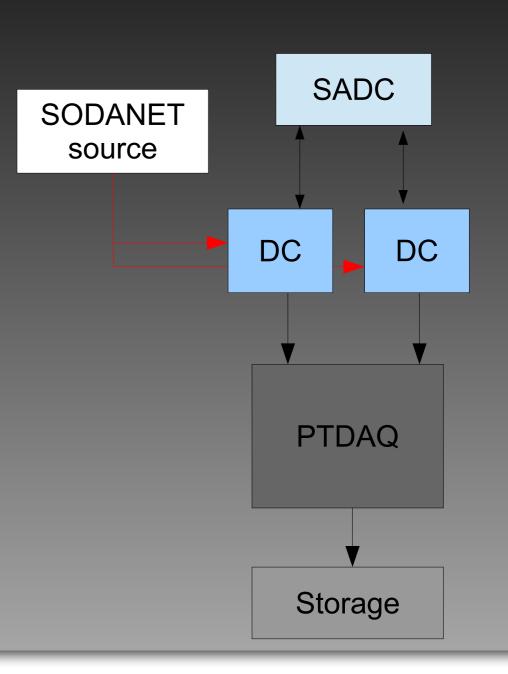


MAMI Test Results

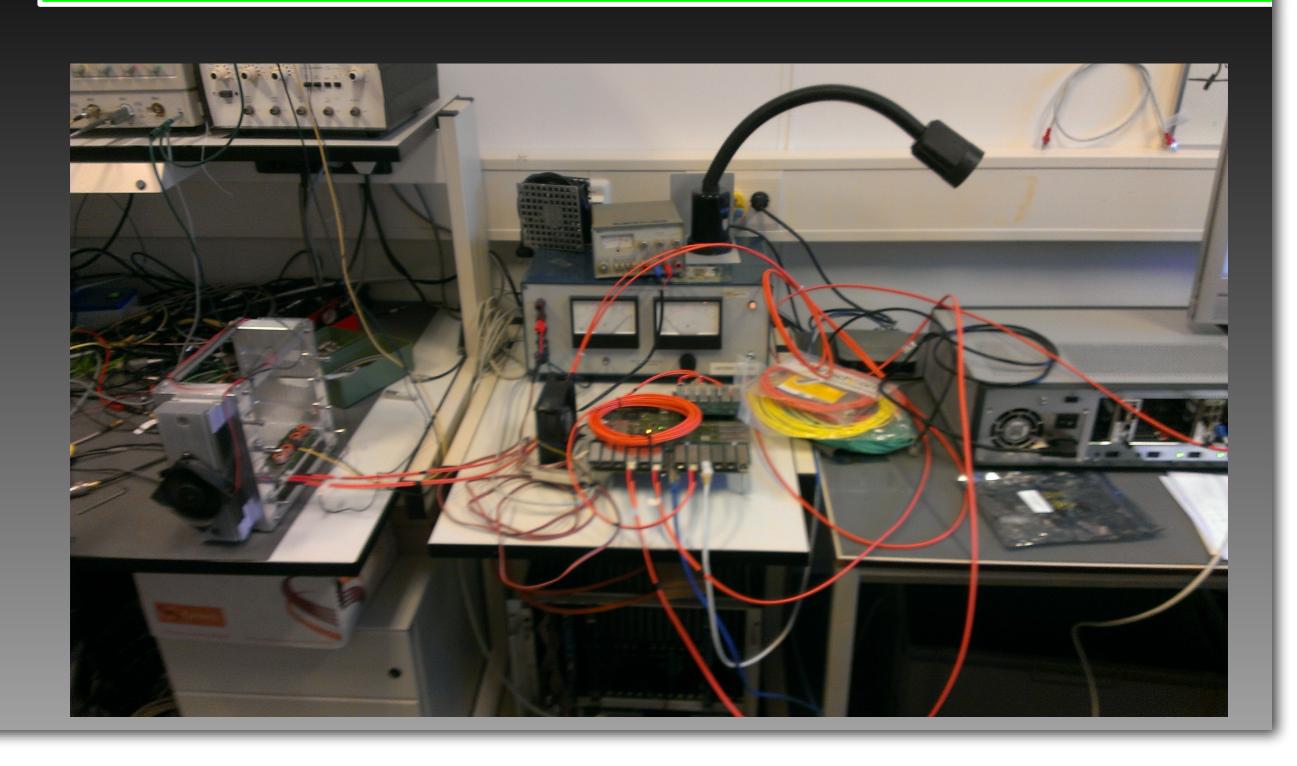
- Stable Connection between DC and xFP
 - 2-Input burst building successful
 - For ~ 15 * 10⁶ Stable events
 - Event size ~ 700 Byte
 - Data rate of ~1 Gbit/s

Groningen SODANEt Connection Test

- DAQ chain
 - 1 Sampling ADC (Uppsala)
 - Feature extraction mode
- 1 TRBv3
 - 2 Data concentrator
 - 1 SODAnet source
- 1 xFP version 3
 - Burst-builder



Groningen SODAnet Connection Test



Results

Stable Connection between TRBv3 and xFP using SODANET

- Stable Connection without burst building
 - Several 100 * 10⁶ events
 - Data rates between
 - -0.5 to 10 MB/s
- 2-Input burst building successful
- 1 * 10⁶ Stable events
 - Event size ~ 60 Byte
- Data rate of ~ 0.5 Mbit/s

Conclusions

- Free-streaming DAQ with online event filtering is crucial prerequisite for our physics program
 - Without effective event filtering, we can only run at low luminosity (a few times $10^{29} \, \mathrm{cm}^{-2} \, \mathrm{s}^{-1}$)
 - Loss of major part of PANDA physics !!
- At this point, we do not have the necessary tools to design the filtering algorithms for high luminosity running with overlapping events
 - Lack of full time-based simulation and reconstruction software
 - Major issue for further development of PANDA DAQ
- Today, we have working prototype hardware available that allows to run test experiments with prototype detectors in a configuration that has all the essential ingredients of the final PANDA DAQ
- Hardware development is progressing, moving to new generations of FPGA based electronics

Next PANDA DAQ&FEE Workshop

- GSI Darmstadt, April 9/10 2015
- Please contact Angelo Rivetti or Miroslav Kavatsyuk if you would like to contribute to the FE electronics section
- Please contact me for contributions about DAQ/Event Filtering