Current Status of the EMC Readout

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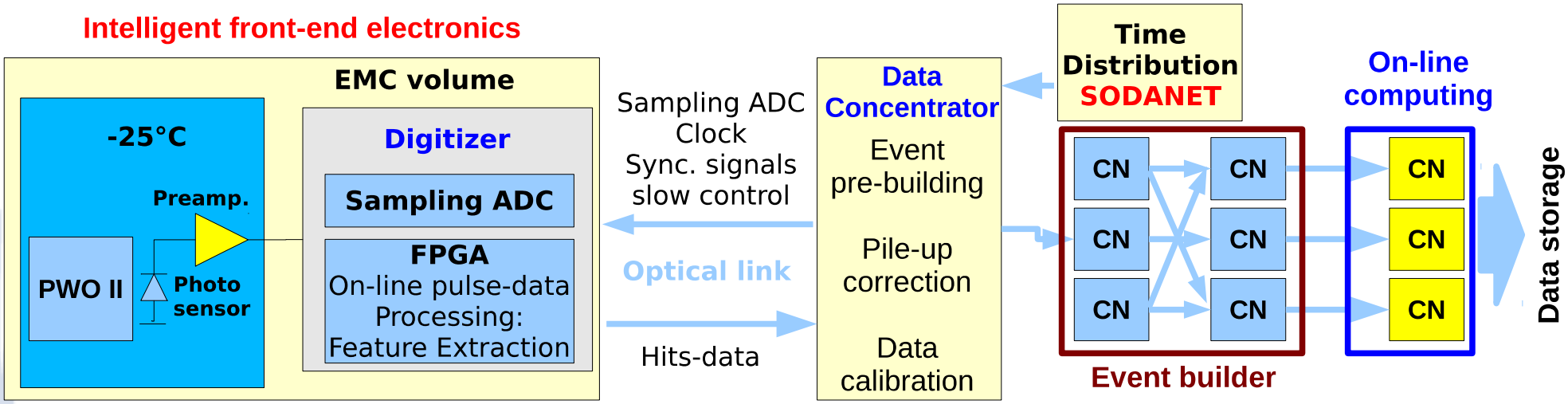
EMC Readout

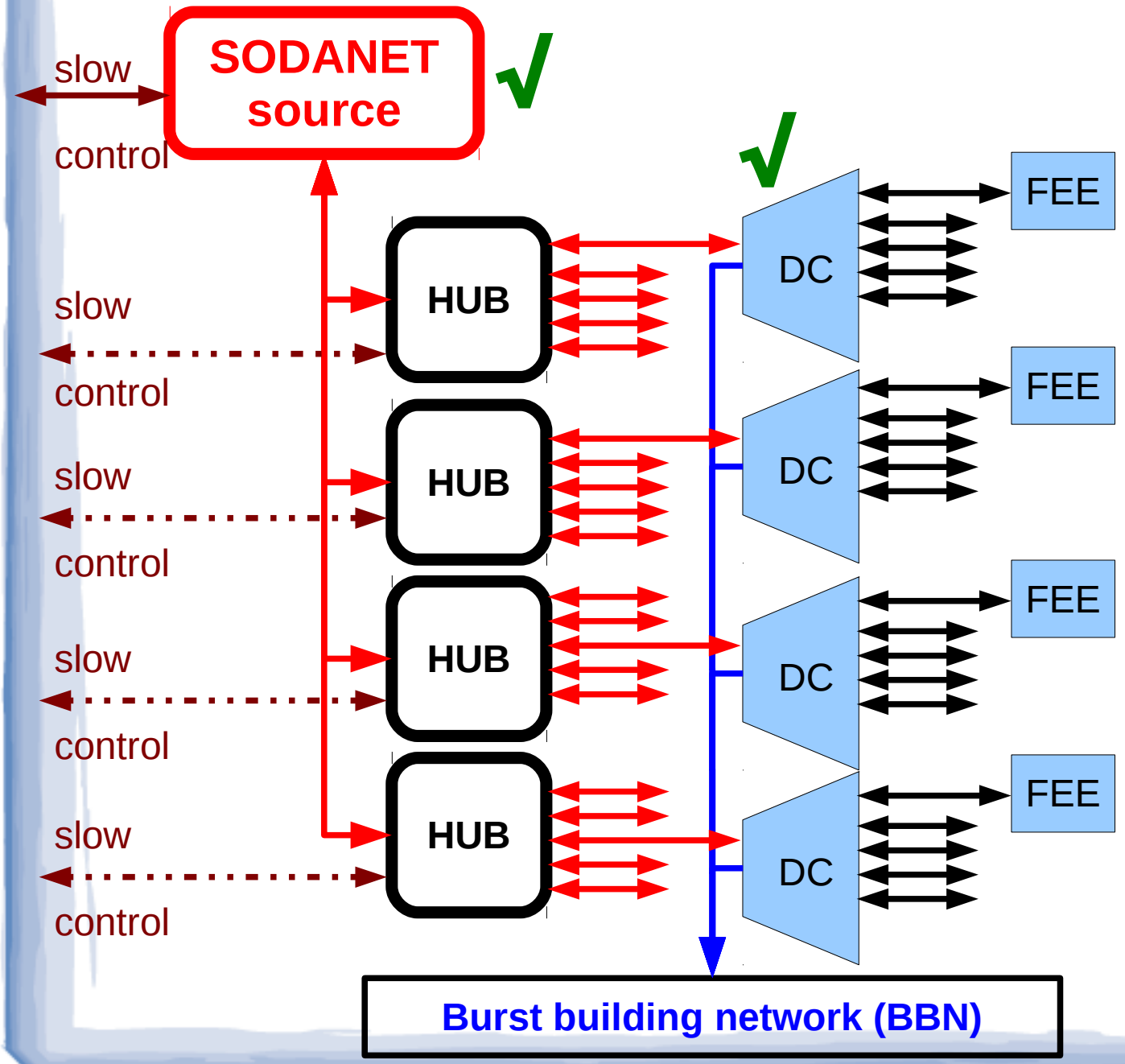


SODANET protocol:

- Determines communication between all key components of the readout (time synchronization, front-end configuration, data transfer for the on-line computing)

Implementation of the SODANET in the readout is required for possibility to perform common tests for few subsystems (including on-line computing)

SODANET Topology



SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
  - DC → source: slow control, used for time calibration

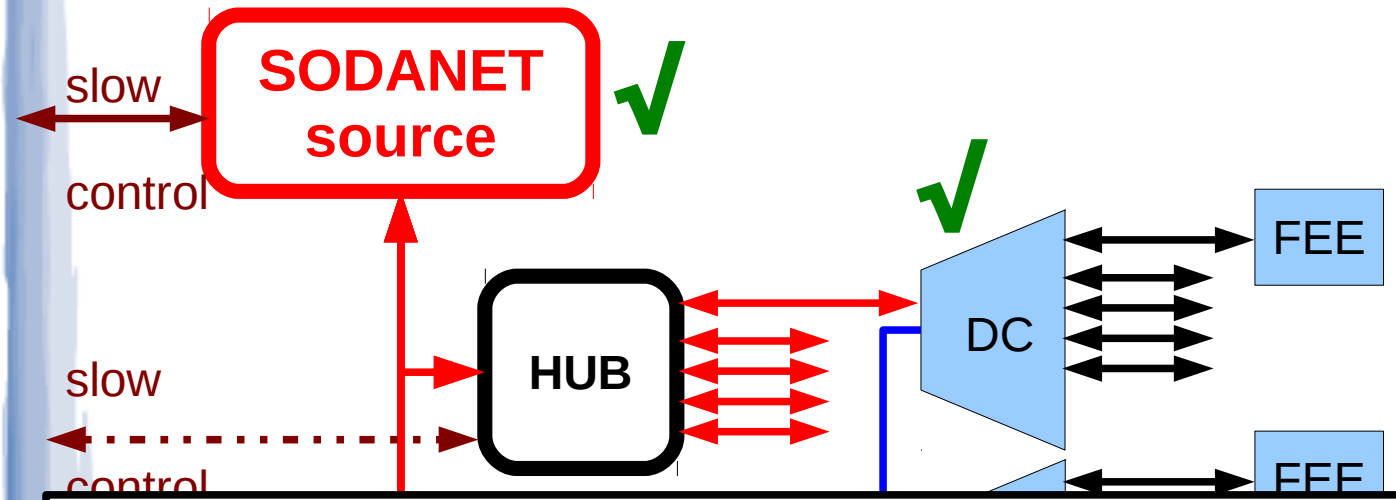
Data link (DC → BBN):

- Unidirectional Ethernet

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

SODANET Topology



SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization

Done (stable operation of the hardware/firmware):
- SODANET source
- SODANET endpoint (DC)

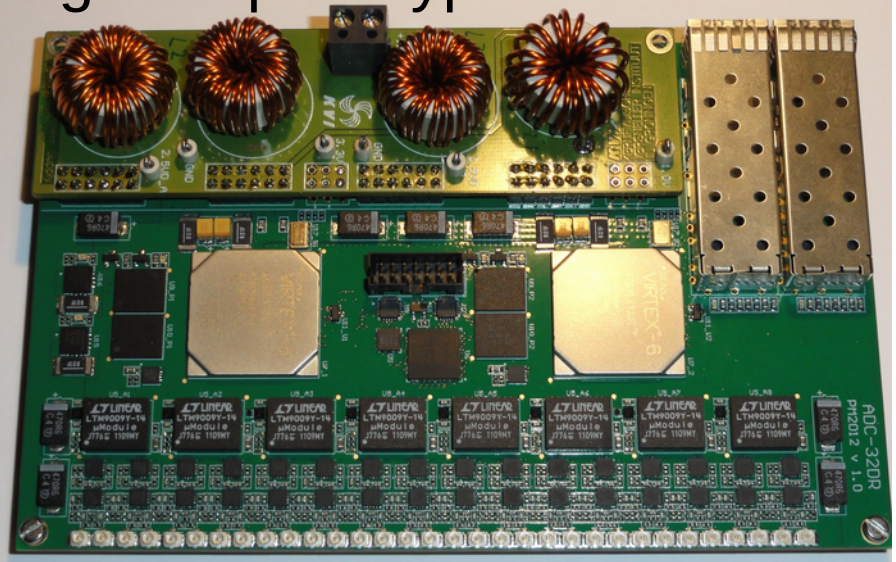
Work in progress:
- SODANET HUB (required for multiple endpoints)
- Switch to the clock frequency of 150 MHz (currently 100 MHz)

Burst building network (BBN)

synchronous
- Protocol up to subsystem

EMC Digitizer

Digitizer prototype v2



(developed by P. Marciniewski)

Feature Extraction:

- Base-line follower
- Pulse detection
- Pile-up detection (output waveforms)
- Precise time (**new**: improved performance for low-amplitude pulses)
- Precise energy
- **New**: Possibility to readout raw ADC data (access to the noise-level measurement)
- **To be done**: Triple redundancy, self-monitoring for configuration errors

Hardware:

Digitizer v2 (available):

- Performance – close to required
- Dual-range input, sequential splitting (not optimal for S/N, not possible to use with APFEL preamplifier)
- Long restart time (~ few seconds)
- Too expensive FPGA

Digitizer v3 (in production):

- 64 separate inputs (parallel splitting for dual range, possible to use with APFEL preamp.)
- Short restart time
- FPGA from the latest family (acceptable price)

Data Concentrator

Implemented and tested:

- SODANET end-point
- Time ordering of data from all inputs
- Packaging of the output data according to the SODANET protocol

Work in progress:

- On-line data reduction (combing data from two different channels related to two LAAPDs, reading out one crystal; data-streams from two digitizers)
- On-line pile-up recovery
- Calibration

Current issues:

- No stable performance of the UDP core (TRB) at the output of the data concentrator (hangs after some time: few minutes – few hours)

Readout demonstrator

Possible configurations of the demonstrator:

- **EMC only, no event-building network**
  (working version exists)
  - One DC with 4 inputs
    (up to 4 digitizers reading out 128 photo sensors)
  - Two Digitisers v2 (two digitizers v3 are in production)

- **EMC only, with event-building network**
  (Requires implementation of the SODANET hub, other components are ready)
  - Two DC with 4 inputs
    (up to 8 digitizers reading out 256 photo sensors)
  - Two Digitisers v2 (two digitizers v3 are in production)

- **EMC+MVD+STT, with event-building network**
  (Requires implementation of the SODANET hub, implementation of the SODANET for the MVD and STT)

Planning

Next steps in the development of the readout:

- Beam measurements with EMC prototypes
- Implement SODANET hub
- Implement missing functionality of the EMC data concentrator
- Implement firmware for the digitizer v3
- Implement event building (on-line clustering in compute node)
- Implement triple redundancy for the digitizer firmware

Steps which require involvement from other subsystems:

- Development of a run-control software (required for all test measurements with prototypes)
- Development of new hardware for the data concentrator/SODANET source

KVI

university of groningen

Thank you for your attention!

KVI TRB v3 as Data Concentrator

Advantages:

- Possibility of different configurations of the readout system

Disadvantages:

- Low optical-fibre speed:
  - max 3.2 Gb/s in asynchronous mode
  - max 2.5 Gb/s in synchronous mode
  - 4 SFPs are connected to a single quad-serdes – have to use same frequency
  - In case of usage of all FPGAs for the DC there might be problems with Ethernet connection (mandatory for the TRB) due to non-standard frequency

In case of usage of the SODANET frequency of 154.52 MHz:

- Maximum link speed for SODANET with TRBv3 is 1.54 Gb/s – might be too slow for the front-end
- Connection to compute node has to be at 3.08 Gb/s

Solution: – new hardware (required for the final version)
– usage of a standard frequenty

DC Output Data-format

- DC can start transmitting FEE data once it is available
  (without waiting till the end of a super-burst)
- If no data are available –
  DC sends an empty package at the end of the Super-burst

Data-package

31 16	15 0
last-packet flag; packet number	data size in bytes
Not used (same as HADES)	Not used (same as HADES)
Status and error	System ID
Super-burst number	
Data	

GbE paket builder in FPGA (HADES) can be reused to pack data