High Voltage - Monolithic Active Pixel Sensors and Luminosity Detector DAQ

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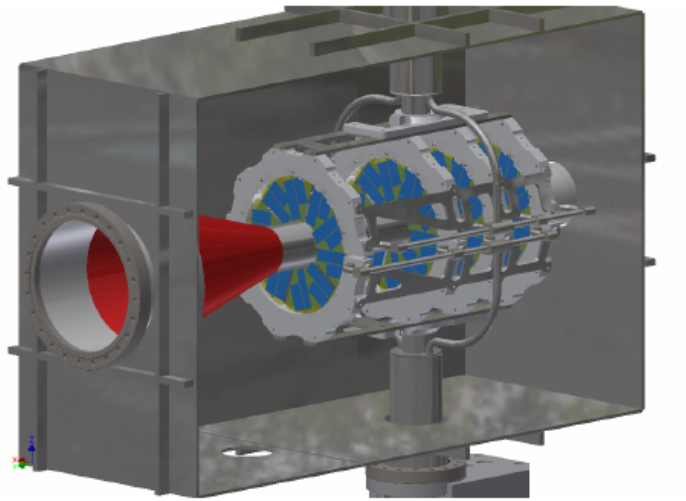
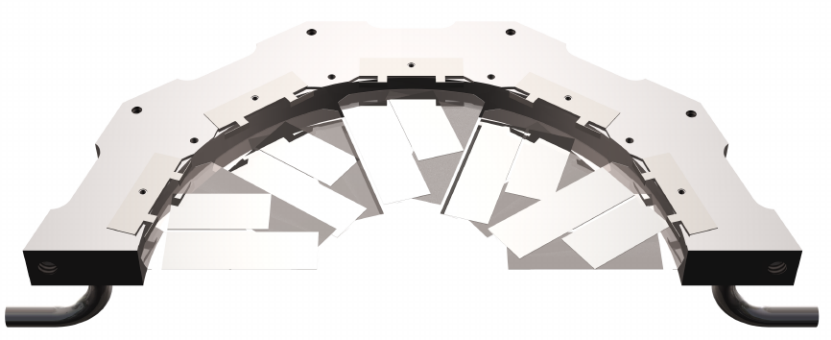
PANDA Collaboration Meeting
DAQ Session

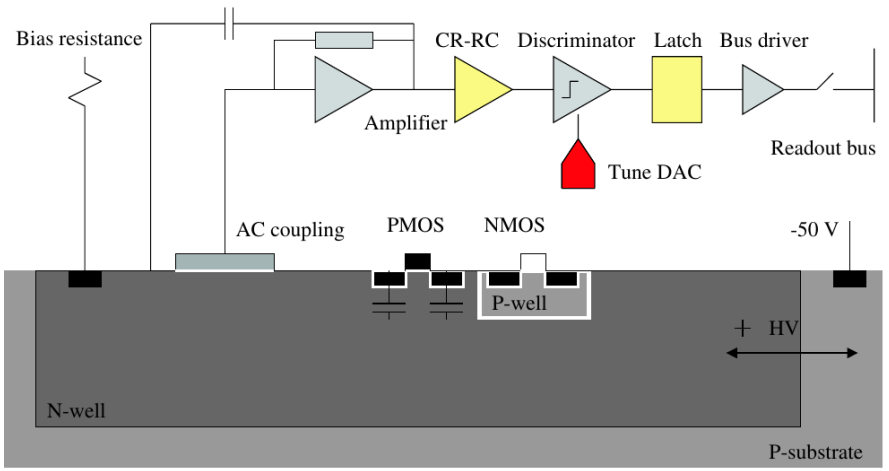
Luminosity Detector





- measurement scattering angle of anti-protons using 4 silicon tracker stations
- 50 sensors per half plane $\Rightarrow$ 400 HV-MAPS in total

HV-MAPS



- under development by Ivan Peric
- fast charge collection
- radiation tolerant
- thickness of 50 µm
- readout frequency between 20-40 MHz
- 2 LVDS-Link @ 400-800 Mbps

Expected Data Rate

- data format (preliminary):

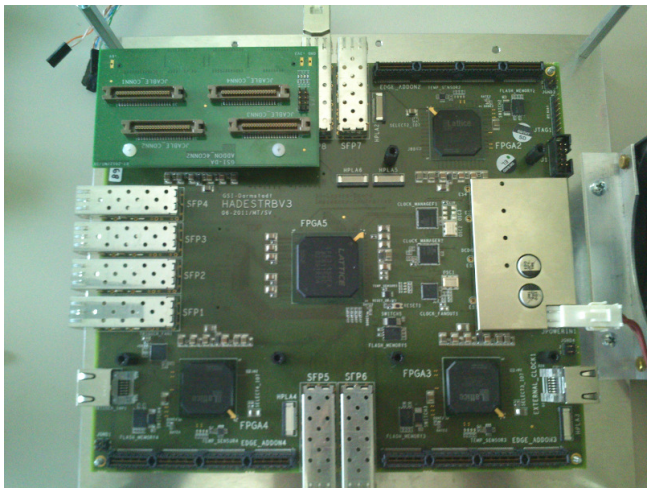
Timestamp	Row-Address	Column-Address
20 bit	8 bit	8 bit

- particle rate simulations with DPM generator (C. Stoll) $\Rightarrow$ data rate per plane

Beam Energy [GeV]	particle rate [MHz]	data rate [Mbps]
1.5	3.80	136
15	3.44	123

- comma word or timestamp if no hits in sensor
- total data rate from all layers: 495 - 550 Mbps

TRBv3 as Frontend Board



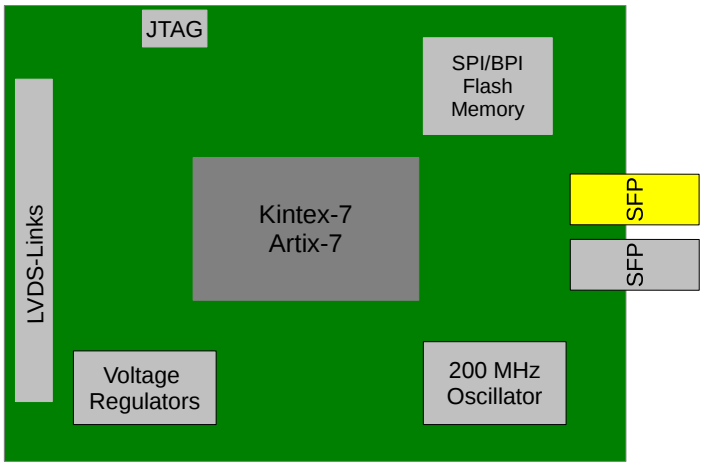
Advantages

- already there and tested
- fast enough for our needs

Disadvantages

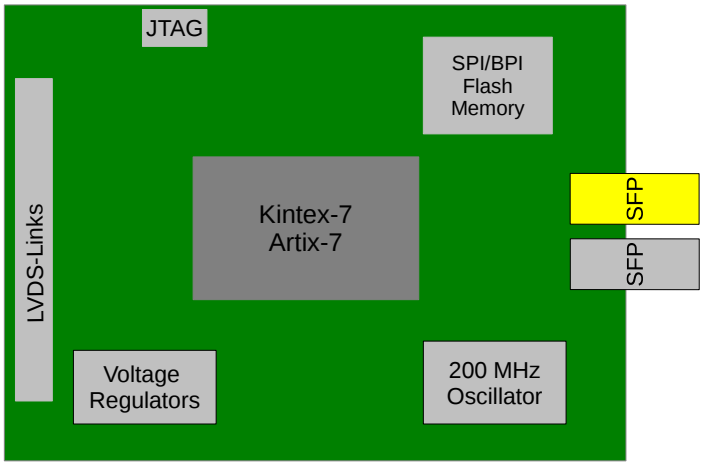
- six free Serdes-circuits per side FPGA $\Rightarrow$ 24 links/TRB
- to increase links/TRB
  - Serdes and 10b/8b Decoder in FPGA-logic
  - Clock-Data Synchronisation with Delay-IC

Luminosity Detector Frontend FPGA-board



- based Xilinx Kintex/Artix-7
- compatible with SODA
- feasibility study by IMM

Luminosity Detector Frontend FPGA-board



- feasibility study by IMM
  - first cost estimate 100.000€
- development with Heidelberg using Altera FPGAs

Questions to DAQ-Group

Frontend Board

- Stay with TRB
- development of own board

SODA

- Does a common repository for SODA VHDL-Code exist?
- Is special hardware required to built soda source or can one use any FPGA board with Xilinx/Lattice FPGA?
- What kind of optical links will PANDA use?

Thank You for your Attention!