Updates on the Strips Front-End Architecture

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PANDA Collaboration Meeting

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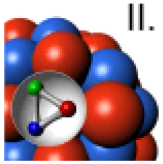

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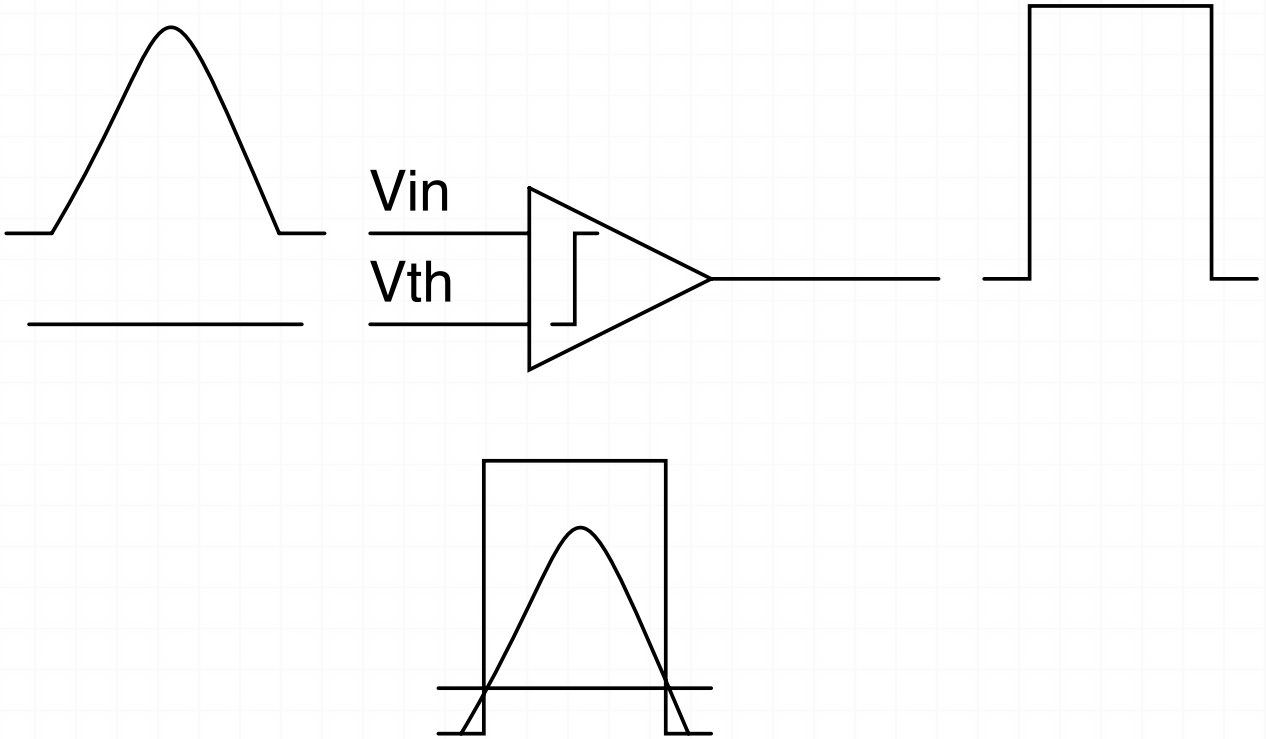
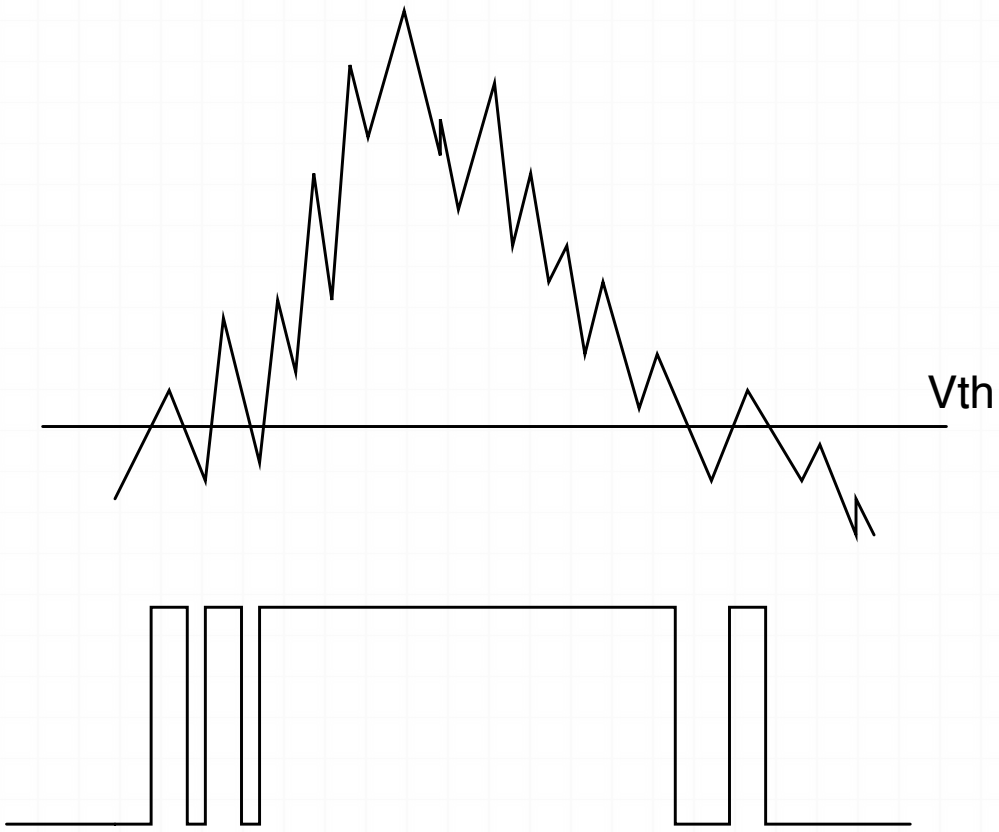
Contents

Comparator



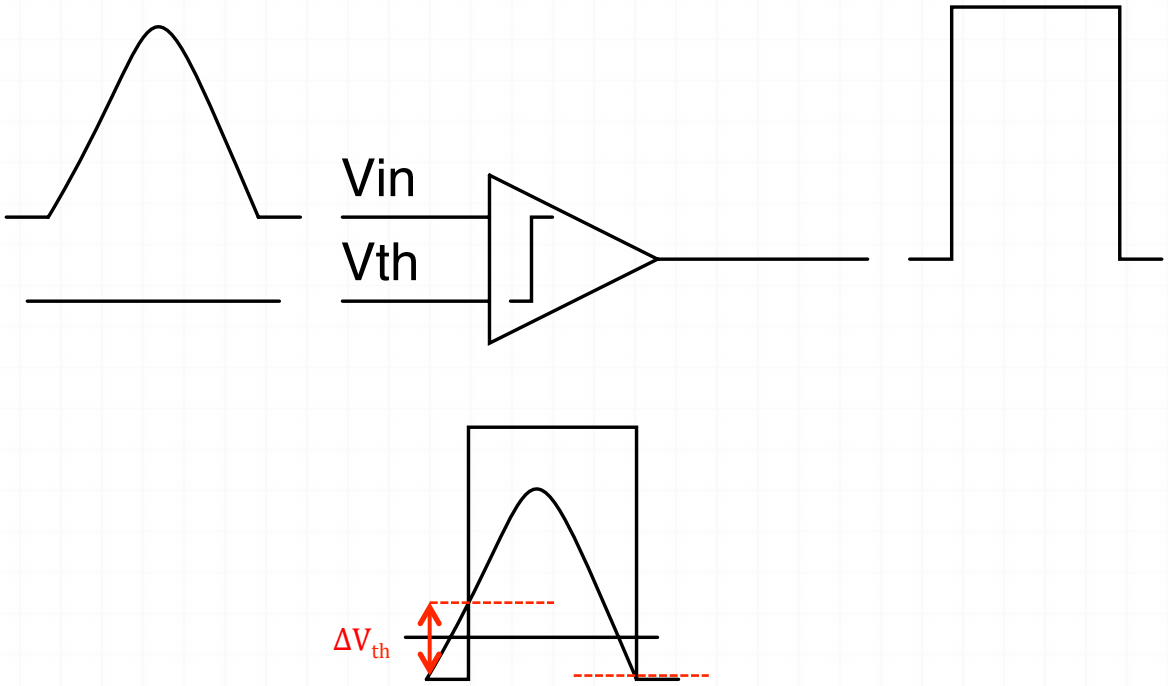
The comparator fires when the signal is equal to the threshold.

Hysteresis Comparator I



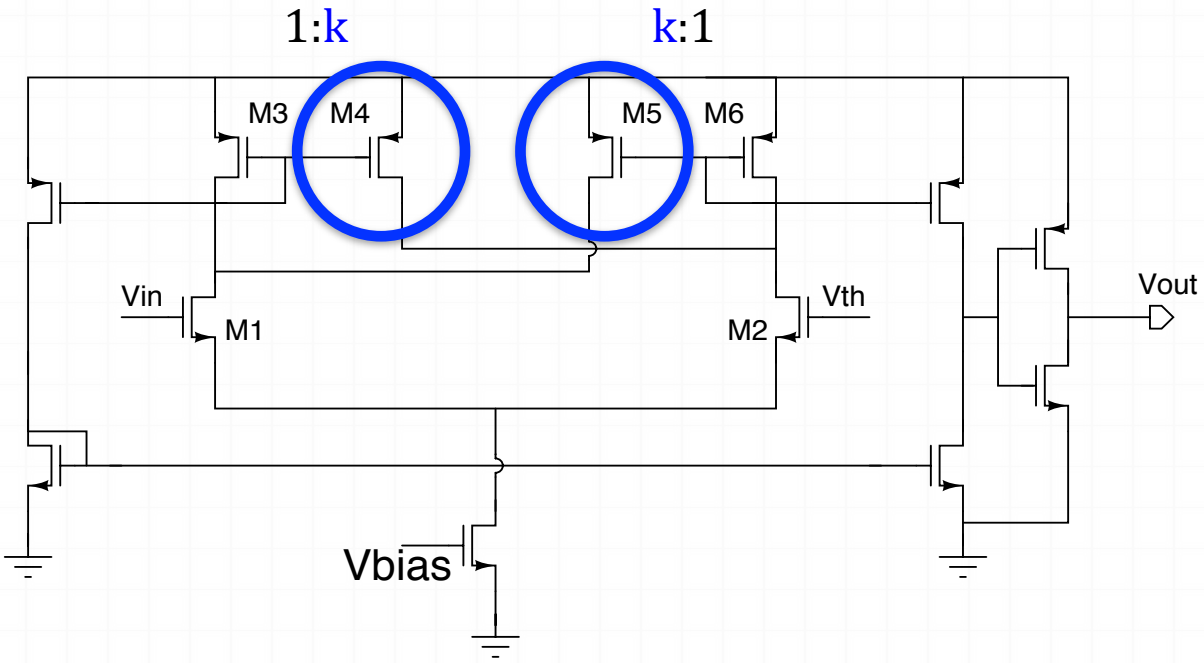
If we take into account the noise, the comparator can fire before or after the expected value and we could also have multiple flippings

Hysteresis Comparator II



The output doesn't fire when the signal reaches the set threshold.

Hysteresis Comparator Transistor Level

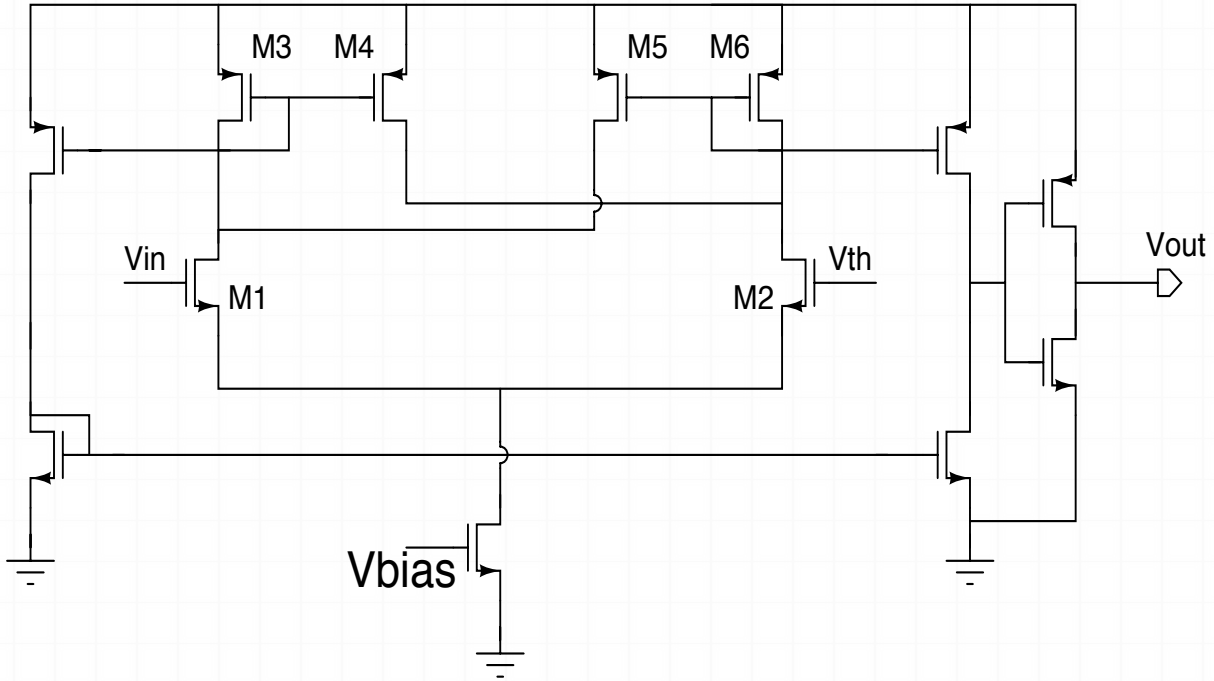


In the “classic” comparator the ouput changes when the current flowing into M1 is equal to the one into M2

In the hysteresis comparator we don’t have this effect

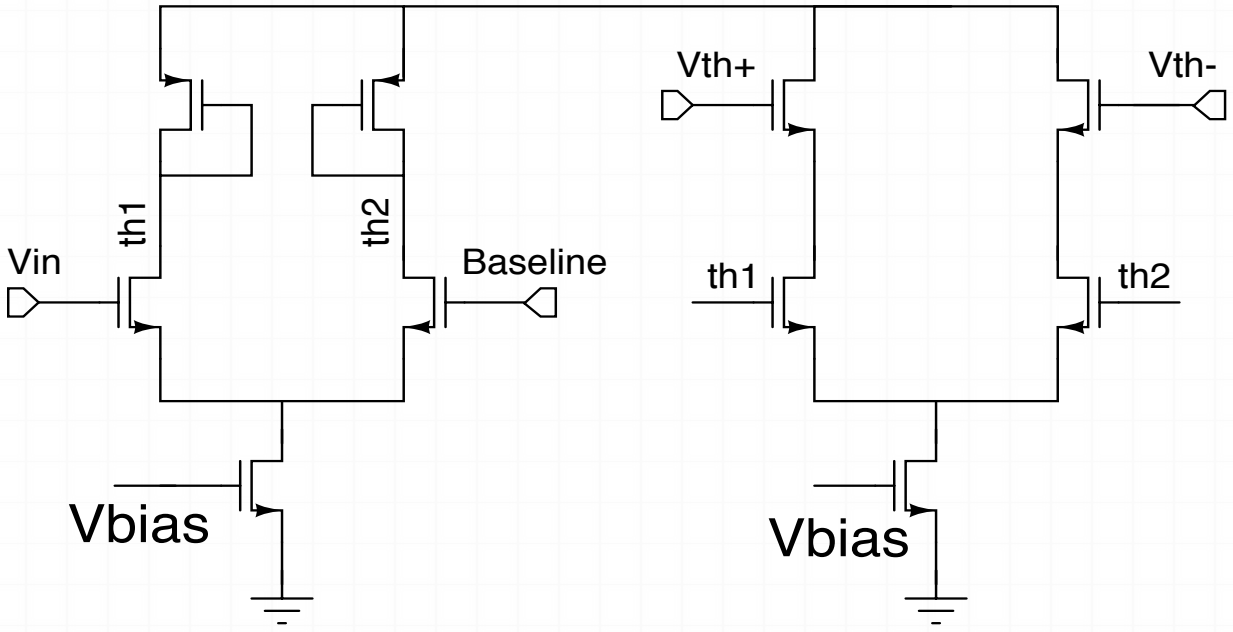
Hysteresis Comparator Current

- $i_{M1} = i_{M5}$
- $i_{M2} = i_{M4}$
- $i_{M5} = k^* i_{M6} = k^* i_{M2}$
- $i_{M1} + i_{M2} = i_{bias}$



- $i_{M1} = k/(1+k)\ i_{bias}$
- $i_{M2} = 1/(1+k)\ i_{bias}$

Single to Differential Stage

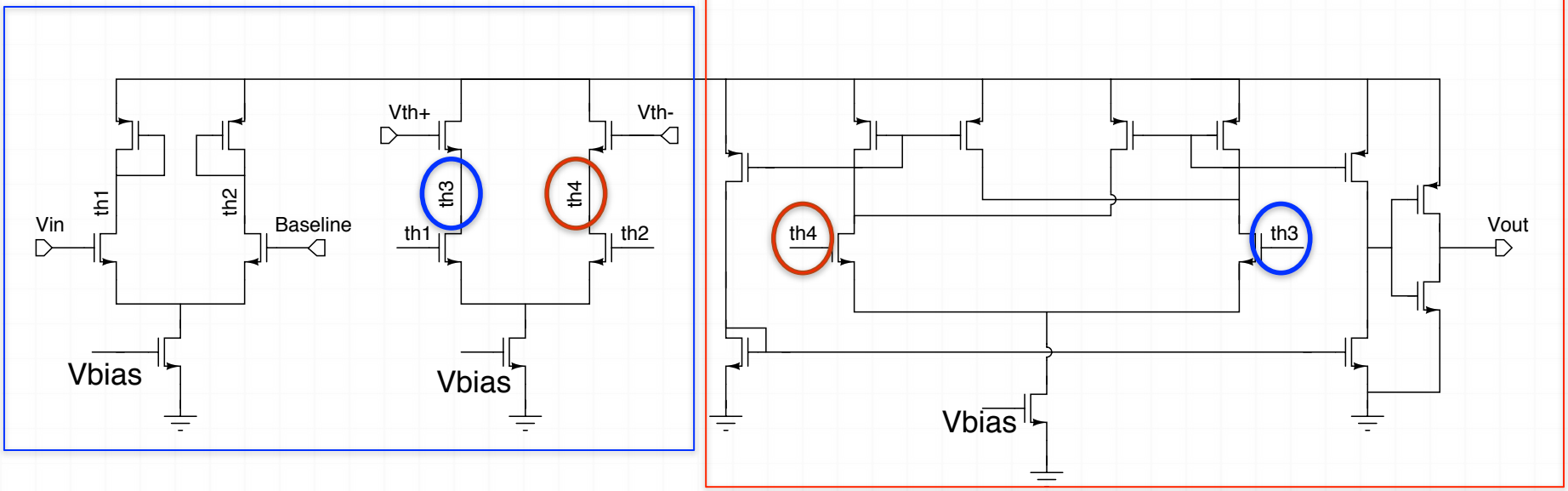


- The first part converts Vin from single ended to differential
- The second part is necessary to set a differential threshold

Complete Hysteresis Comparator

Differential Stage

Comparator Stage



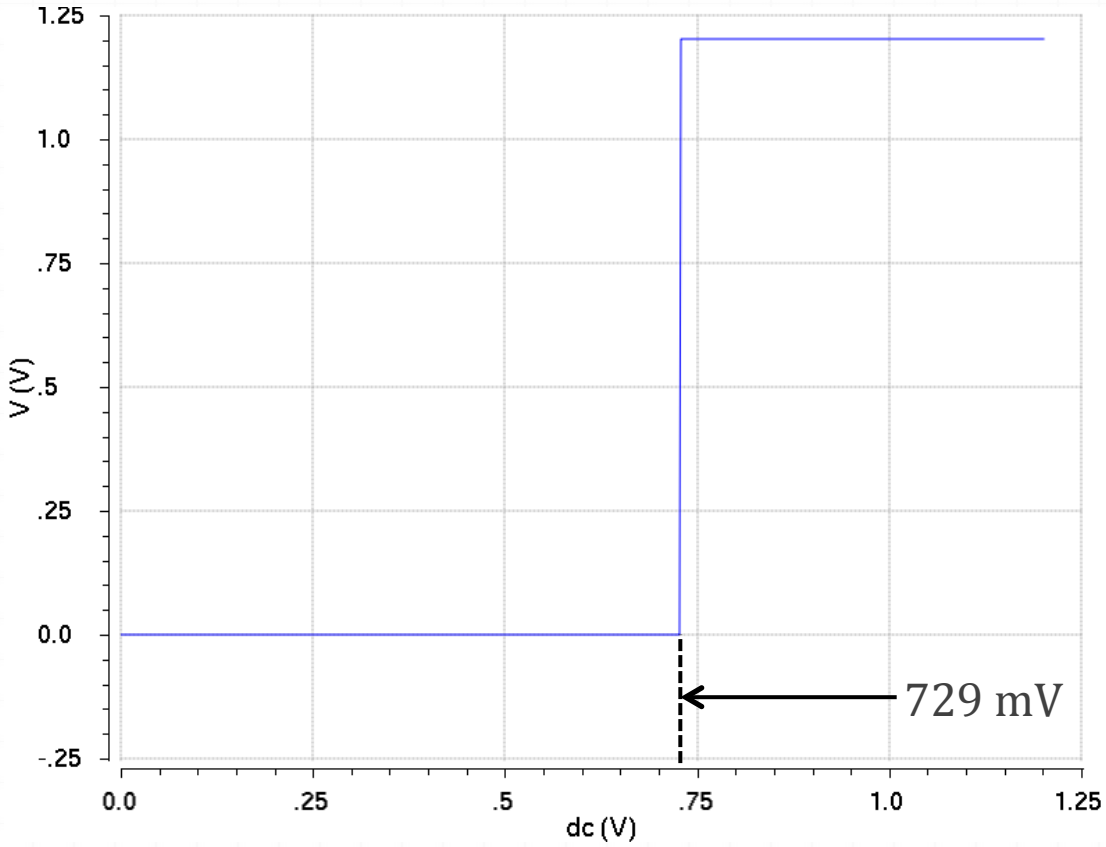
Theoretical Threshold

A = 2.612

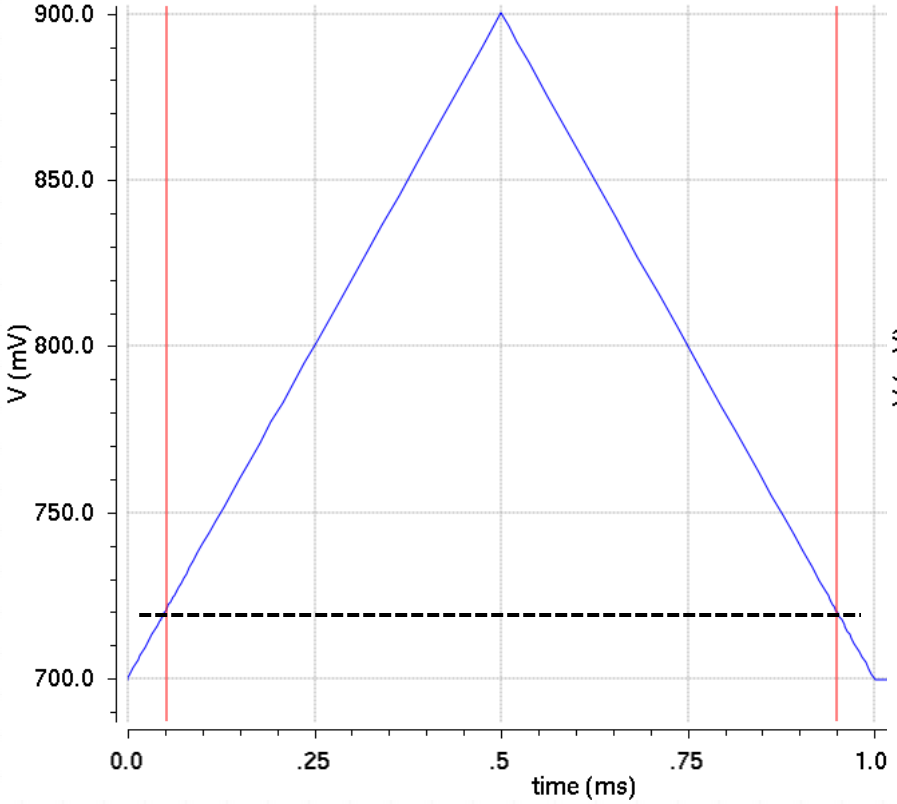
Baseline=700 mV

$(V_{th+}-V_{th-}) = 60$ mV

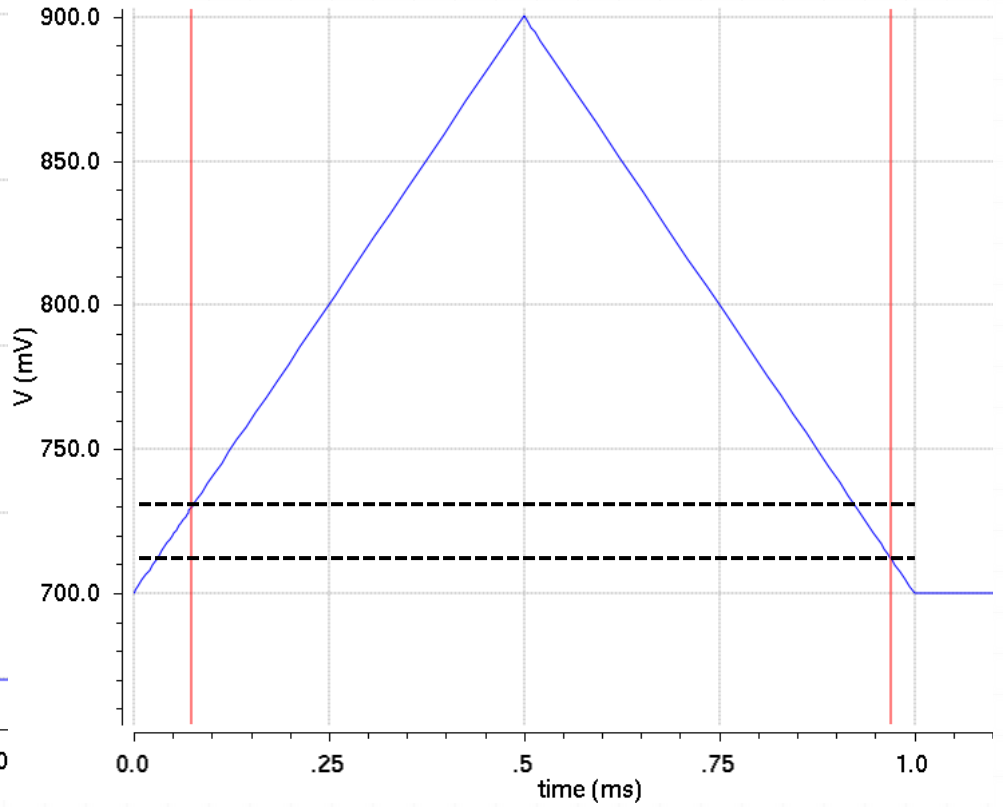
V_{th}= 22.89 mV + Baseline



Hysteresis Comparator II



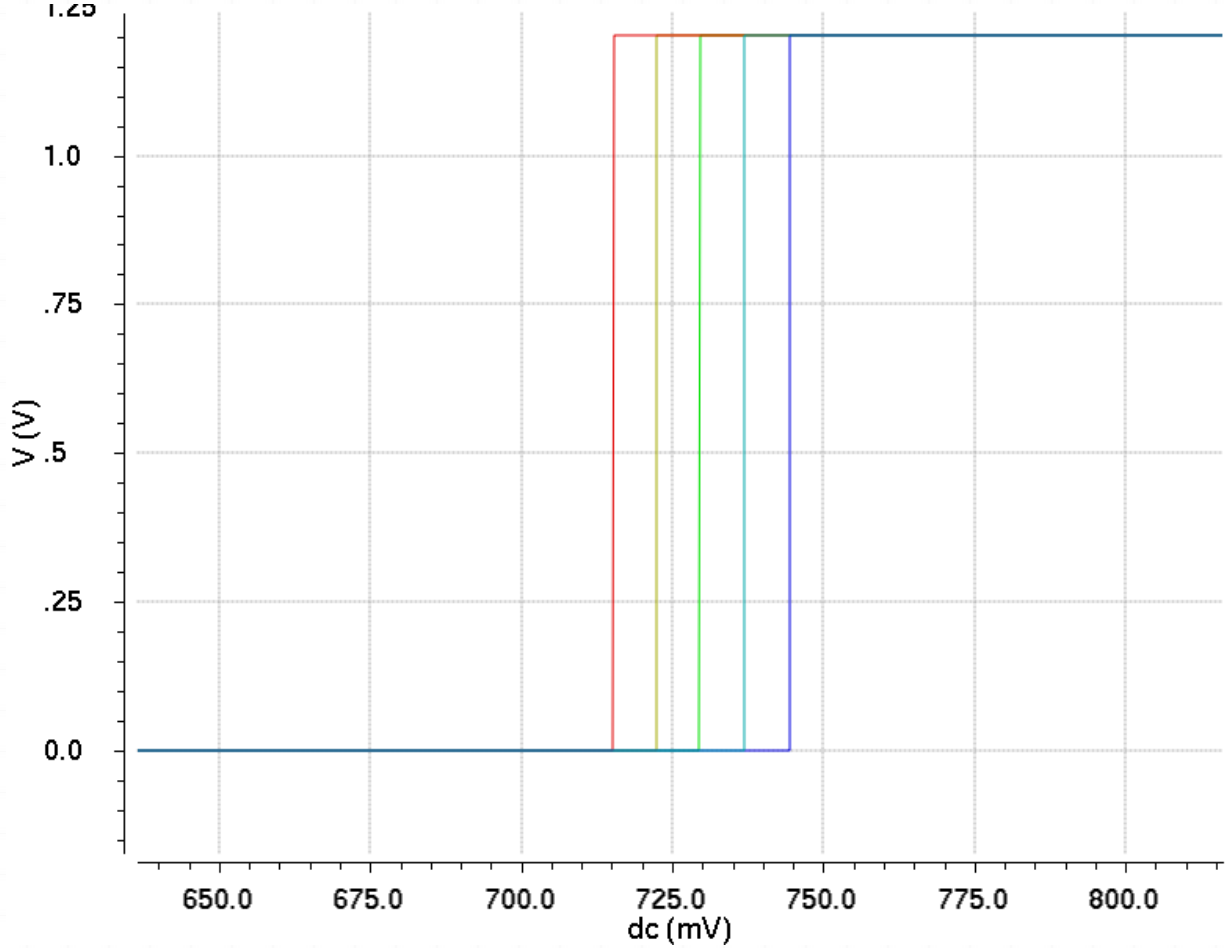
Without Hysteresis



With Hysteresis

Sweep Threshold

V_{th+}-V_{th-}
10mV
20mV
30mV
40mV
50mV



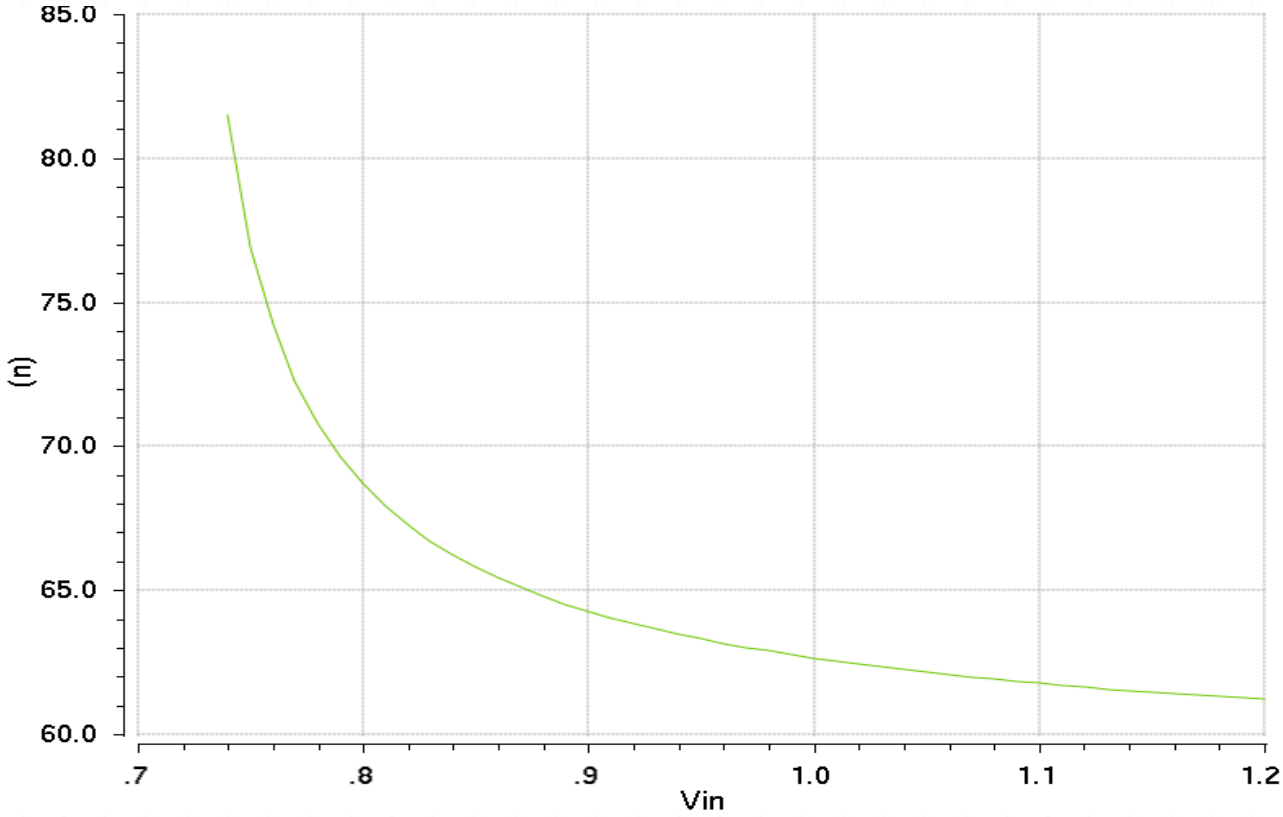
Time Walk

Vin = (700 ÷1200) mV

Rise Time = 23 ns

Fall Time = 100 ns

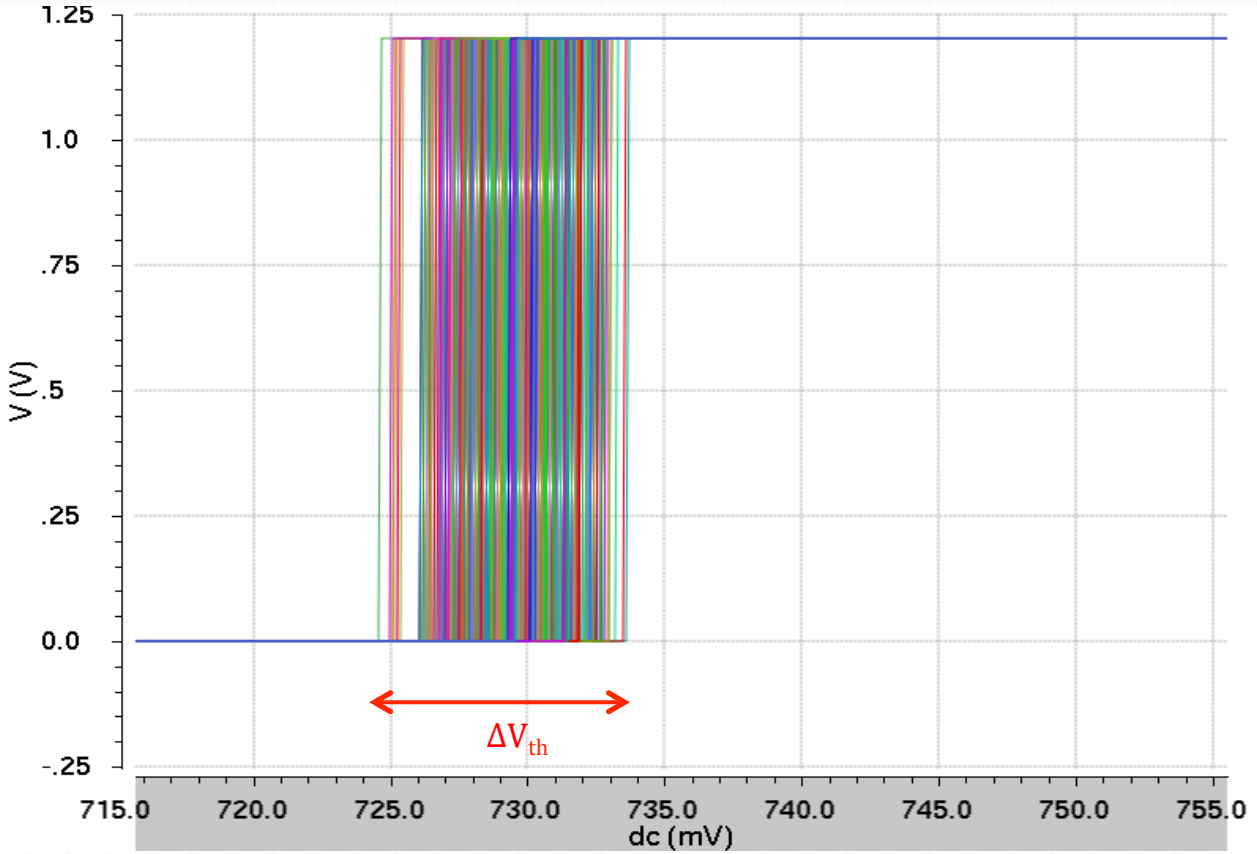
Time Walk = 20 ns



The time walk must be comparable with the rise time

Montecarlo Simulations

$\Delta V_{th} \sim 8$ mV



DAC Parameters

LSB* = ½ rms noise

Noise ~(2-4) mV

LSB = 2mV

Number of Bits:

Typical values for this kind of architecture is in the range 3-4 bits

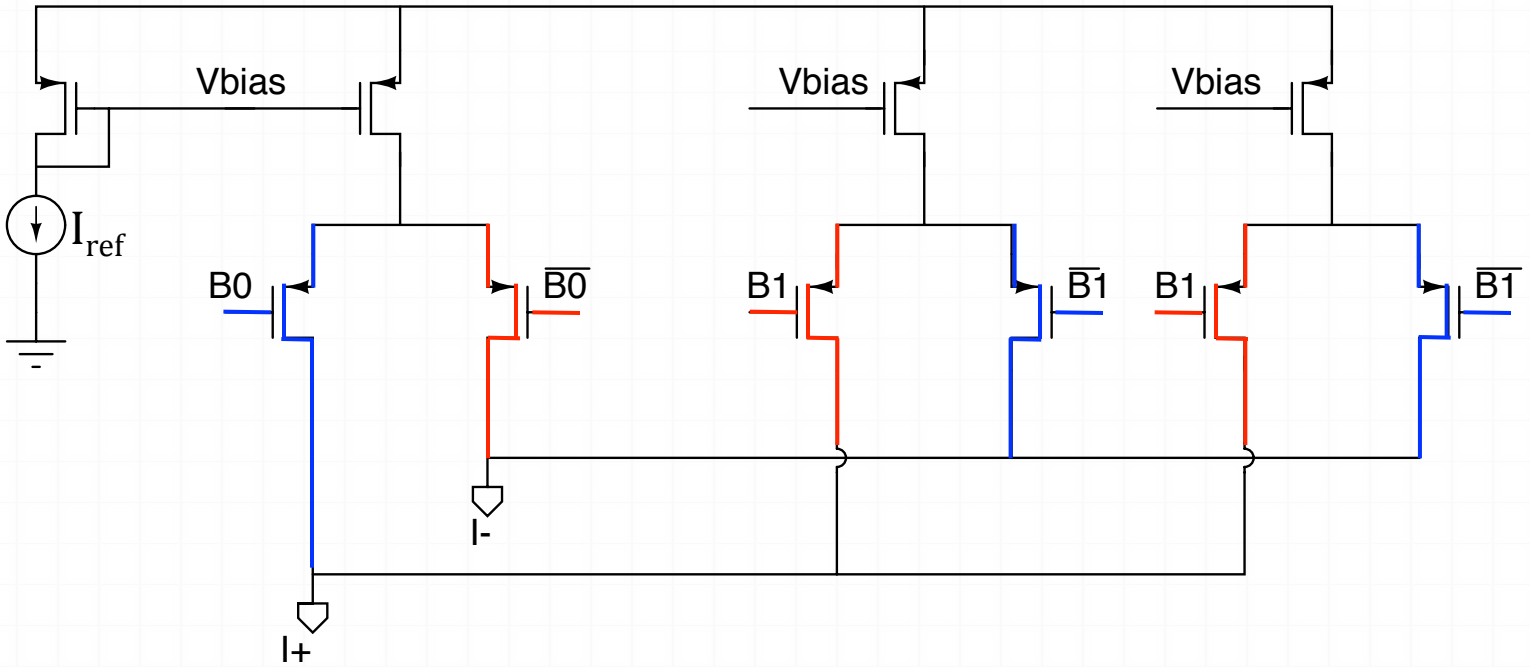
4 bits

* Least Significant Bit

Differential DAC

Standard configuration: 10

B1 B0



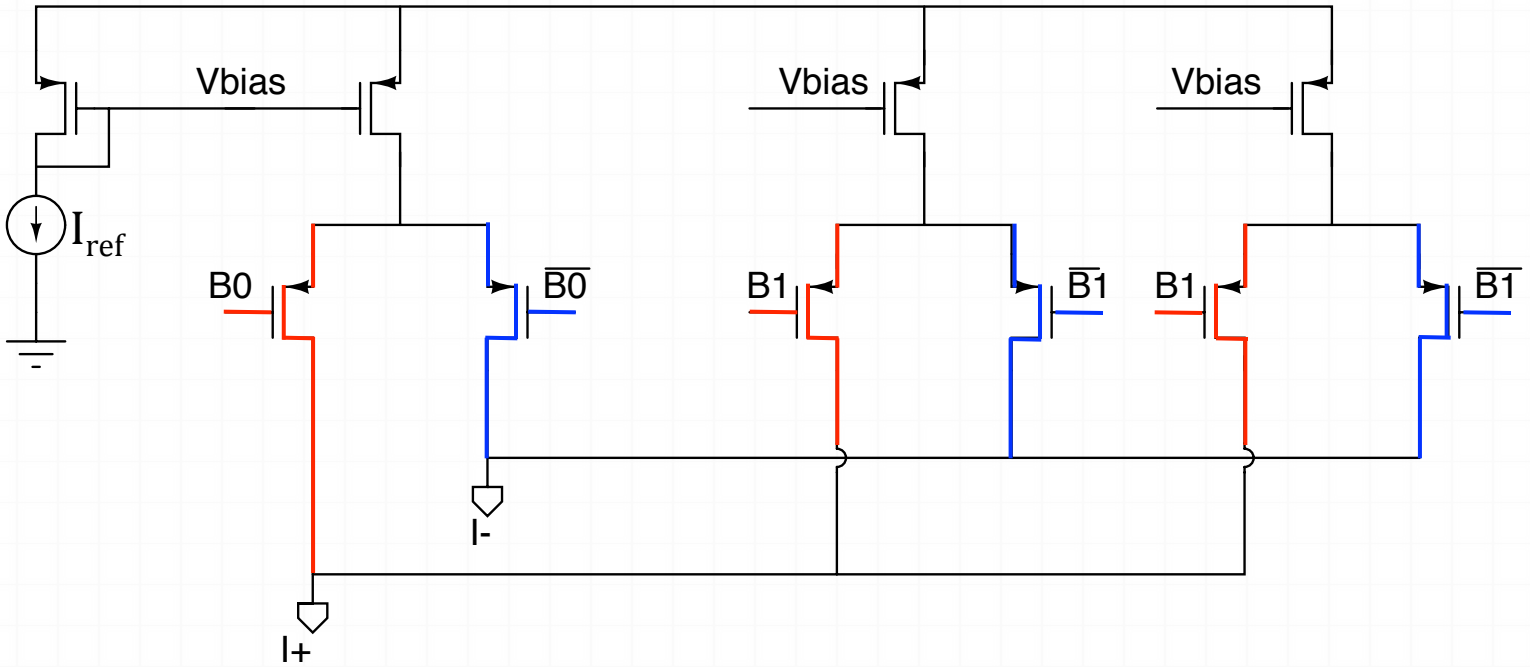
$I_- = 2\ I_{ref}$

$I_+ = 1\ I_{ref}$

Differential DAC

Standard configuration: 11

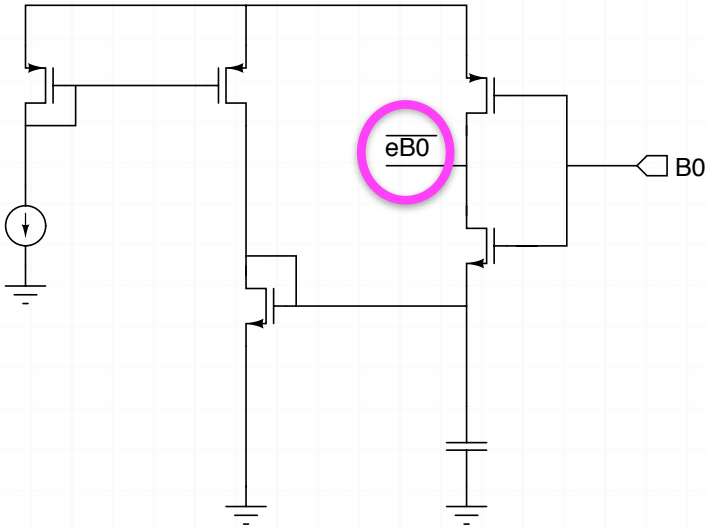
B1 B0

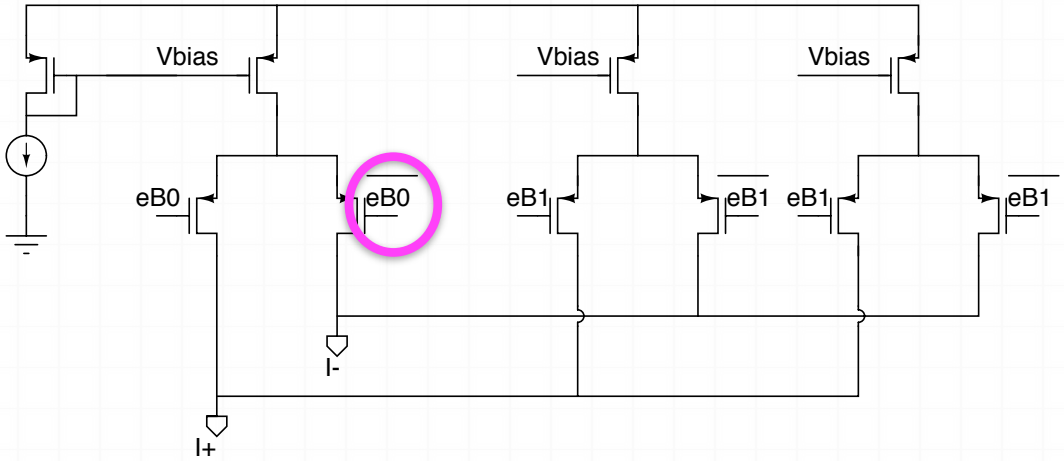


$I_- = 3\ I_{ref}$

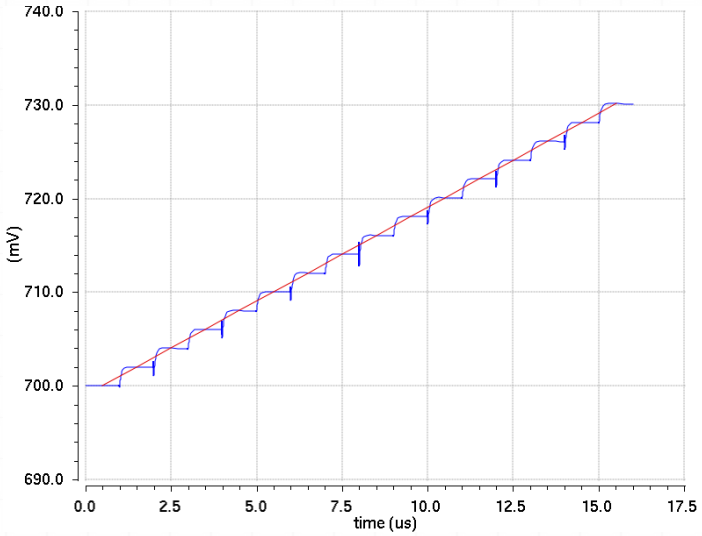
$I_+ = 0\ I_{ref}$

DAC Output Resistance

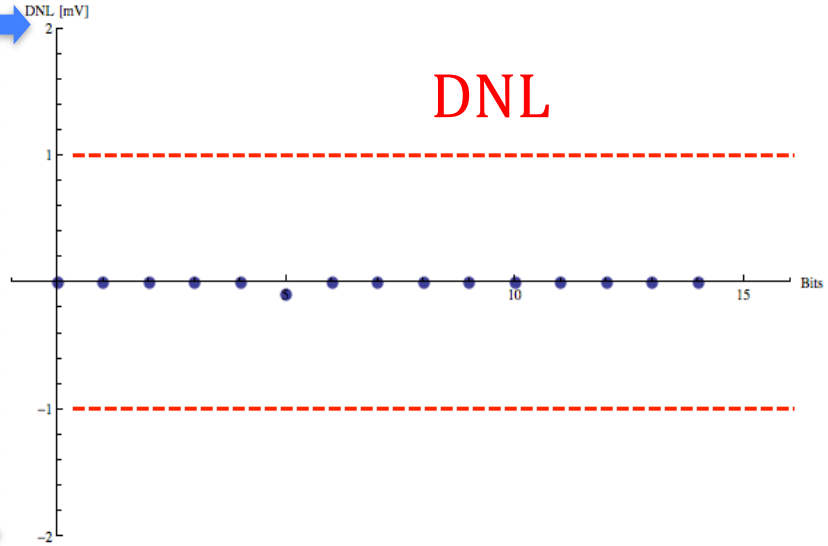




Nonlinearity



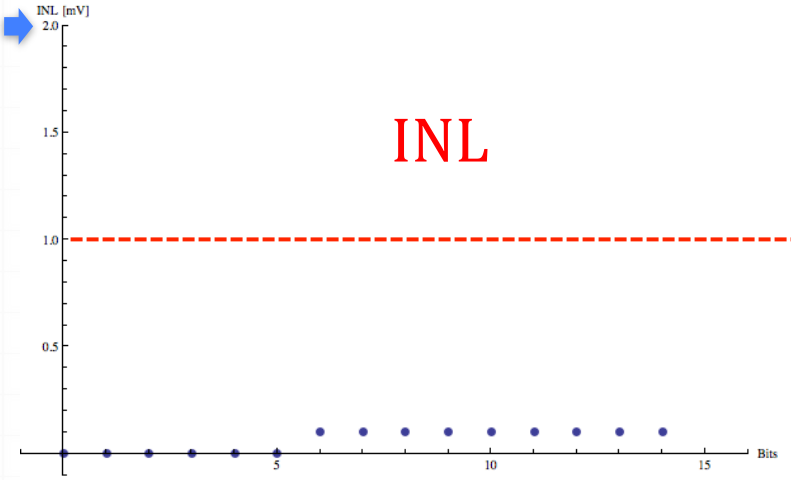
LSB



DNL

-LSB

LSB

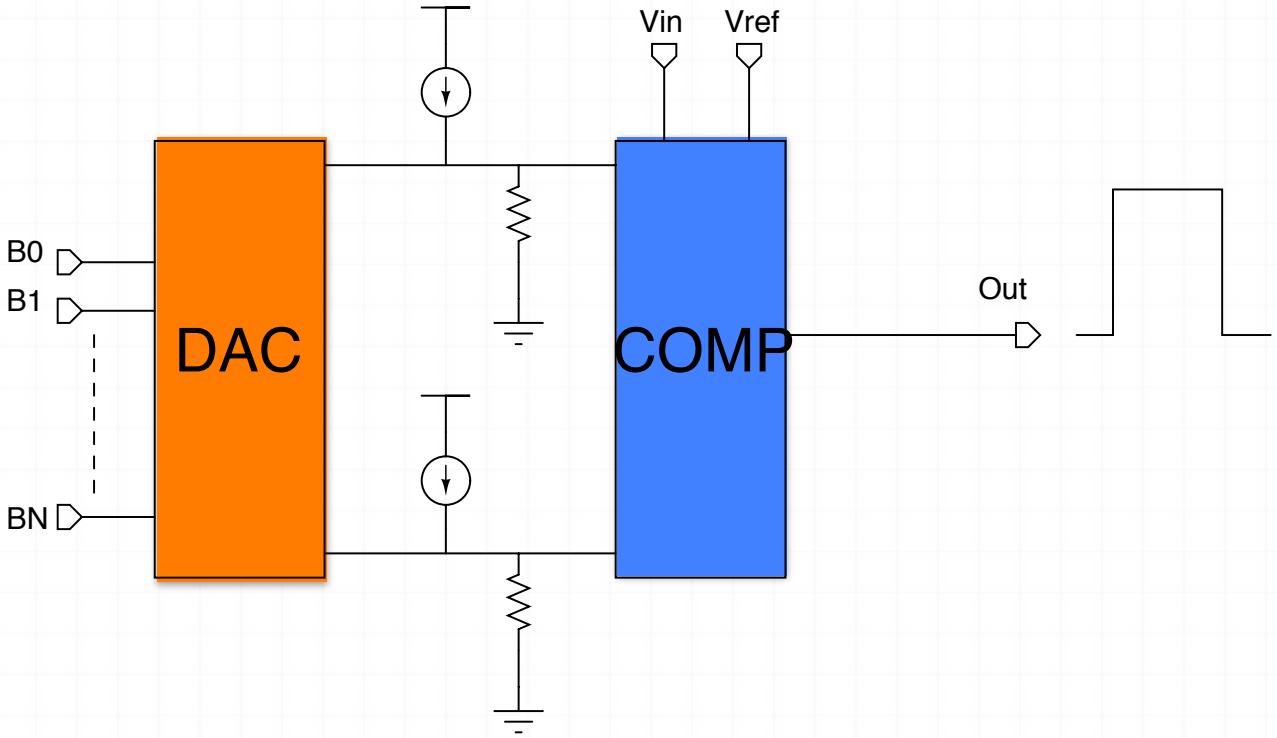


INL

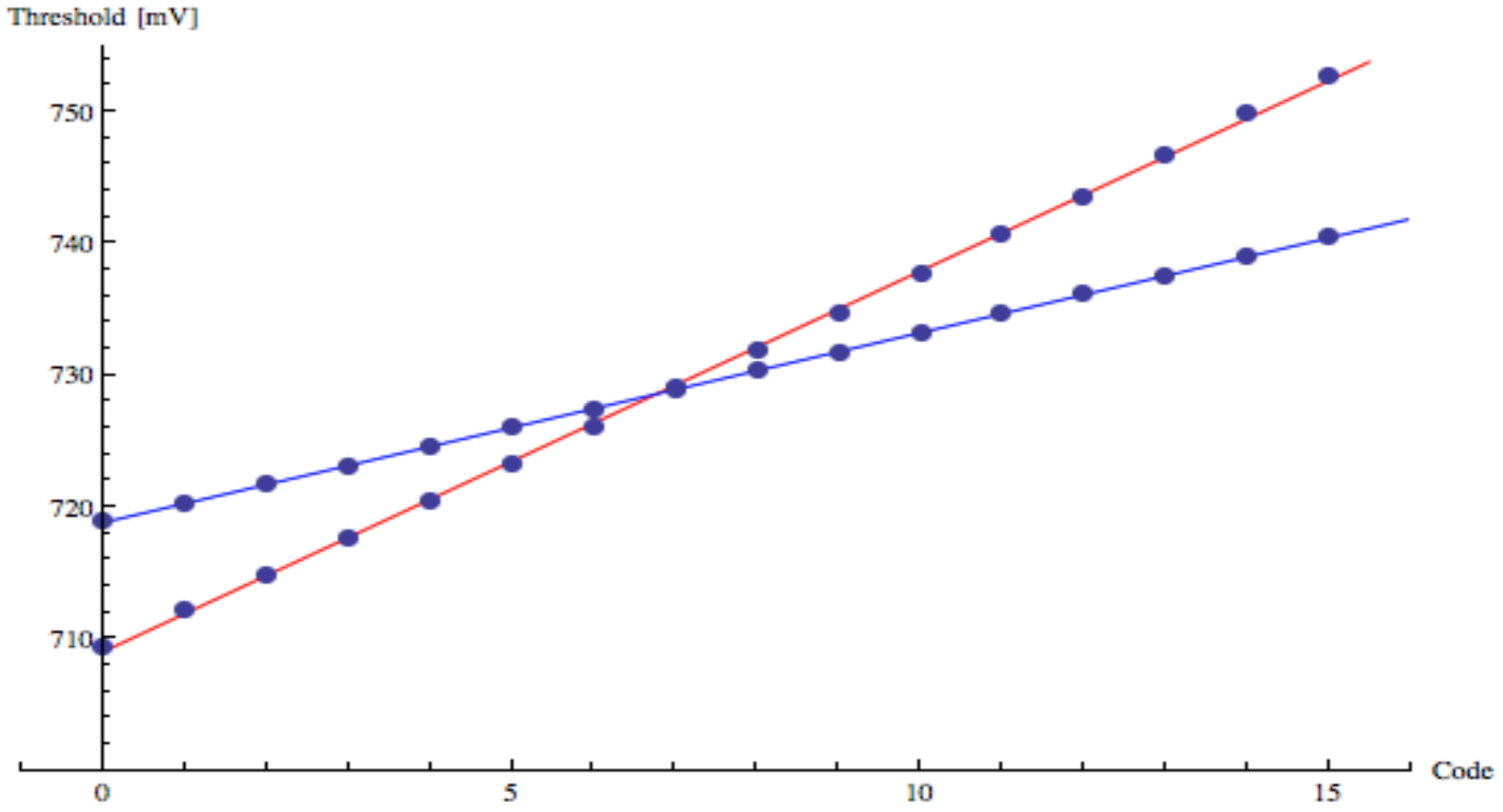
DNL = differential nonlinearity

INL = integral nonlinearity

Complete Architecture



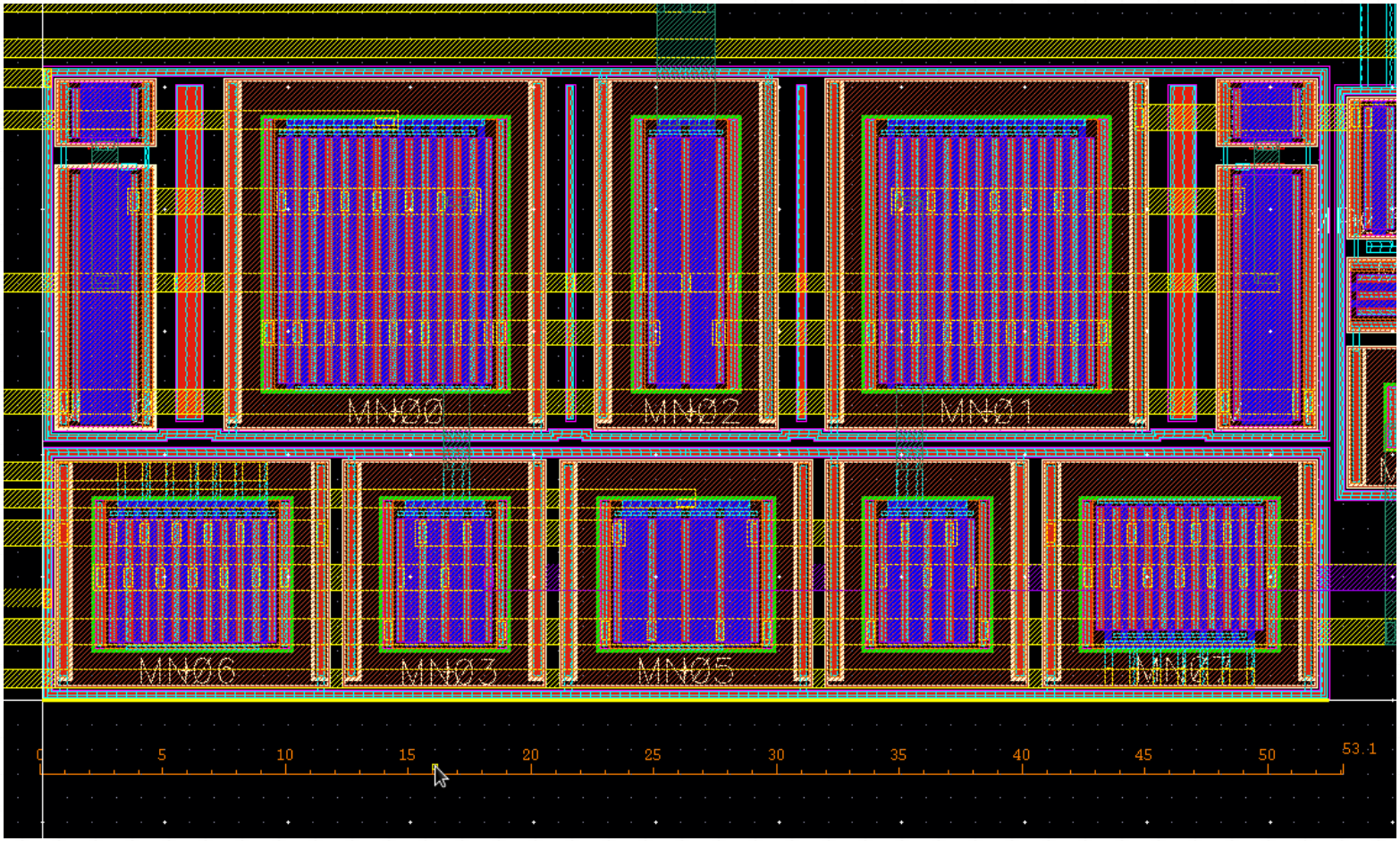
Comparator and DAC Simulations



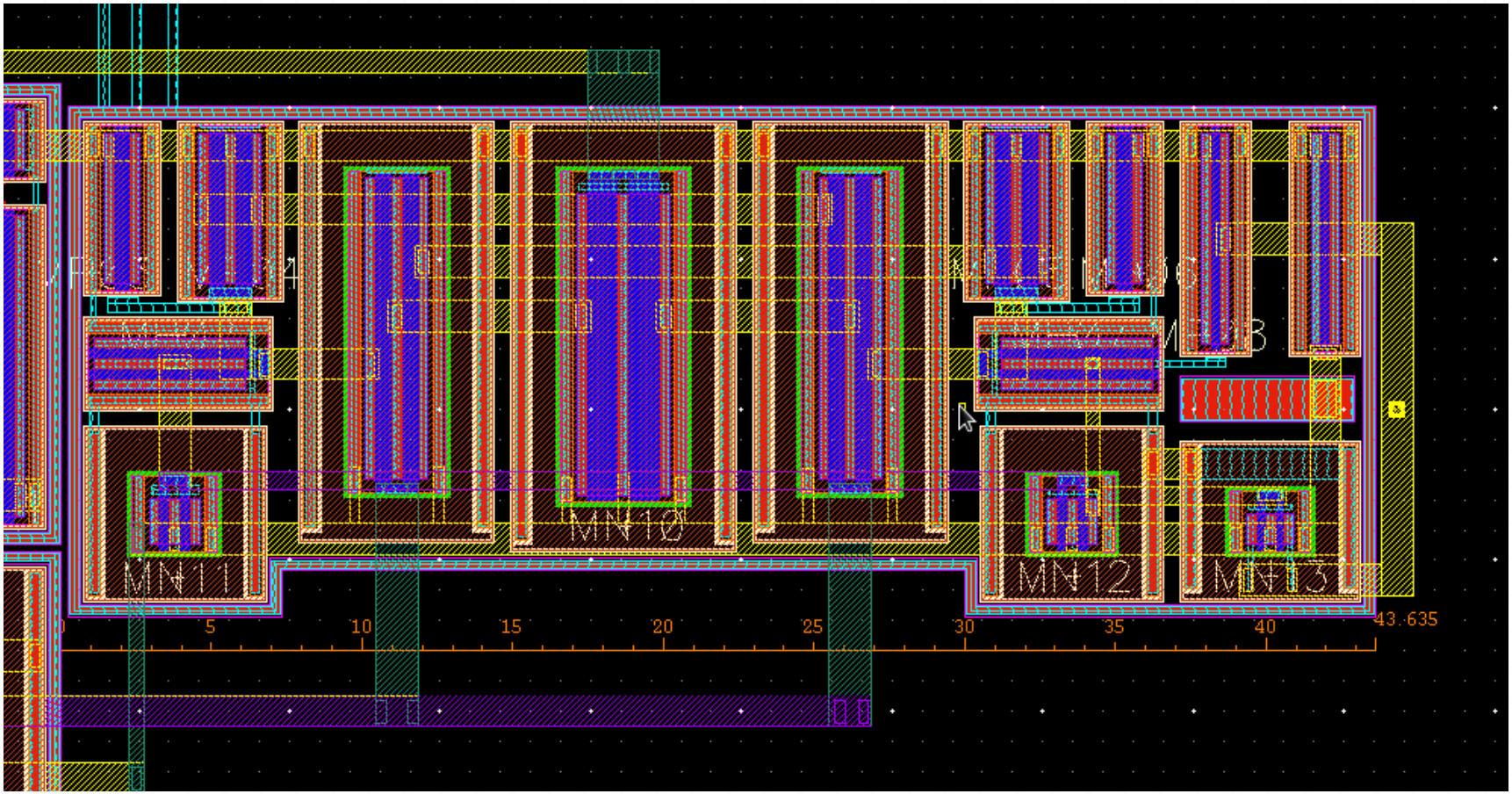
b = 1.439 mV/bit
LSB = 2 mV

b = 2.880 mV/bit
LSB = 4 mV

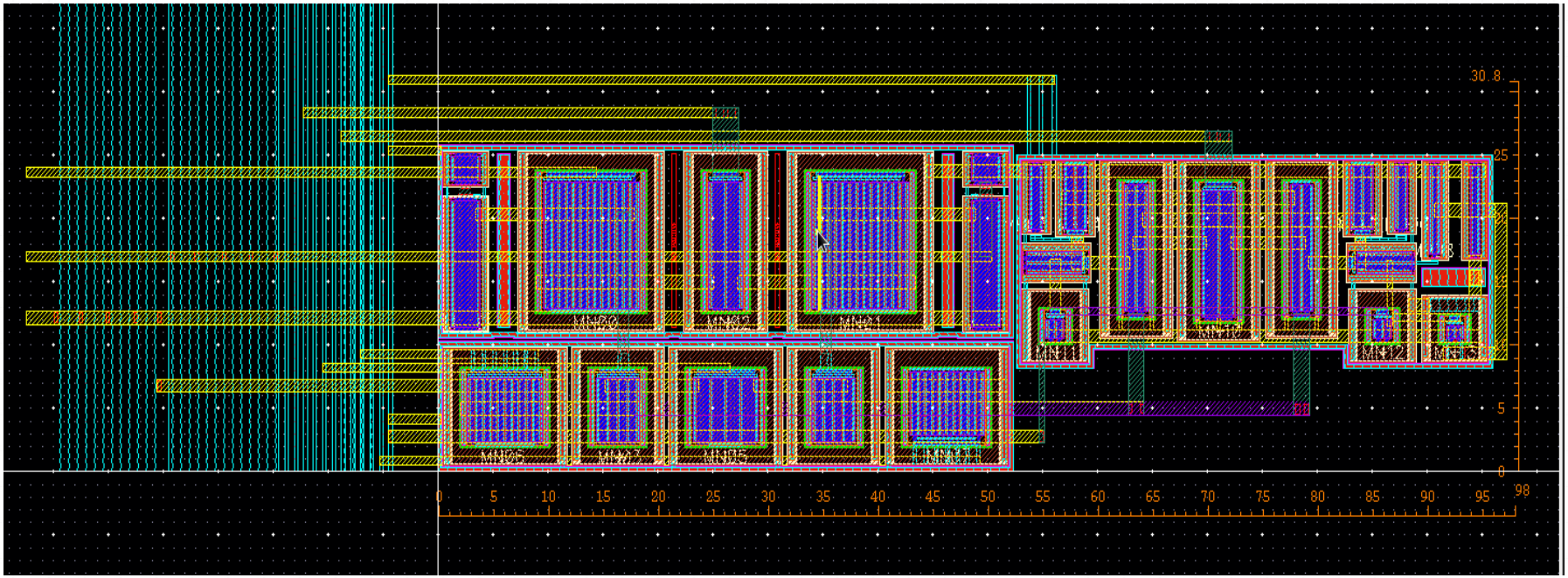
Layout I


MN00
MN02
MN01
MN06
MN03
MN05
MN04
0
5
10
15
20
25
30
35
40
45
50
53.1

Layout II



Layout III

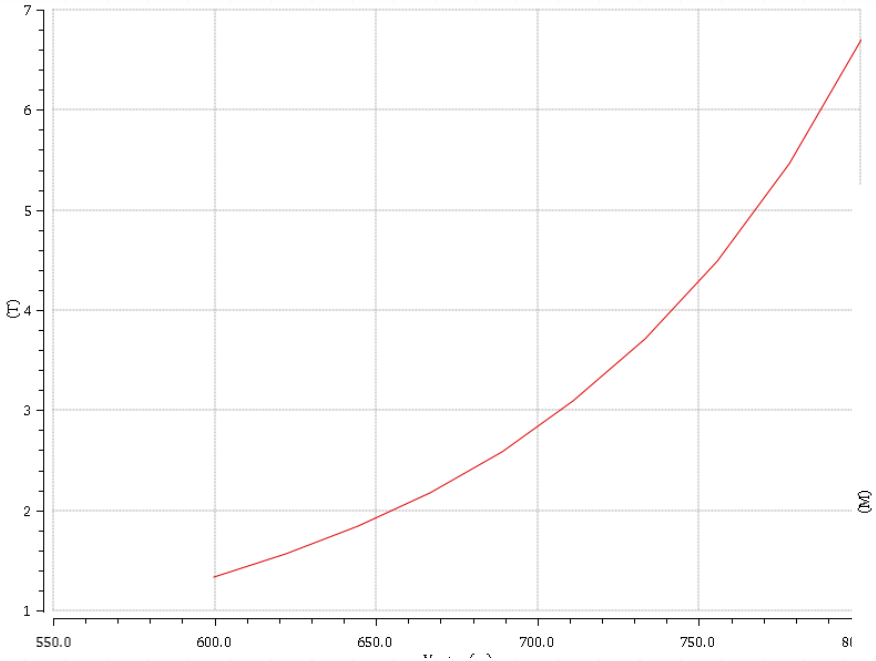


Conclusions

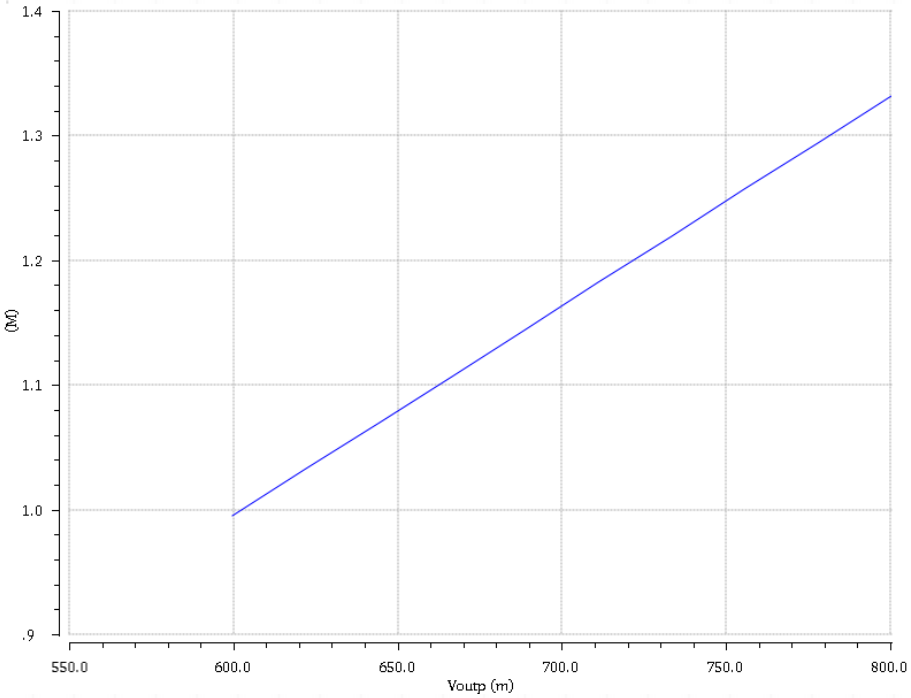
- The Hysteresis comparator is basically complete
- It's necessary to improve the analog TDC be ready for the layout design.

Thanks for your attention!

DAC Output Resistance

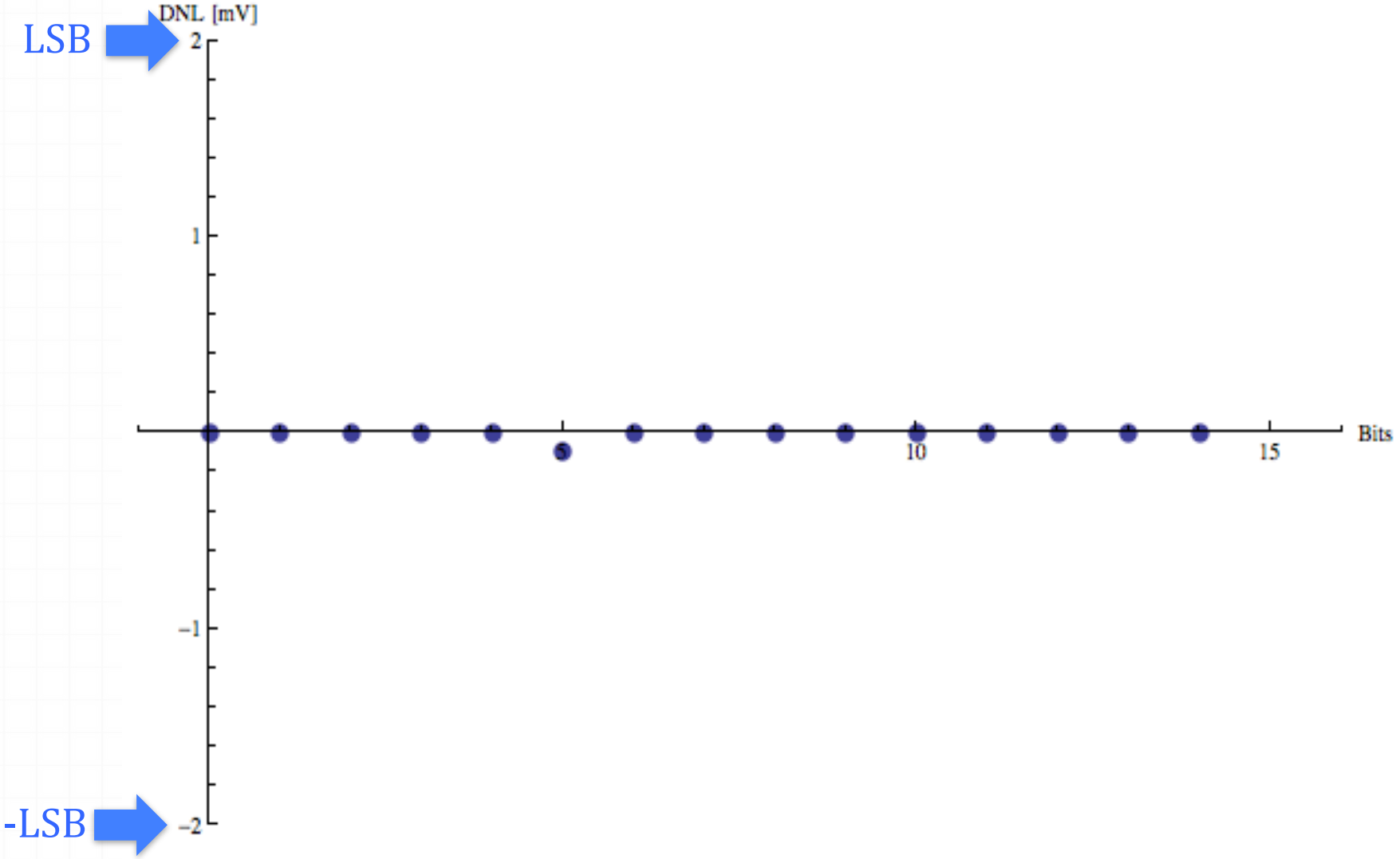


Rout open mode > 1 TΩ



Rout open mode > 1 MΩ

DNL



INL

LSB