JÜLICH
FORSCHUNGSZENTRUM

panda

Status of PASTA Development

Progress in Digital Part and Design Decisions

André Goerres

10 December 2013

47. PANDA Meeting (@ GSI), MVD Session

Content

- Concept of the chip
- Geometry design decision
- Progress on digital development
  - TDC control
  - Global controller
  - Input generator

Requirements of the MVD to Readout

- No central trigger information
  - ⇒ Autonomous data taking
- High event rate ($2 \cdot 10^7$ collisions per second)
  - ⇒ Minimized dead time — < 6 µs
  - ⇒ High rate capability — 40.000 s^{-1}
- Event building afterwards
  - ⇒ Accurate time information — < 10 ns
- Support event identification
  - ⇒ Measure charge deposition — ≥ 8 bit over dyn. range
- MVD as compact as possible
  - ⇒ Low power consumption — < 4 mW/ch

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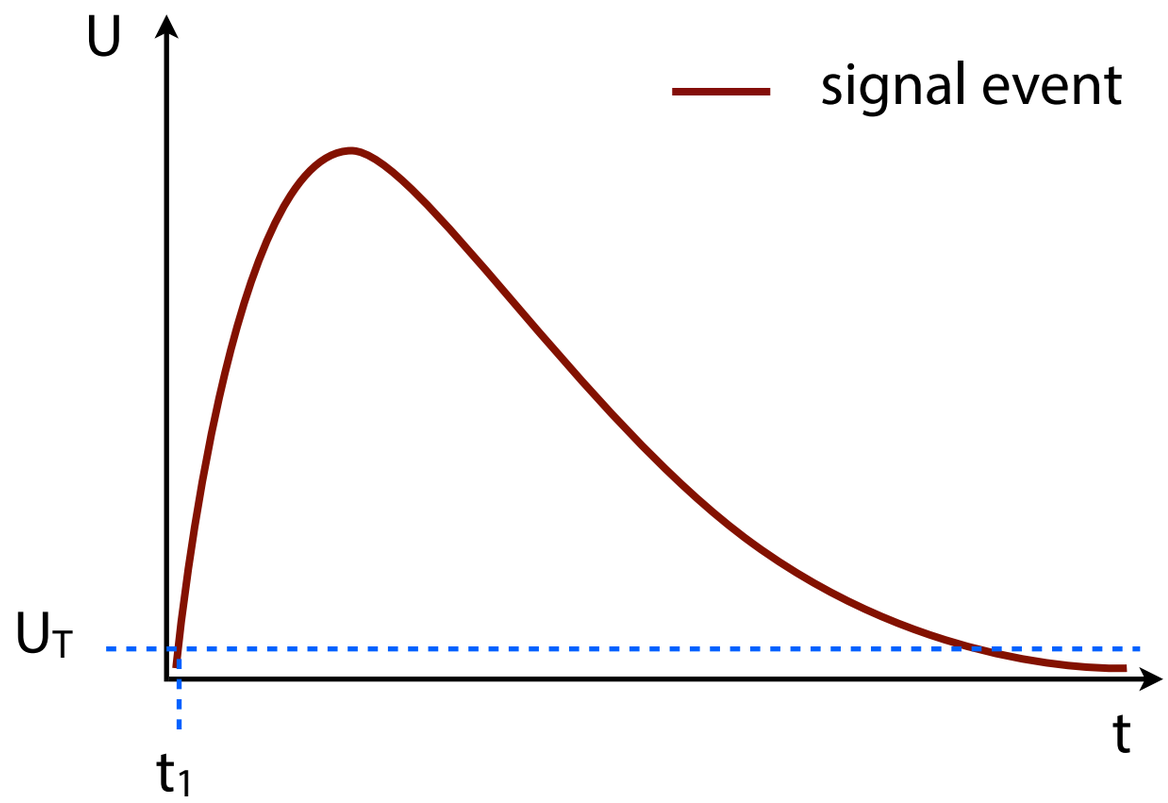
Time-based readout
- Simple & low power
- Experience with concept (TOF-PET ASIC)

Concept of the ASIC

- Time-based readout of silicon strips
  - Save time stamps (50 ps)
  - Leading edge discriminator
  - Charge by time over threshold



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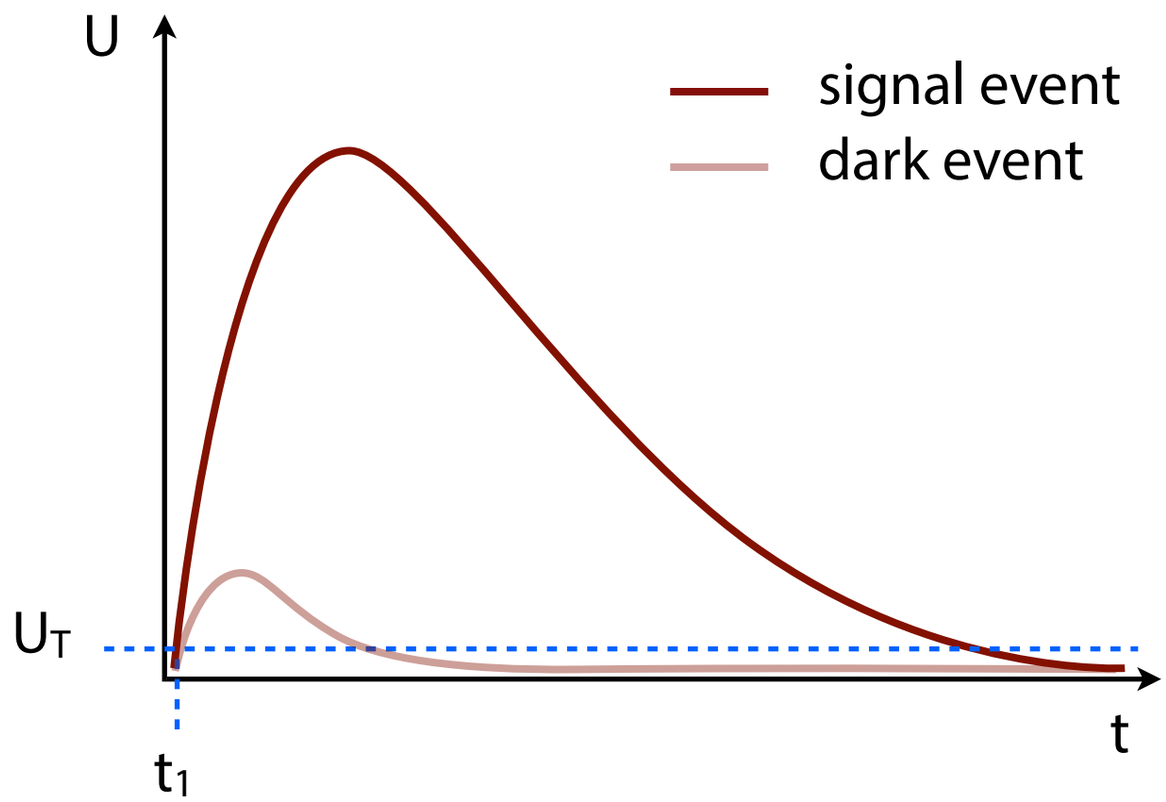

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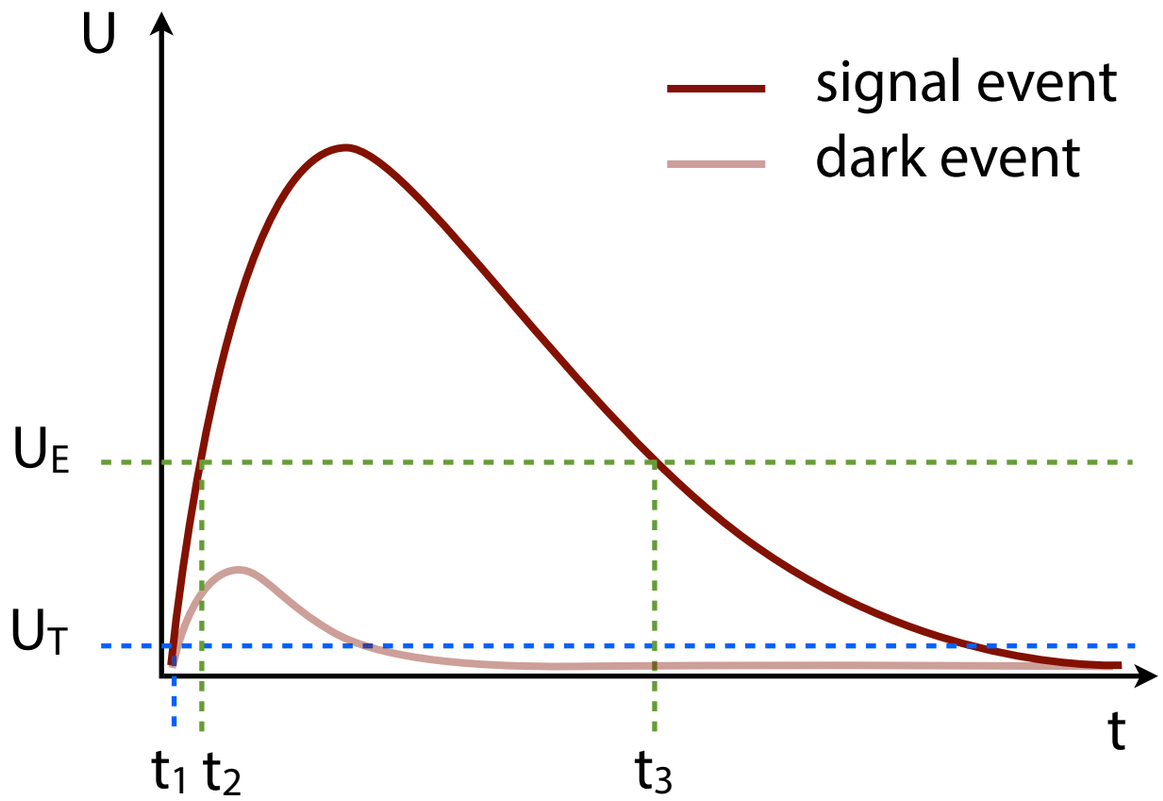

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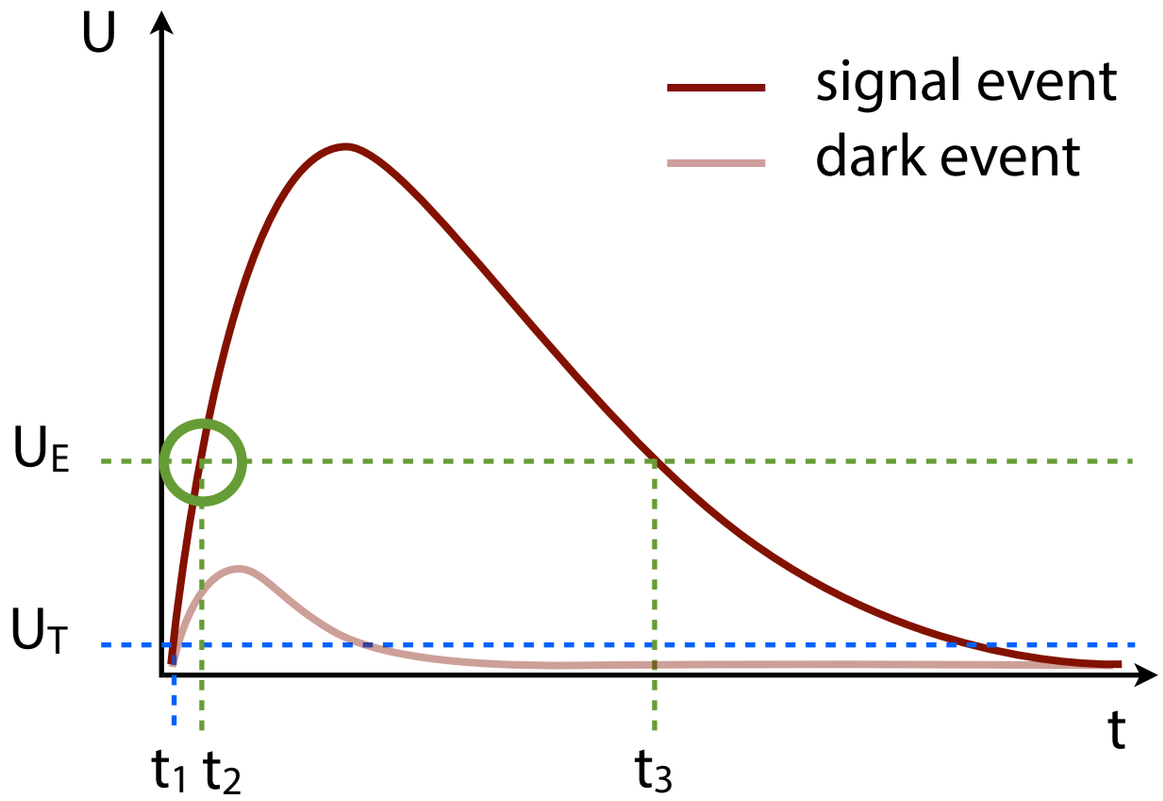
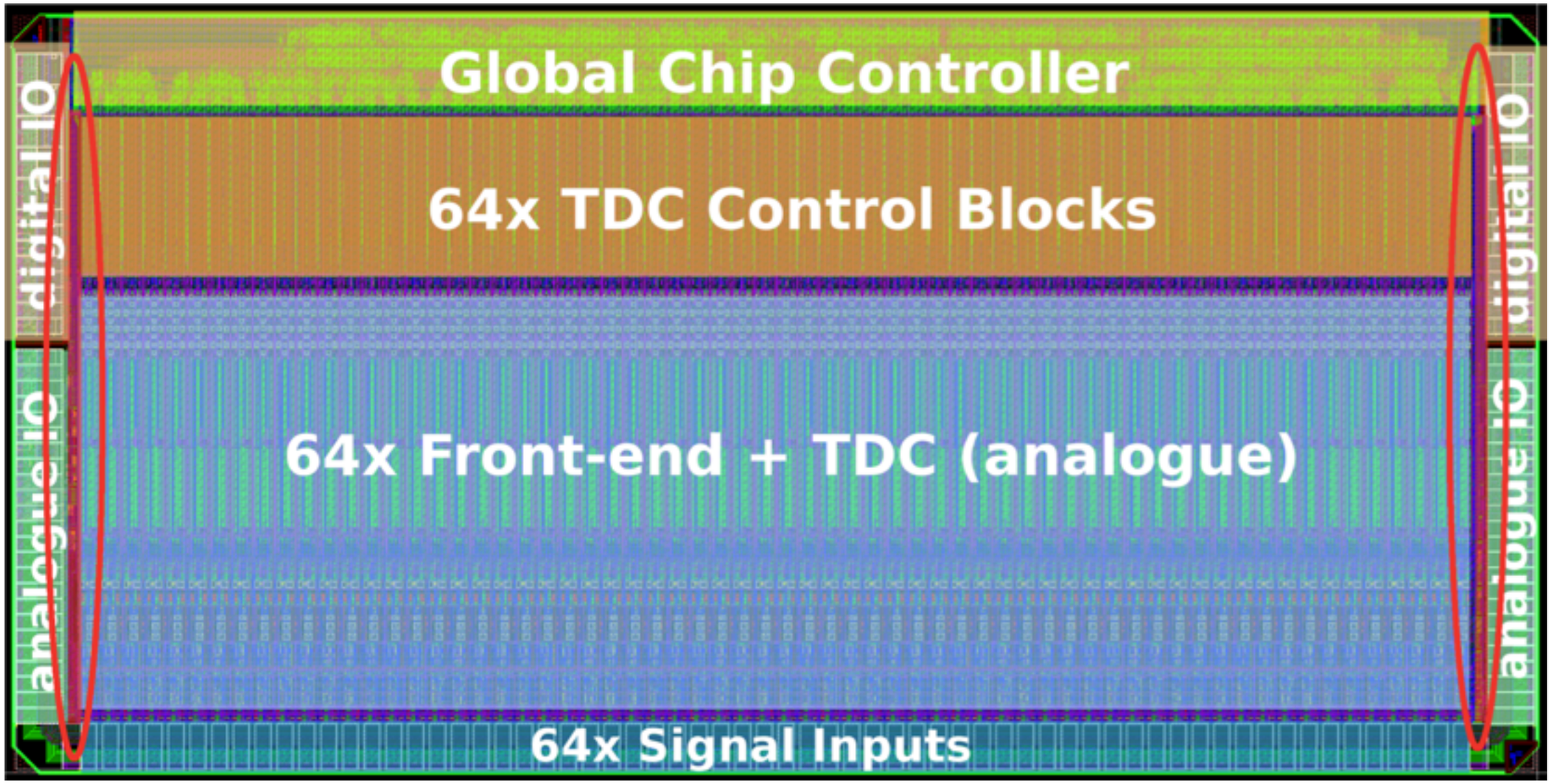


- Two TDCs per channel
  - Time and energy branch
    (low and high threshold)
  - Energy trigger (t_2)
    validates time trigger (t_1)
  - Reduces susceptibility to dark counts

- Concept already realized: TOF-PET ASIC

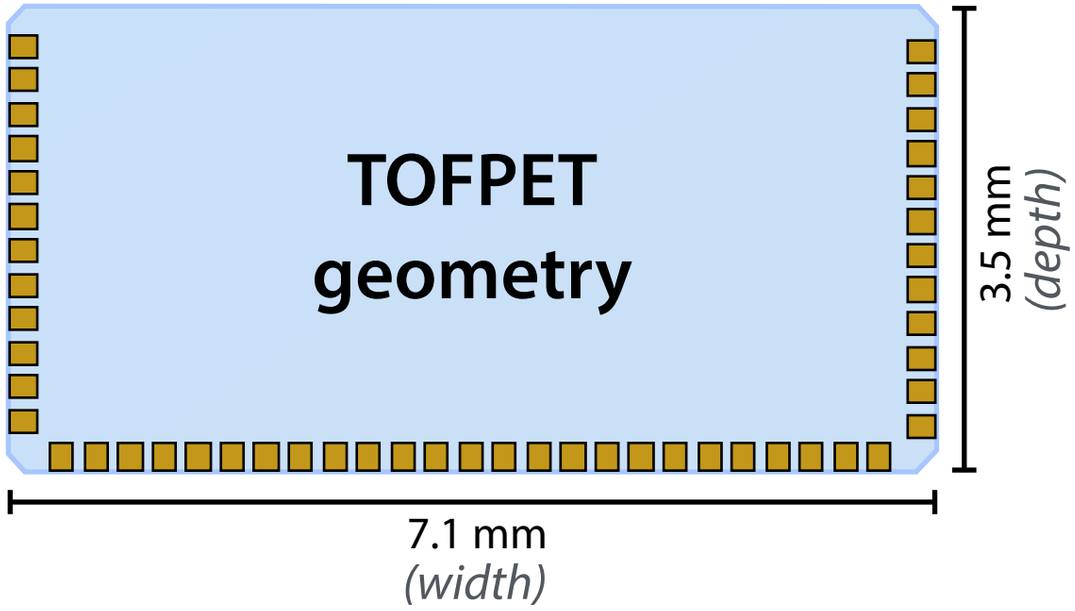
Floorplan of TOF-PET ASIC

- CMOS 130 nm, 64 channels on 25 mm^2
- One pad-free edge to attribute two twin chips back-to-back



Red ellipses: bias and calibration circuitry

Geometrical boundaries



- Limitations due to placement
  - Depth per chip 5-6 mm
    (routing on barrel)
  - Width for all channels 34.5 mm
    (wedge sensors)
  - Space between chips ~ 400 µm

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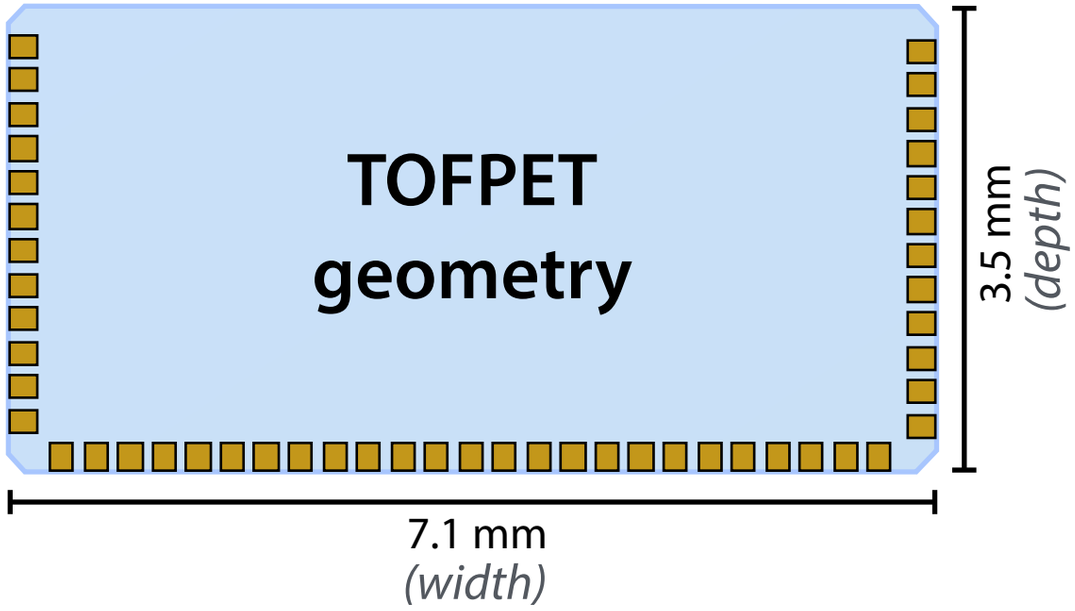

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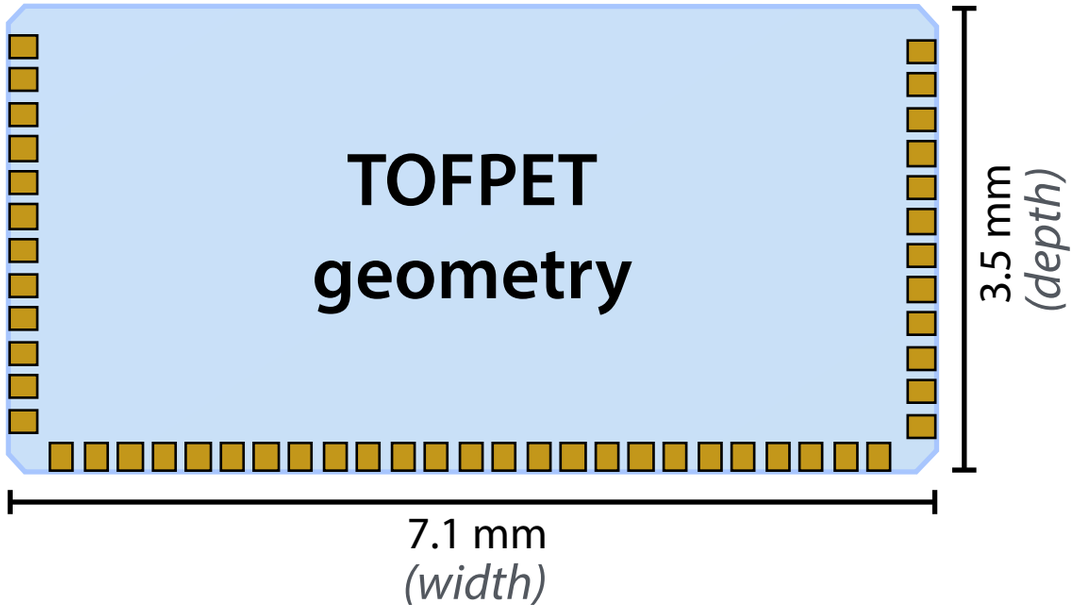

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  - Rim around chip: ~ 200 µm
  - Bonding pads width: 60 µm
    (also for fitting everything inside)
  - Production grid in dev. run:
    5 x 5 mm

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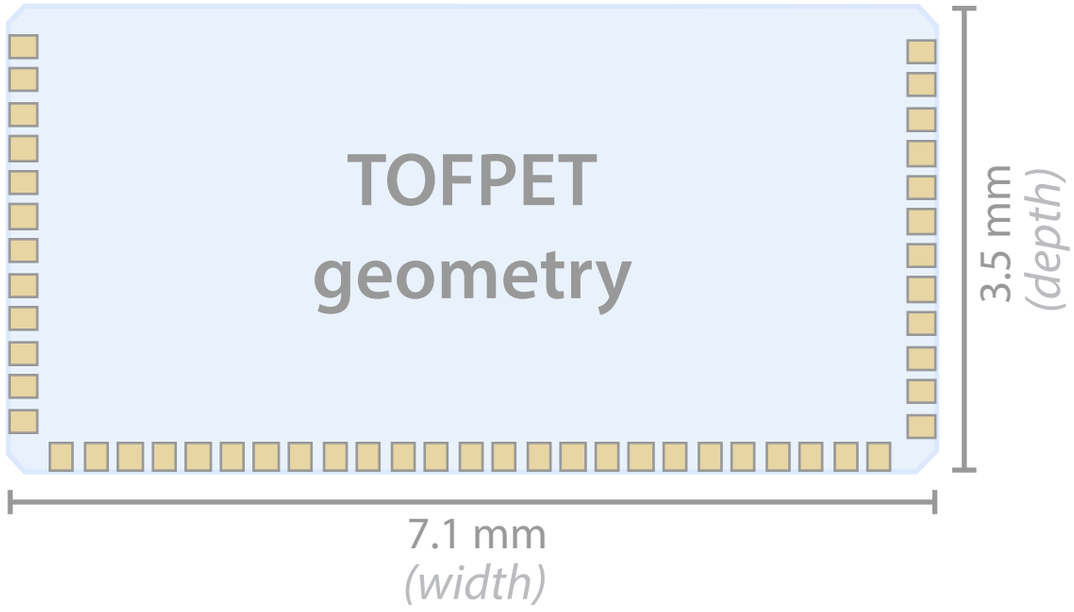

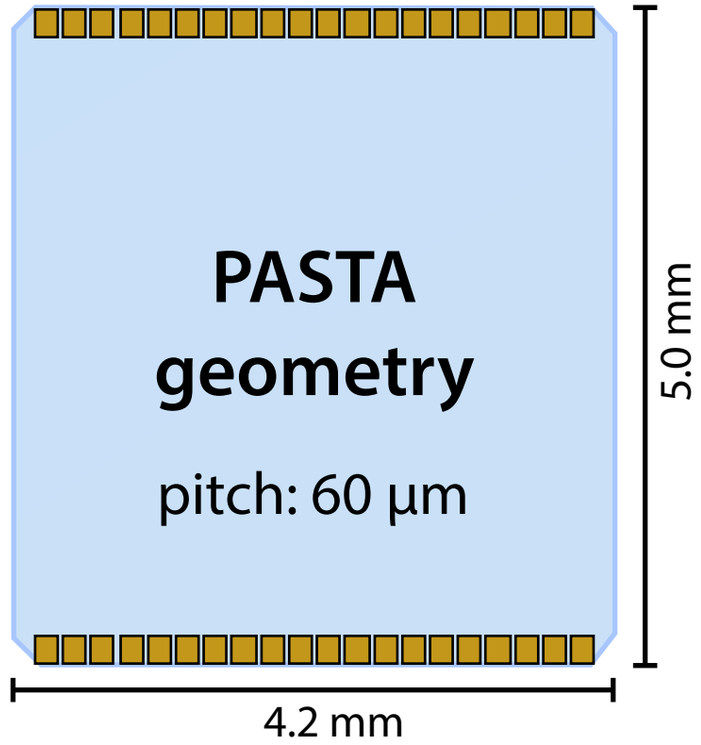

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Situation for Wedged Sensors

- Original design:
  - 512 channels per sensor, 67.5 µm pitch
  - readout every channel

⇒ 8 ASICs with < 50 µm input pitch

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  - 768 channels per sensor, 45 µm pitch
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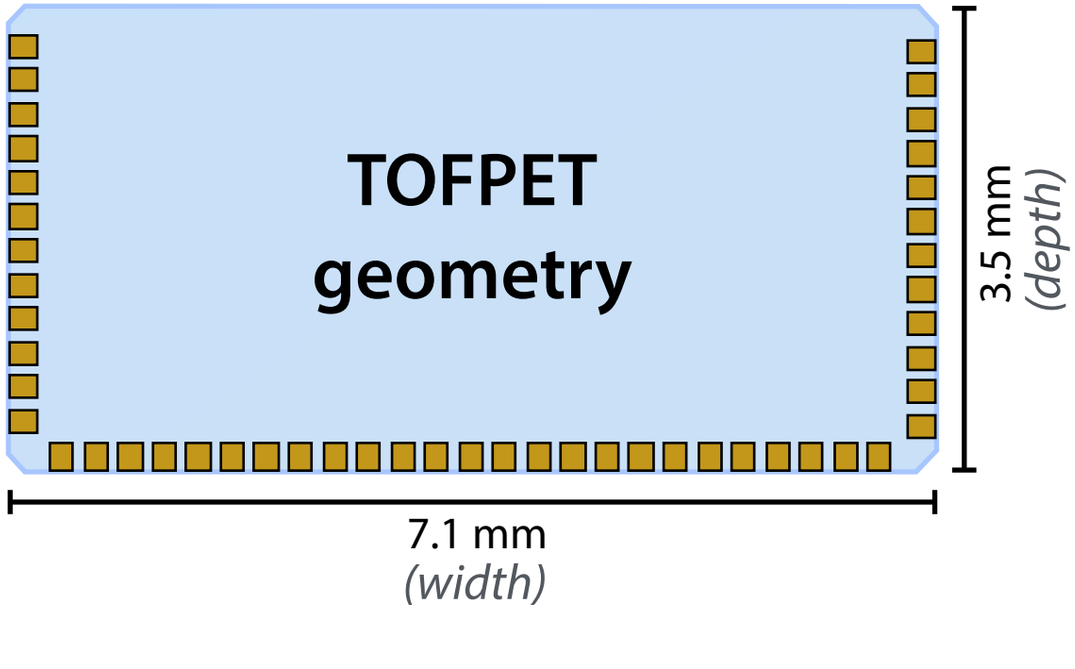
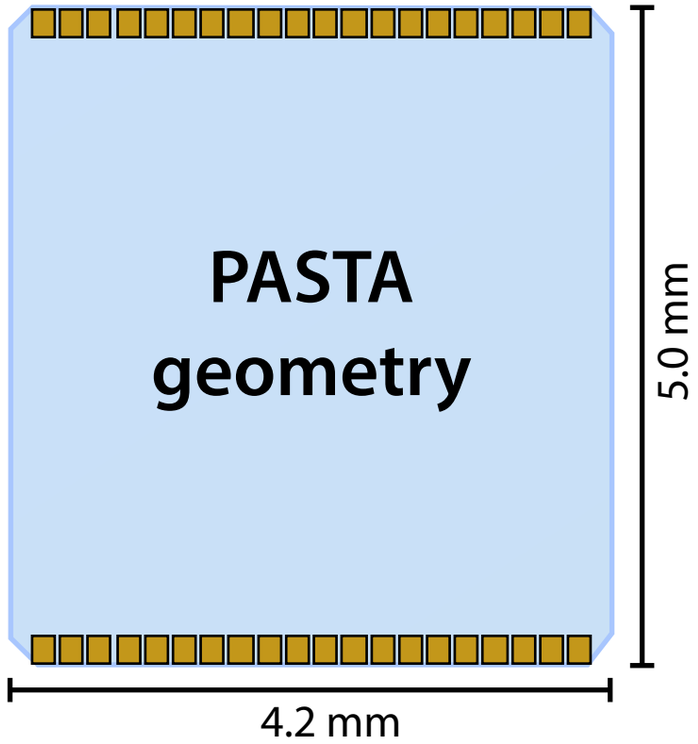
- Simulations (H.-G. Zaunick)
  - Spatial resolution of floating channel to direct readout: Worse by ~20 %

r/o pitch (µm)	worst RMS resolution $\frac{p}{\sqrt{12}}$ (µm)	nr. of intermediate strips	SNR	spacial resolution RMS (µm)
65	18.8	0	10	16.09 ± 0.02
			16	13.08 ± 0.02
			25	10.63 ± 0.01
130	37.5	0	10	34.70 ± 0.05
			16	31.64 ± 0.04
			25	29.28 ± 0.04
130	37.5	1	10	24.92 ± 0.03
			16	16.13 ± 0.02
			25	12.11 ± 0.02

Geometrical boundaries





- Footprint: $7.1 \times 3.5\ mm^2 \rightarrow 4.2 \times 5.0\ mm^2$
  ($25\ mm^2 \rightarrow 21\ mm^2$)
- Smaller channel pitch: 102 µm → 60 µm
- Position of bonding pads: front, sides → front, back

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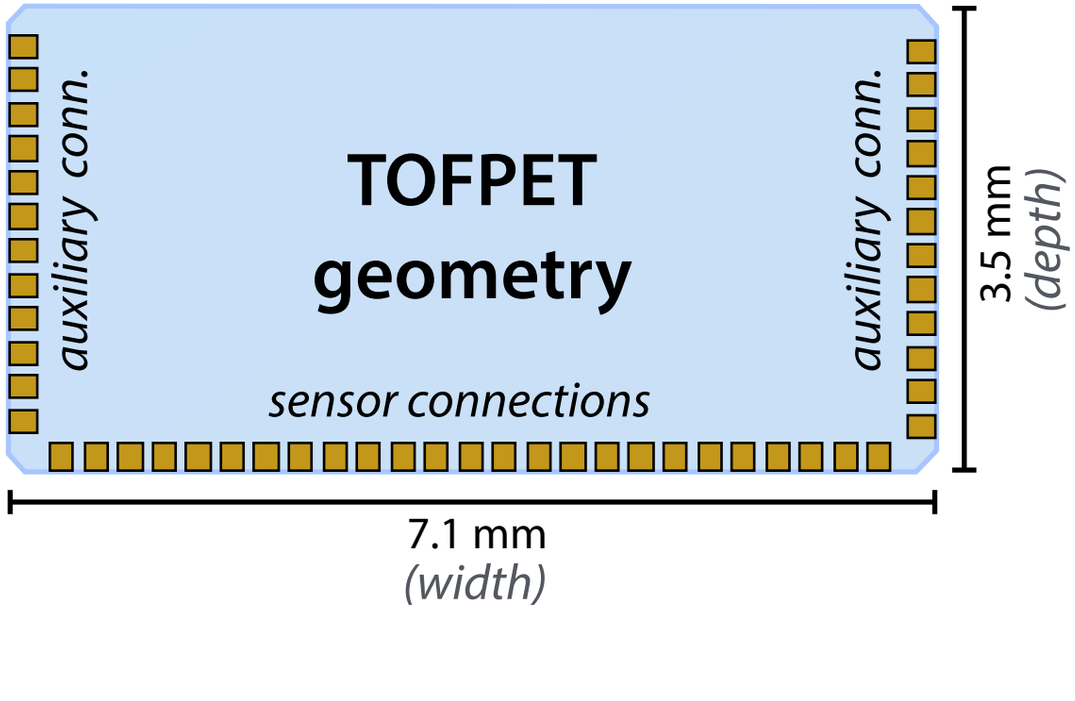

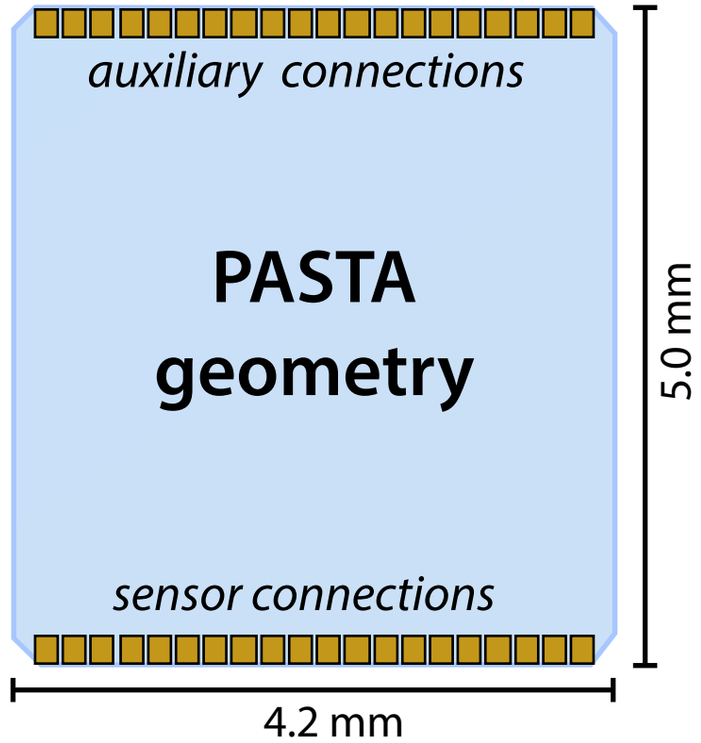

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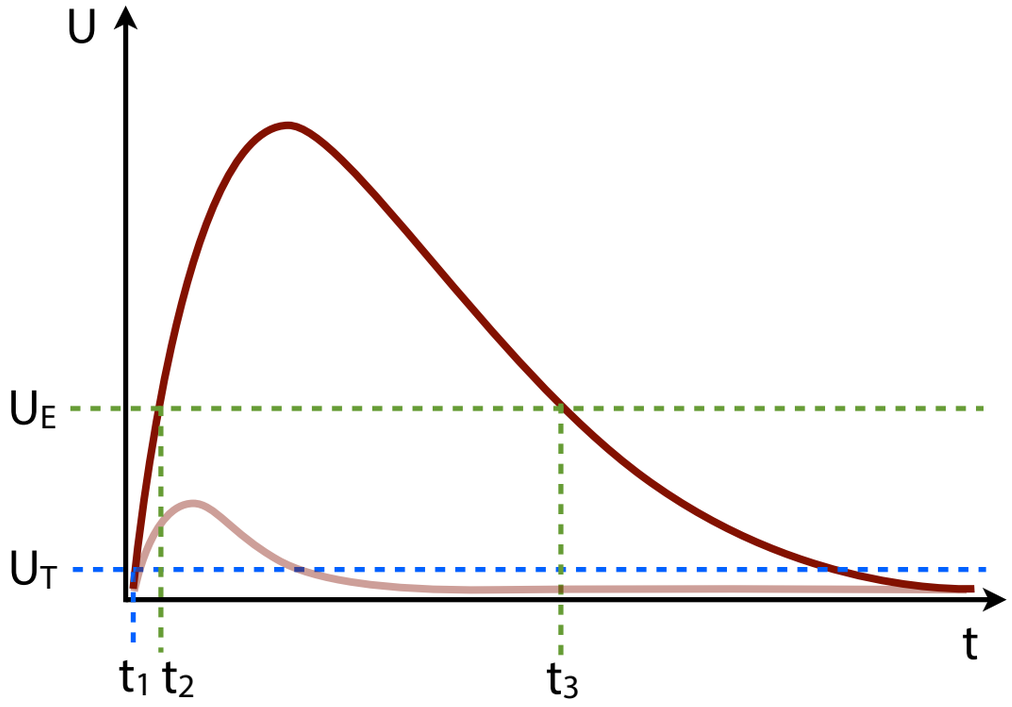
Some Conceptual Differences

- **New TDC control** (clearer & simpler structure)
- Time buffers move to global controller
  - Saves connections, speed up simulations
- Hit validation in two ways
  (delayed & synchronous)
- More flexibility what to store
  (t_1-t_3, t_1-t_2, test pulse)
- Optimization in charging time
  - Smaller offset in TAC charging
  - Conversion end on falling edge
- TAC refresh local instead global
  (Capacitors back to reference level after inactivity)



Current Status of TDC Control

- Basic concept is implemented
  - Trigger, TAC selector, charge transfer and measurement, …
- Left to do:
  - Solve inefficiency for events close to clock
  - SEU protection (*TDC CTRL v1* has it, *v2* not yet)

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	TDC_CTRL v1 (incl. SEU, tech. A)	TDC_CTRL v1 (incl. SEU, tech. B)
Occupancy (1.1 x 0.1 mm²)	84.8 %	37.0 %
Cells	3155	2850
Power (@ 160 MHz)	1.57 mW/ch	1.78 mW/ch

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Occupancy (1.1 x 0.1 mm²)	84.8 %	37.0 %	5.6 %
Cells	3155	2850	261
Power (@ 160 MHz)	1.57 mW/ch	1.78 mW/ch	0.05 mW/ch

Estimate for final TDC Control:
Save up to 80-90% in terms of power/occupancy

Current Status of GCTRL

- Global controller merged to TDC_CTRL v2
  - Time stamps moved, different connections, small adaptions
  - Test bench for digital part …

Generator for VHDL Test Bench

- Digital part needs validation
- Test bench
  - Logic behavior of GCTRL and TDC_CTRL
  - Analog behavior emulated
    - Charge proportional to time, gets transferred, …
  - Input: simulated output of discriminators (text file)
- New* tool to generate input
  - Written in python
    - Multithread compatible
  - Internally: generate voltage input
  - Output:
    - Wait time for next discriminator change of state

* based on idea of R. Bugalho

time of arrival time over threshold

```
0.000006520456 0.000000101280
0.000030262739 0.000000104310
0.000035721378 0.000000081840
```

↓

```
000006520900
000000100830
000023641450
000000103860
000005354740
000000081430
```

Code available at: https://github.com/Nepomuk/ASIC_generator

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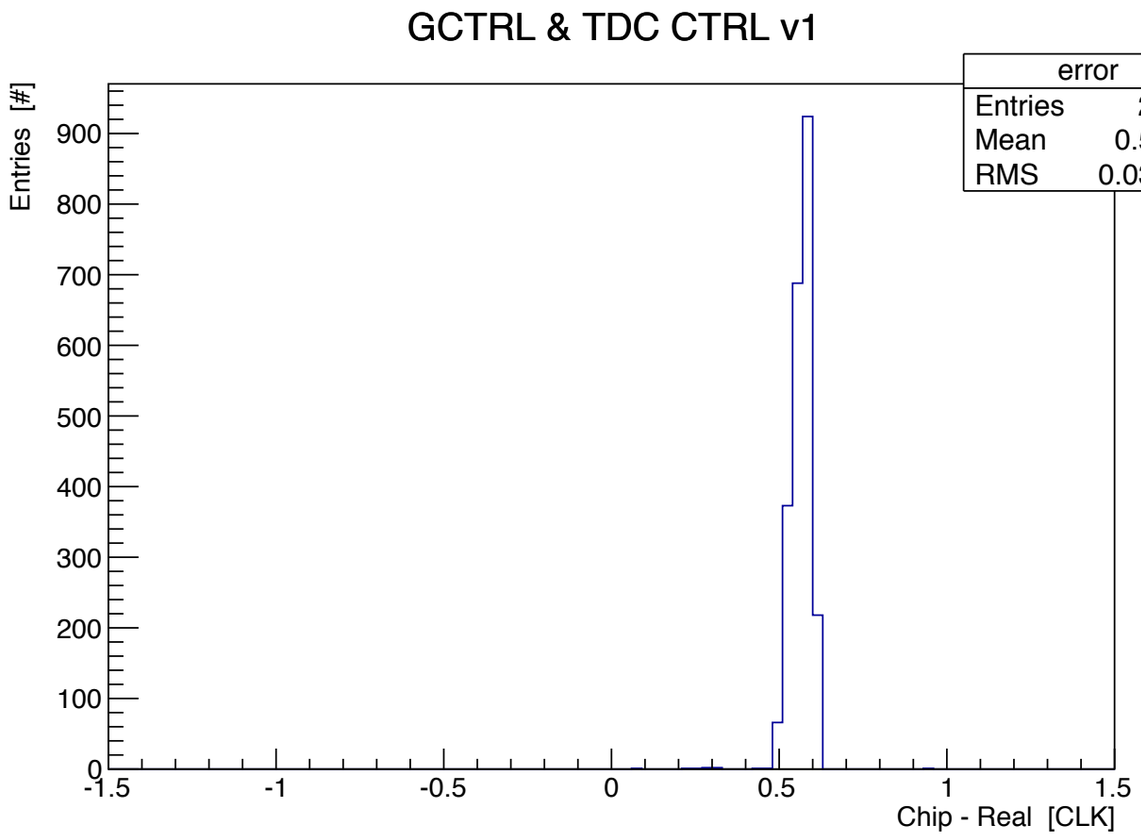

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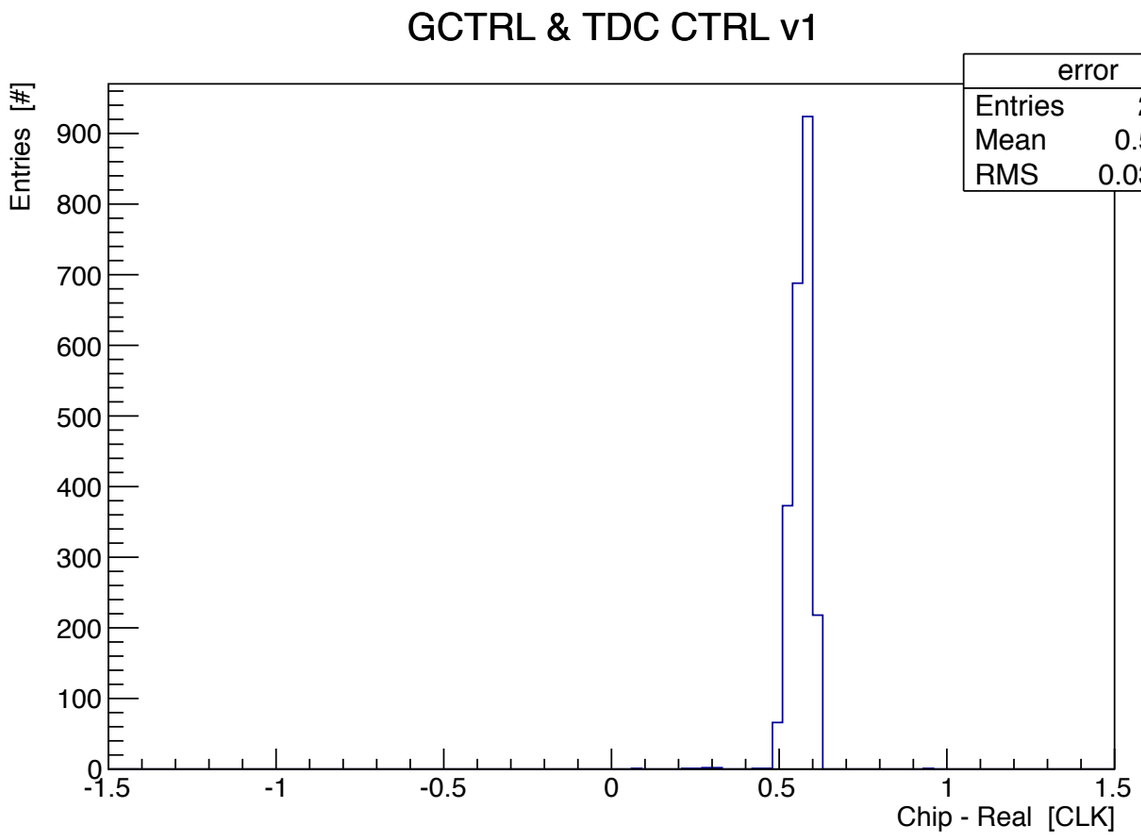

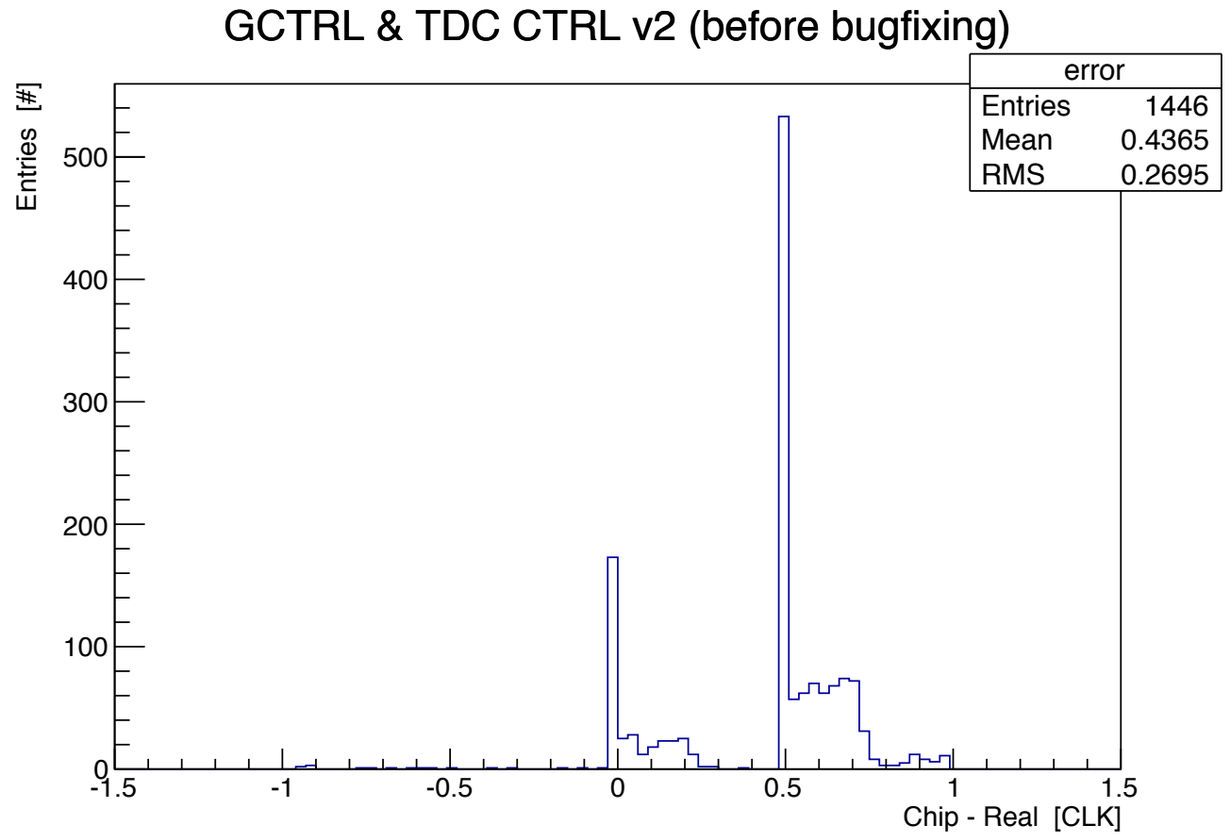

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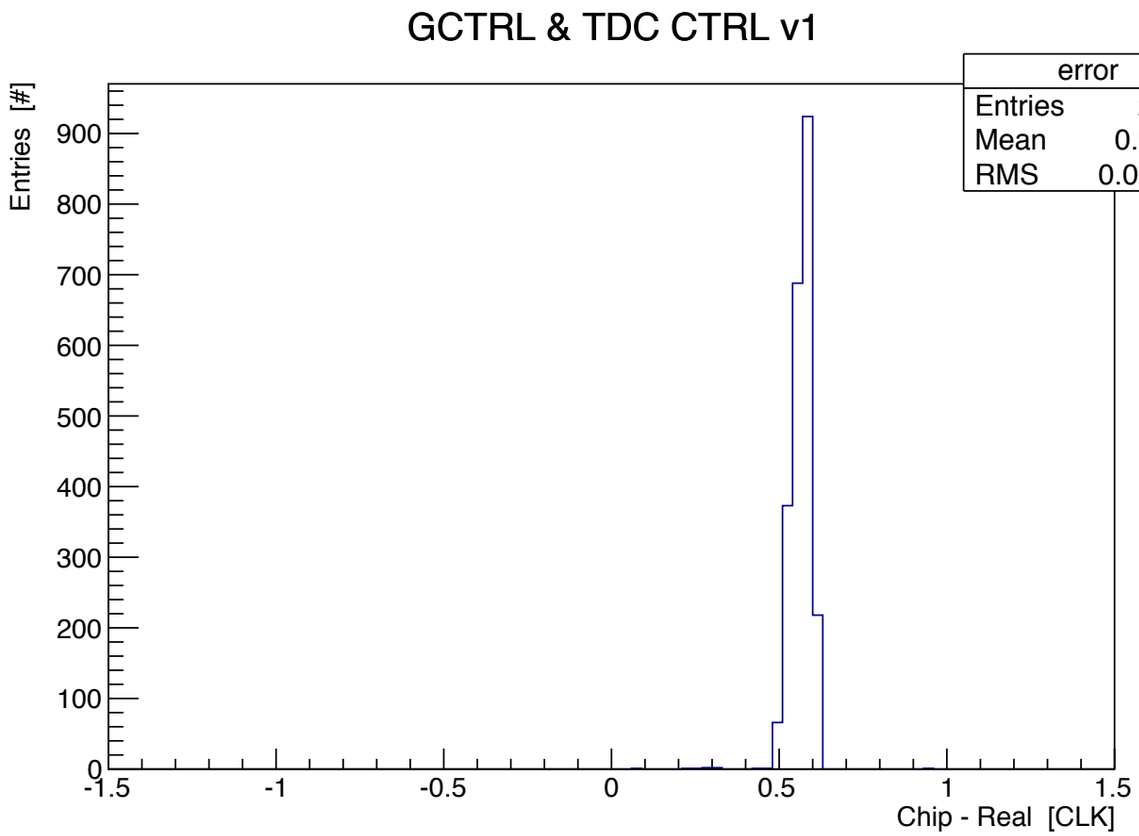

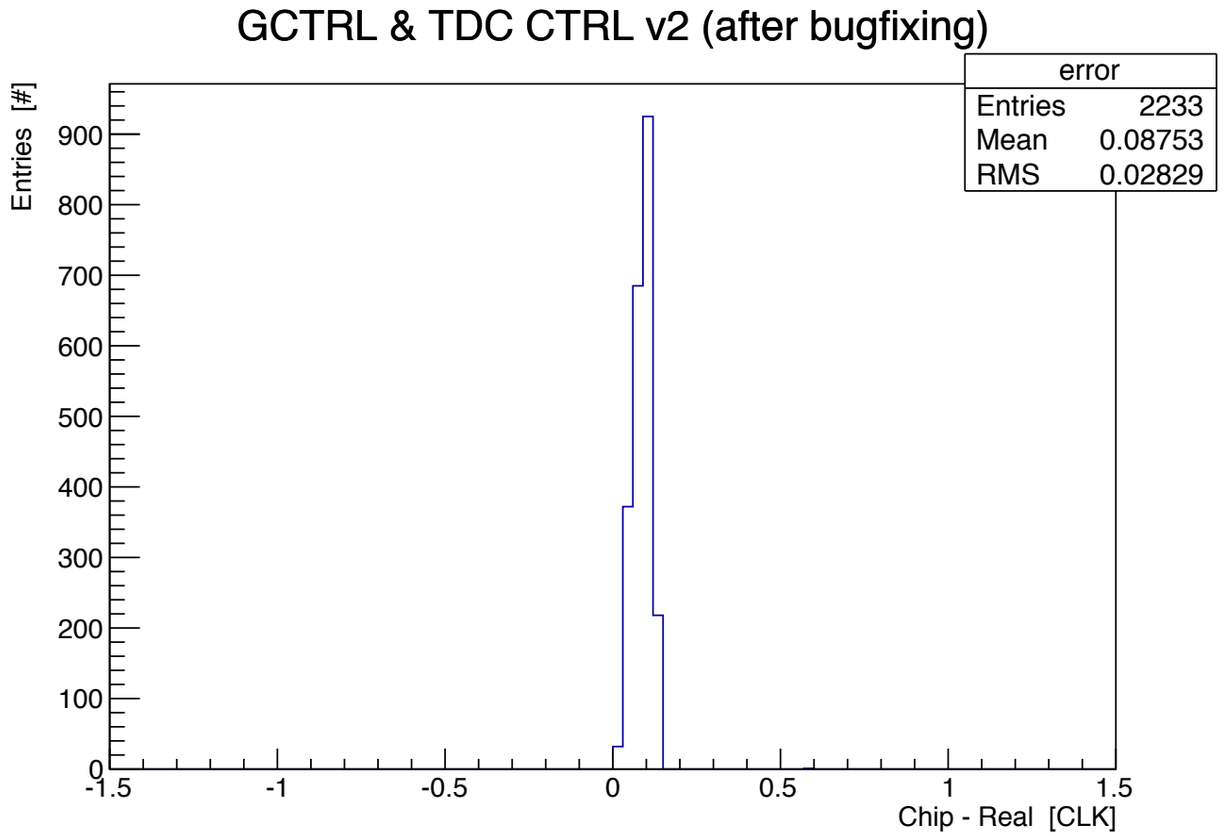

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	GCTRL v1 (tech. A)	GCTRL v1 (tech. B)
Occupancy (0.35 x 6.6 mm²)	70.5 %	38.1 %
Cells	44,949	45,695
Power (@ 160 MHz)	52.2 mW	61.3 mW

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	GCTRL v1 (tech. A)	GCTRL v1 (tech. B)	GCTRL v2 (current status, tech. B)
Occupancy (0.35 x 6.6 mm²)	70.5 %	38.1 %	34.5 %
Cells	44,949	45,695	57,703
Power (@ 160 MHz)	52.2 mW	61.3 mW	65.4 mW

Conclusion & Outlook

- First PASTA version in development
  - Time-based concept (store time stamps)
    - Based on TOFPET ASIC
    - Fast, simple, and low power consumption
  - New geometry due to placing constraints
  - Changed technology (A, 130 nm → B, 110 nm)
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Resources

- [**3**, MVD requirements] PANDA Collaboration; *PANDA Technical Design Report for the Micro Vertex Detector* (2013) [→ direct link]
- [**5**, TOFPET floorplan] M. D. Rolo, LIP Lisbon / INFN Torino (2013)