Updates on the PASTA Chip Front-End

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- Performance

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- Performance

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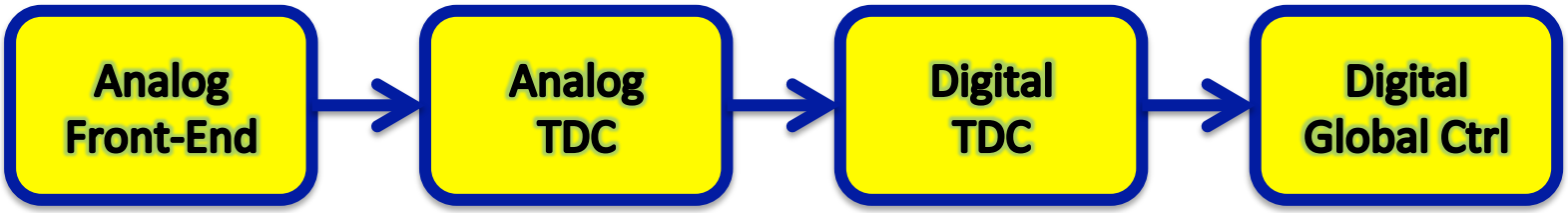
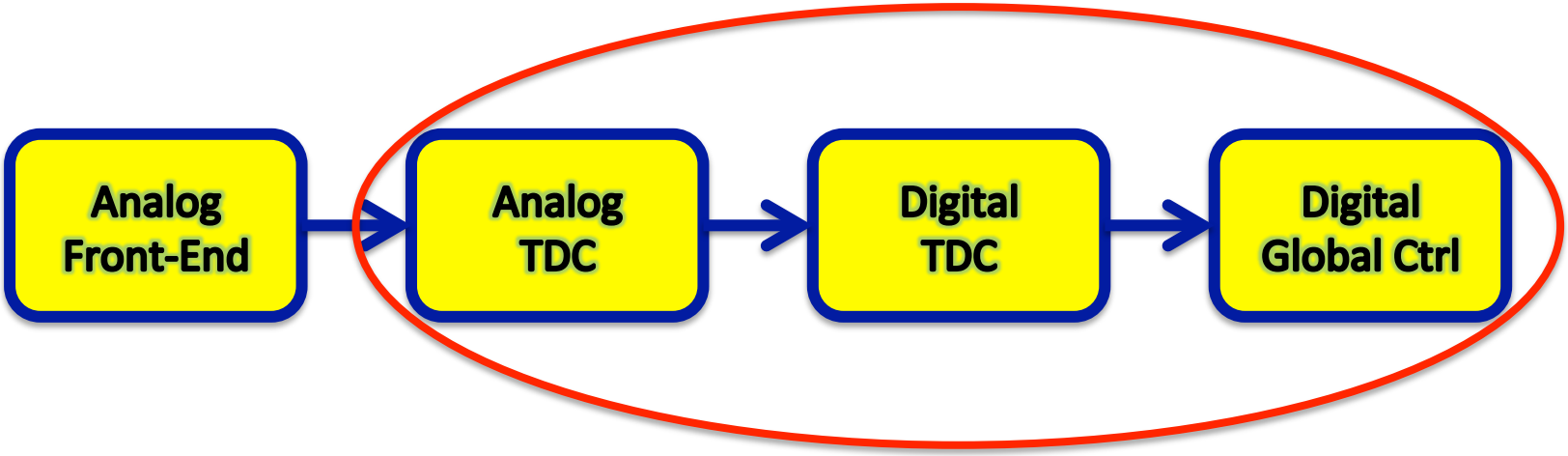
④ Conclusions and perspectives

PASTA Chip


Analog
Front-End
Analog
TDC
Digital
TDC
Digital
Global Ctrl

PASTA Chip

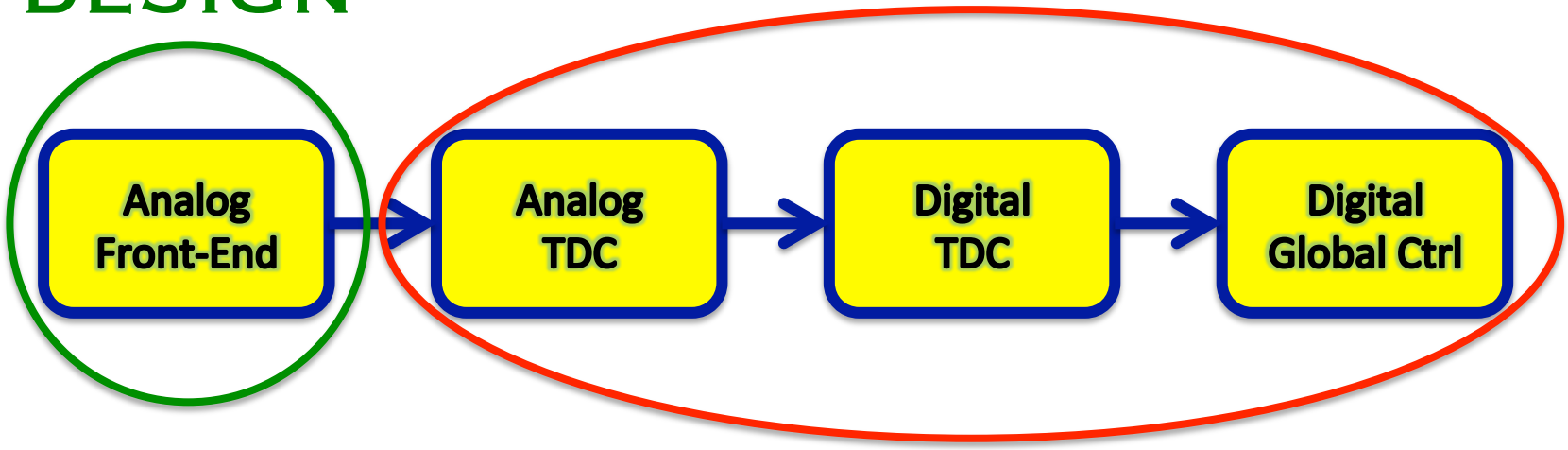


BASED ON TOFPET

PASTA Chip

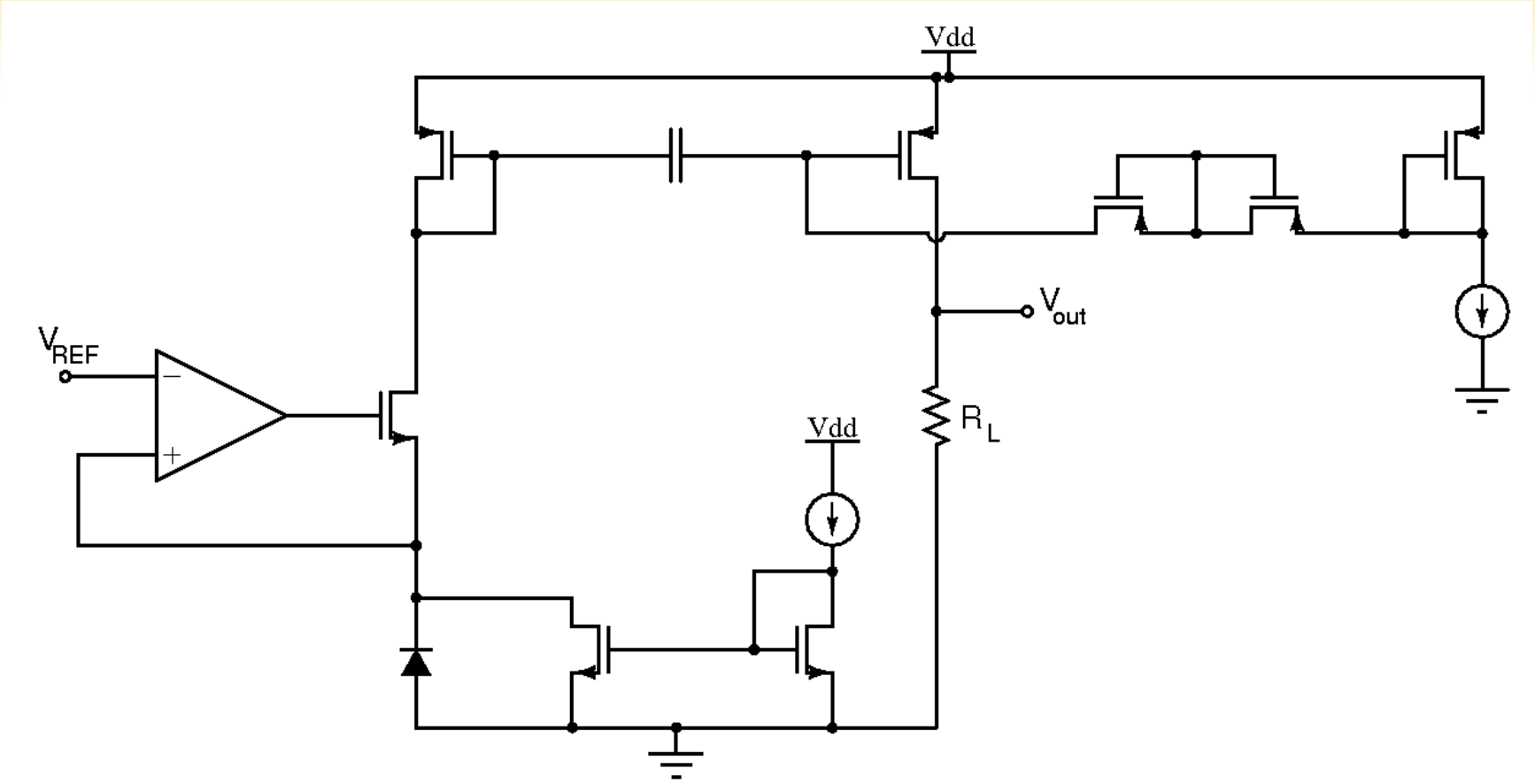
New

design

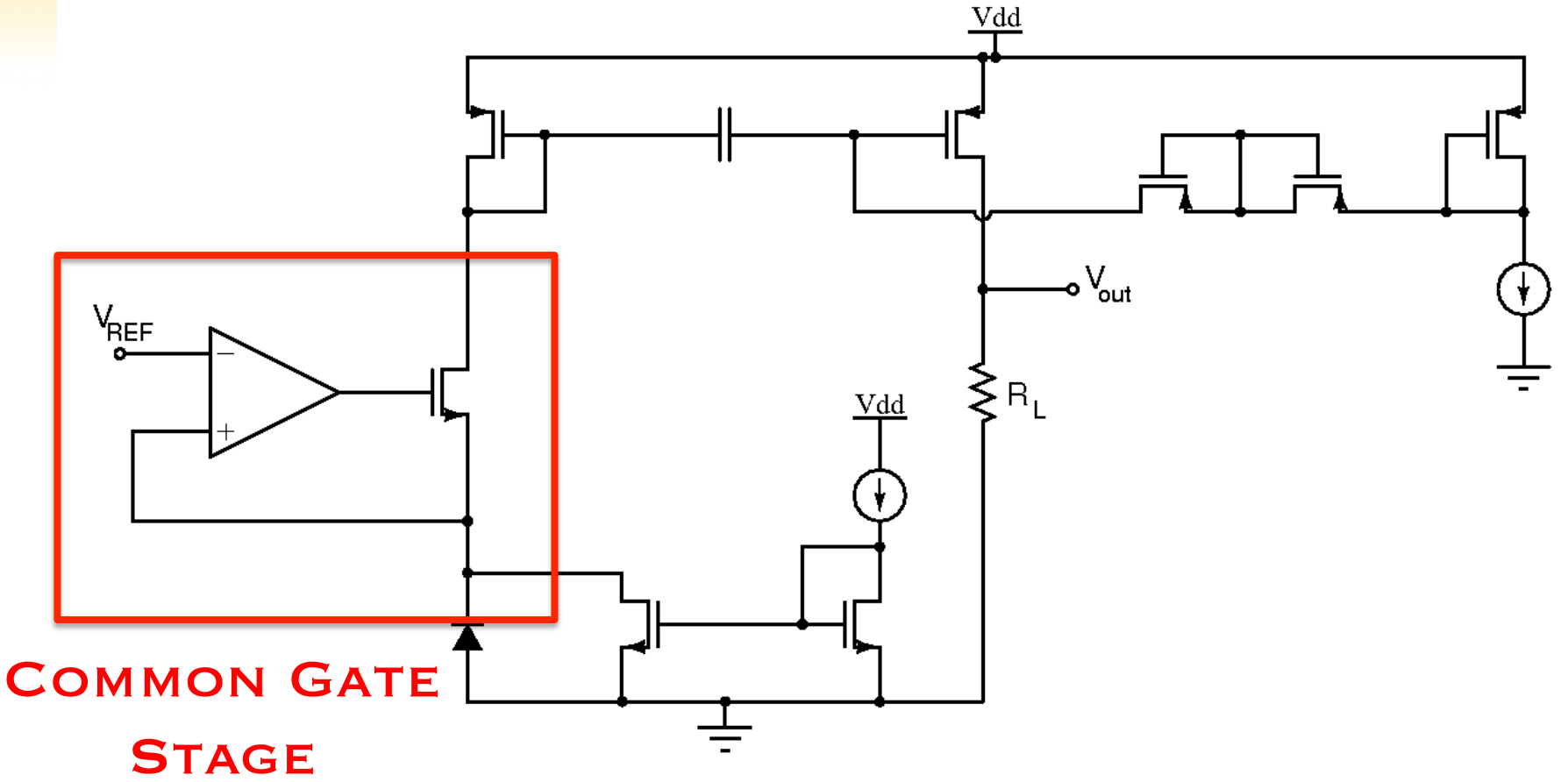


Based on TOFPET

TOFPET Front-End: Schematic

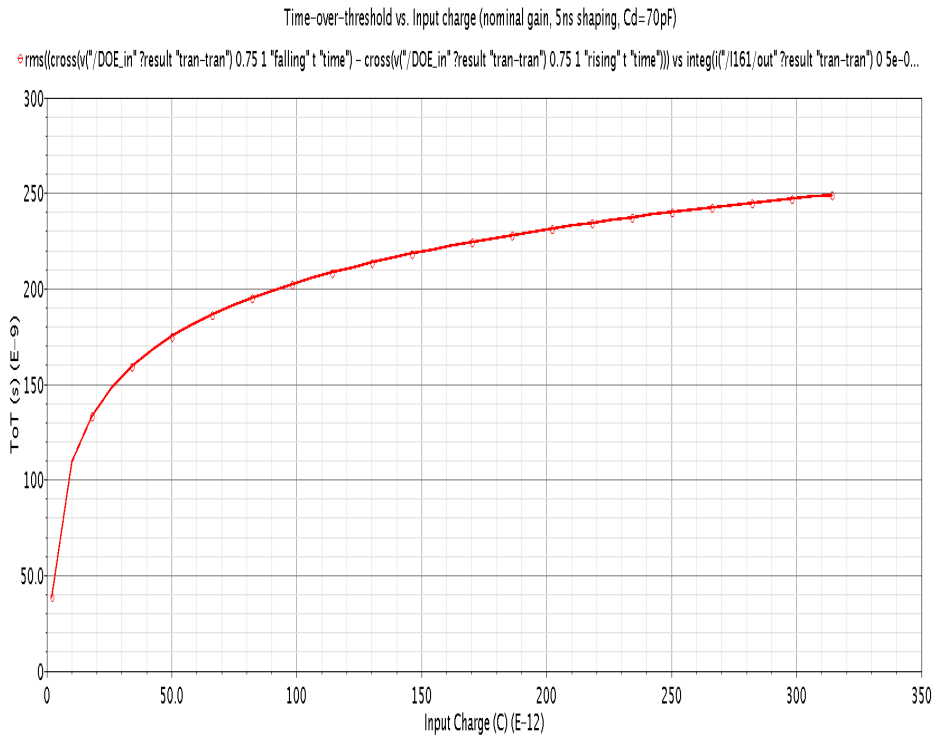


TOFPET Front-End: Schematic

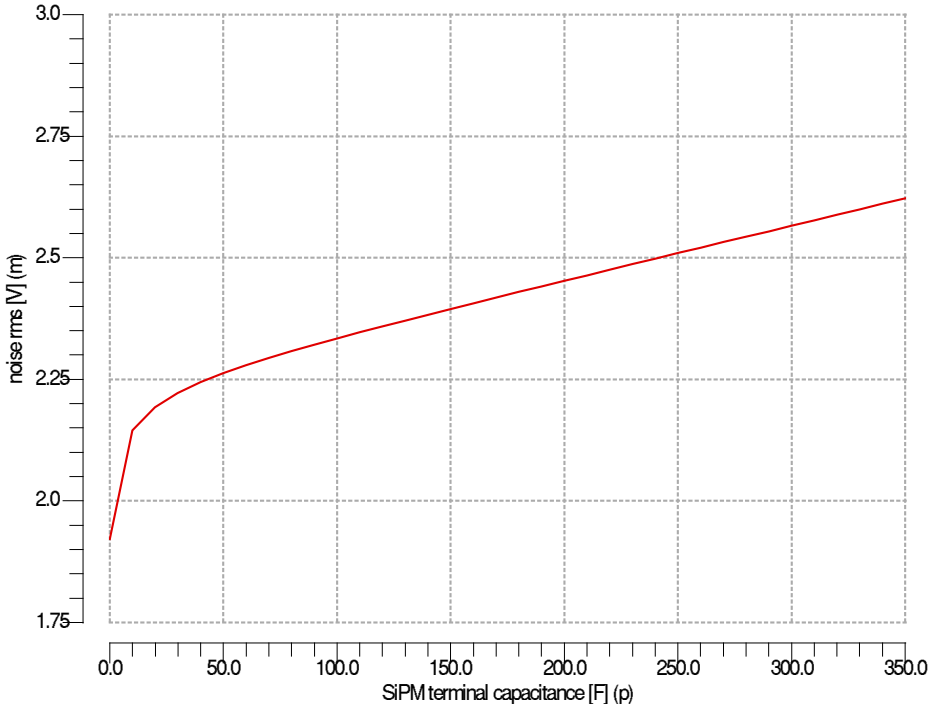


TOFPET Front-End: Performance

Linearity



Noise



Simulations by Manuel D. Rolo

TOFPET Front-End: Performance

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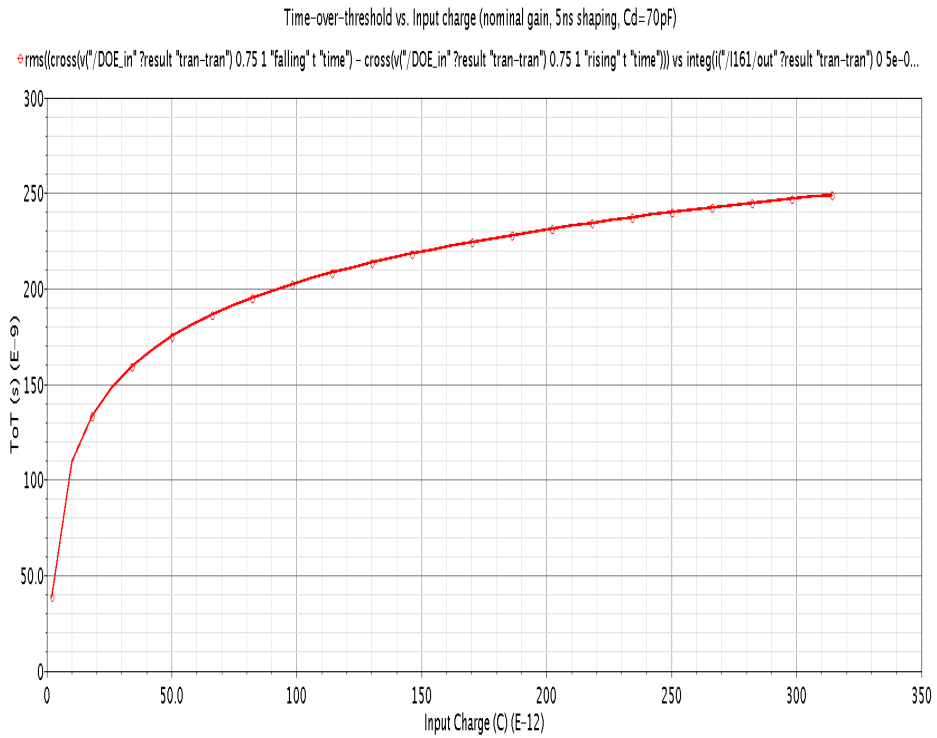

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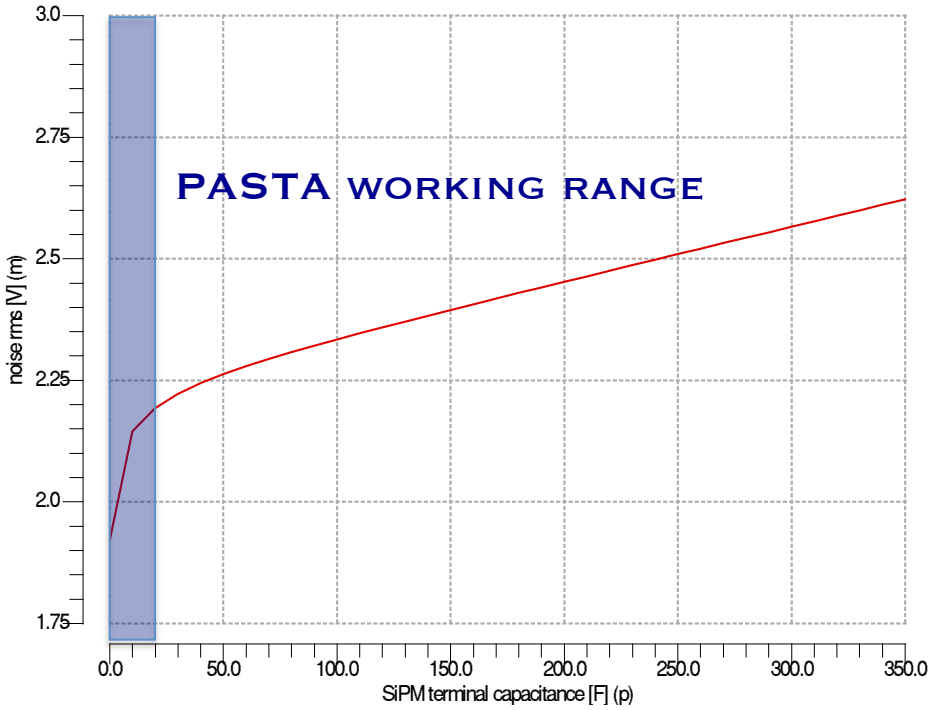
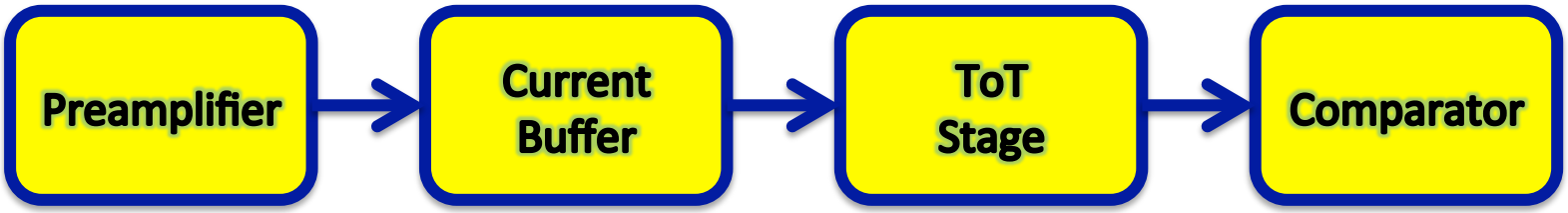


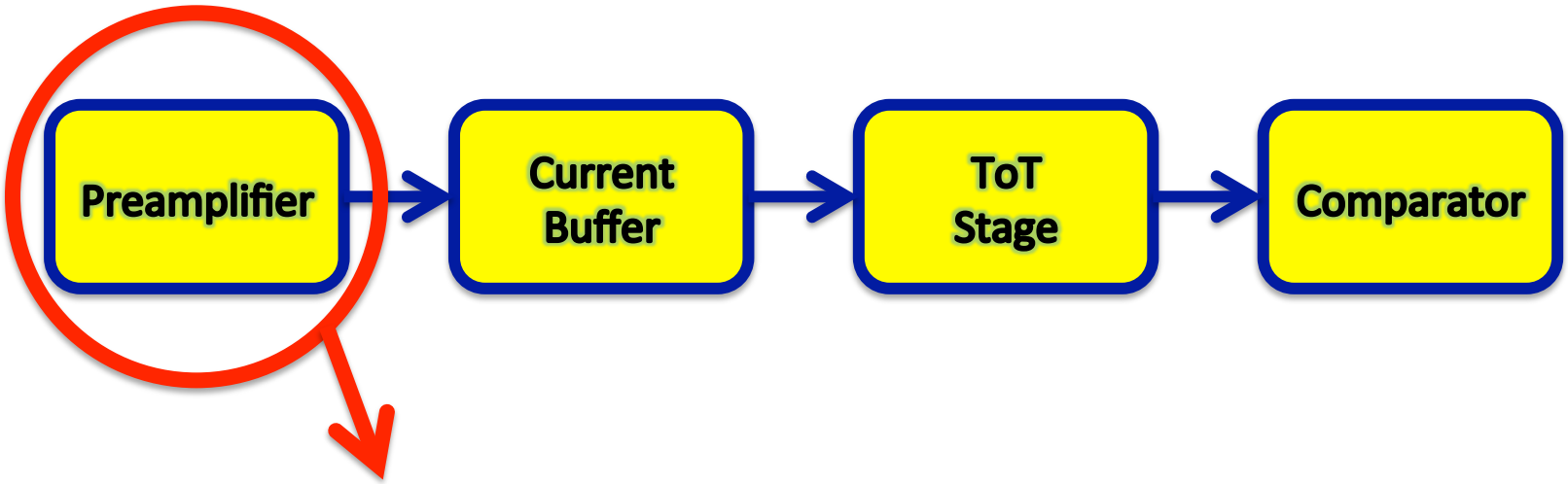
Simulations by Manuel D. Rolo

Back to September



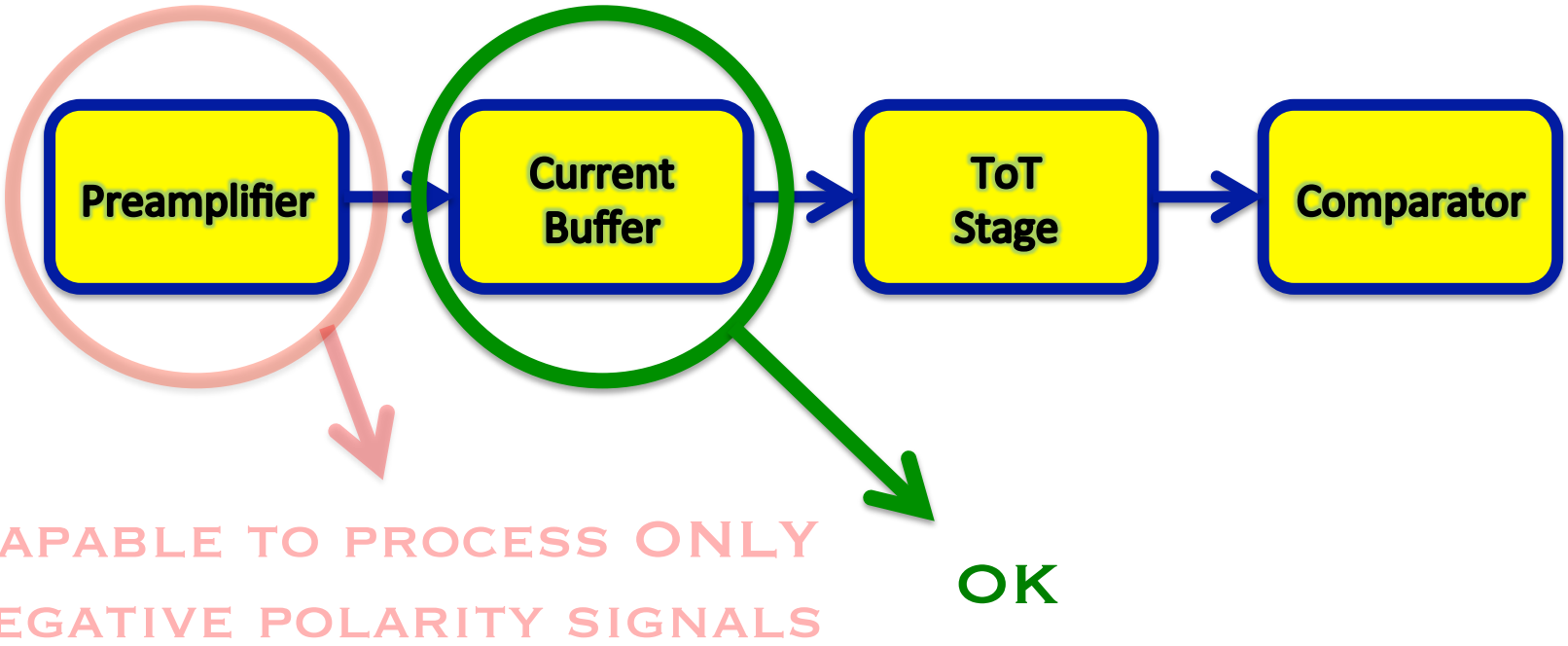
FRONT-END CHAIN

Back to September



CAPABLE TO PROCESS ONLY NEGATIVE POLARITY SIGNALS

Back to September



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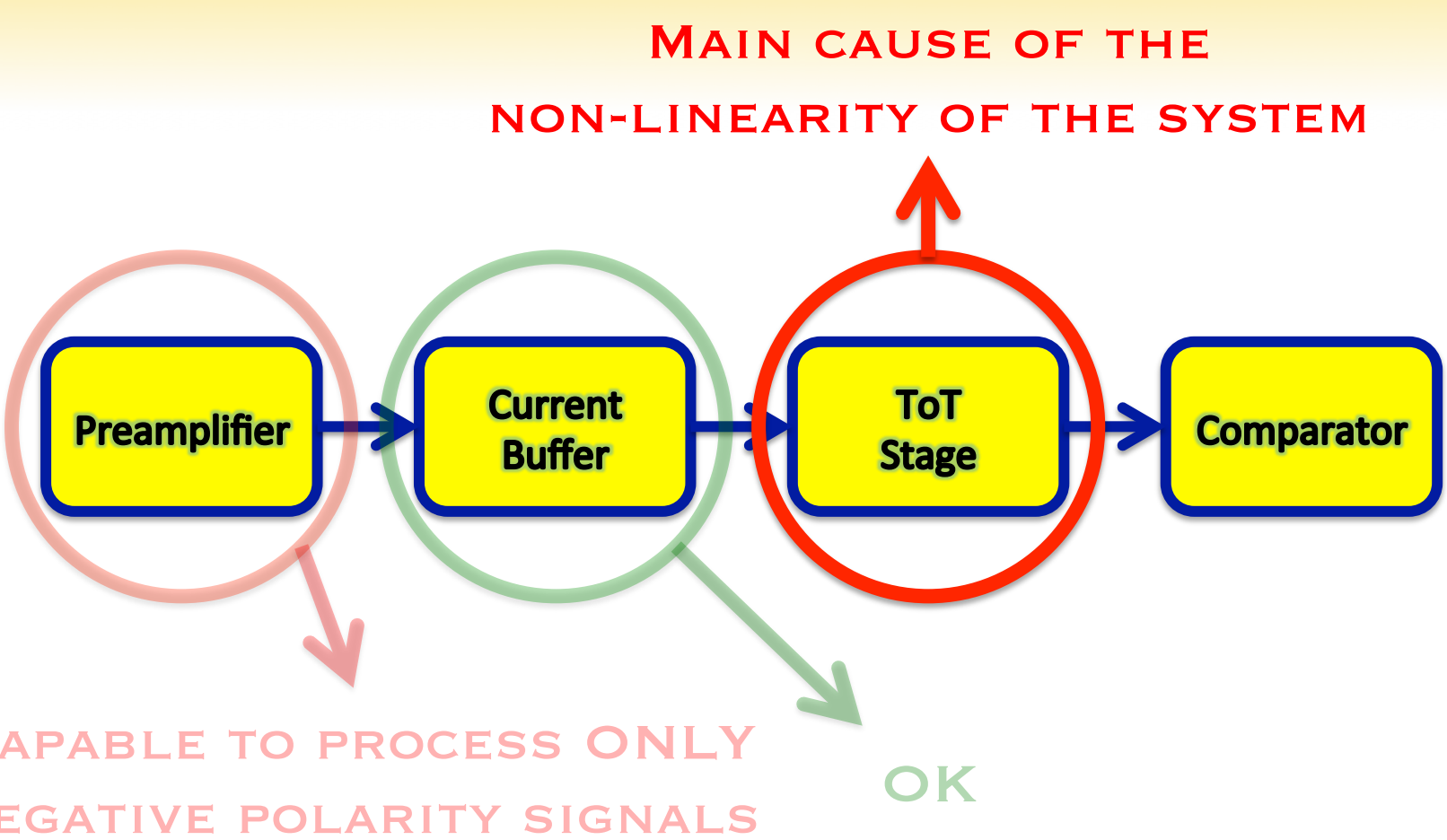

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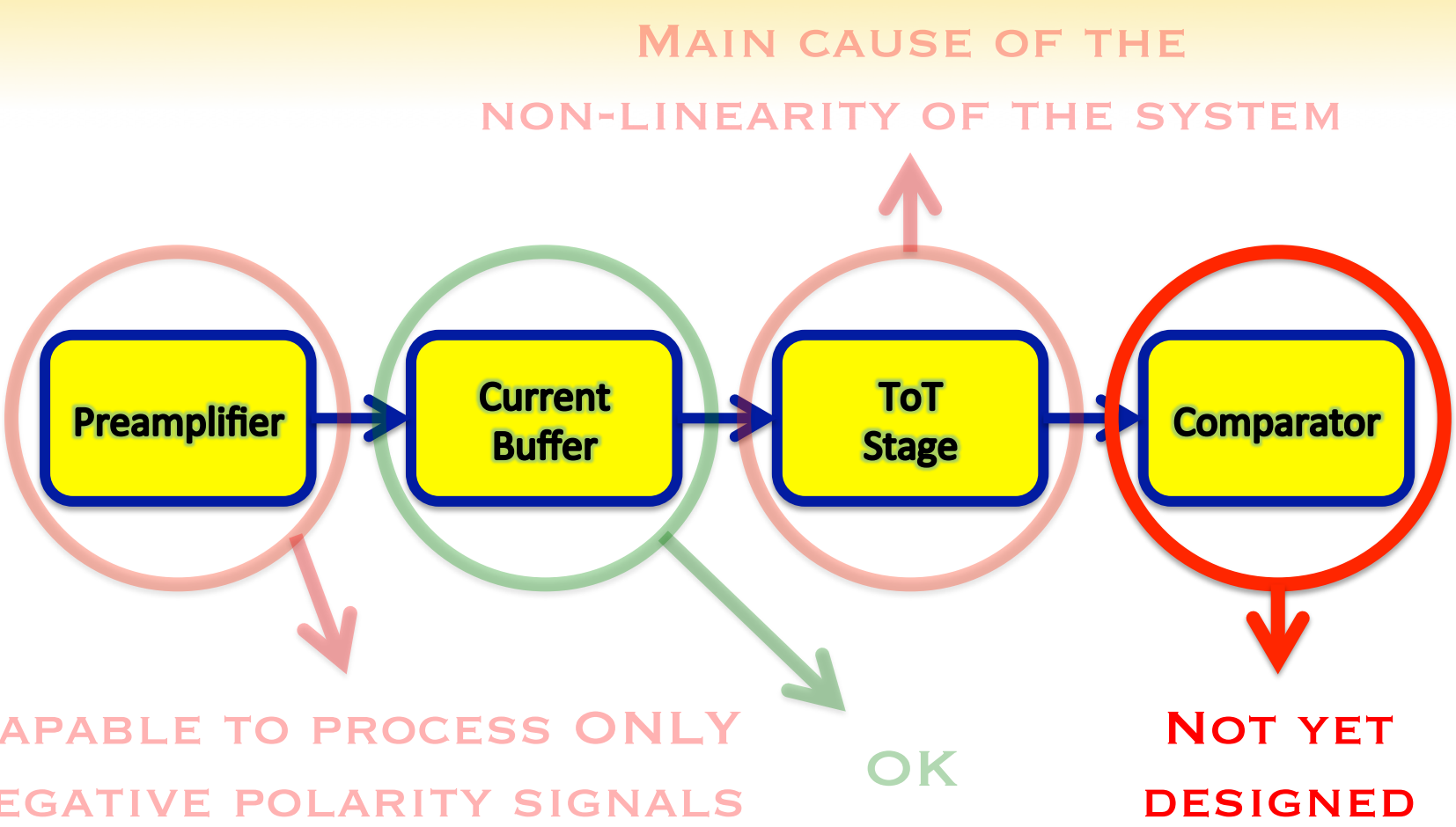
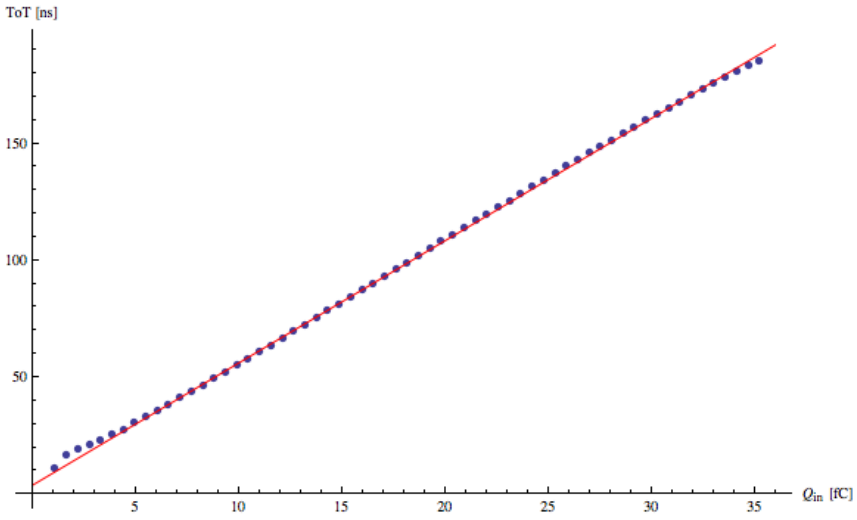
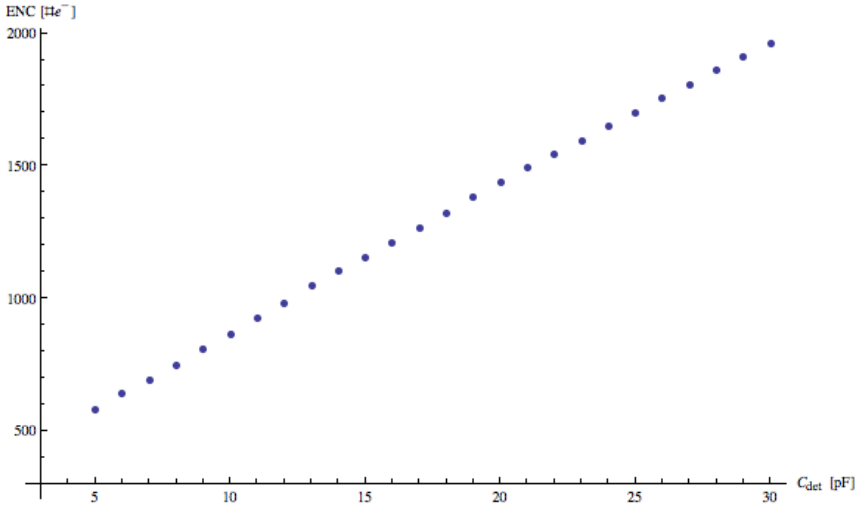


Old Chain Performance

Linearity



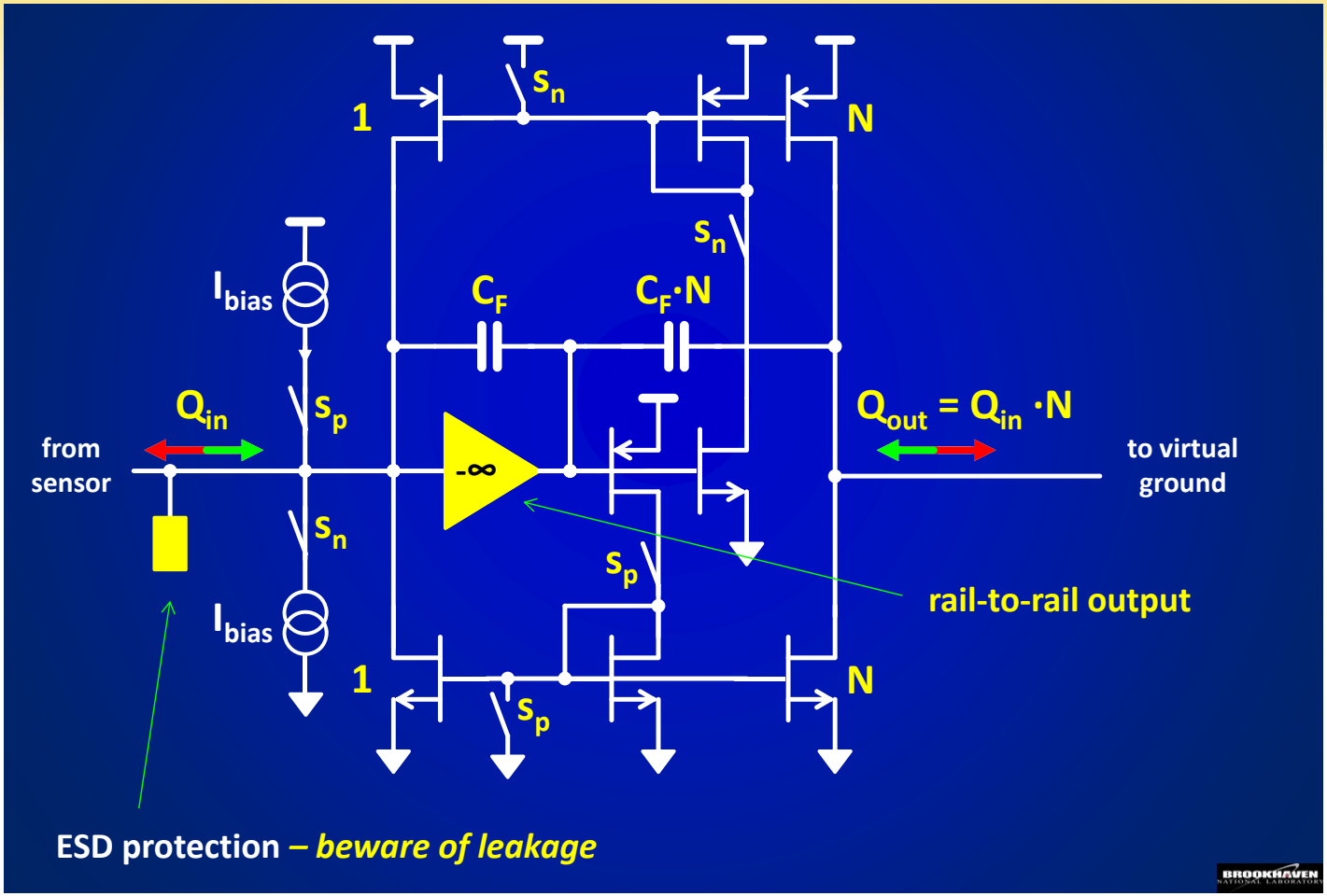
Noise



Updates

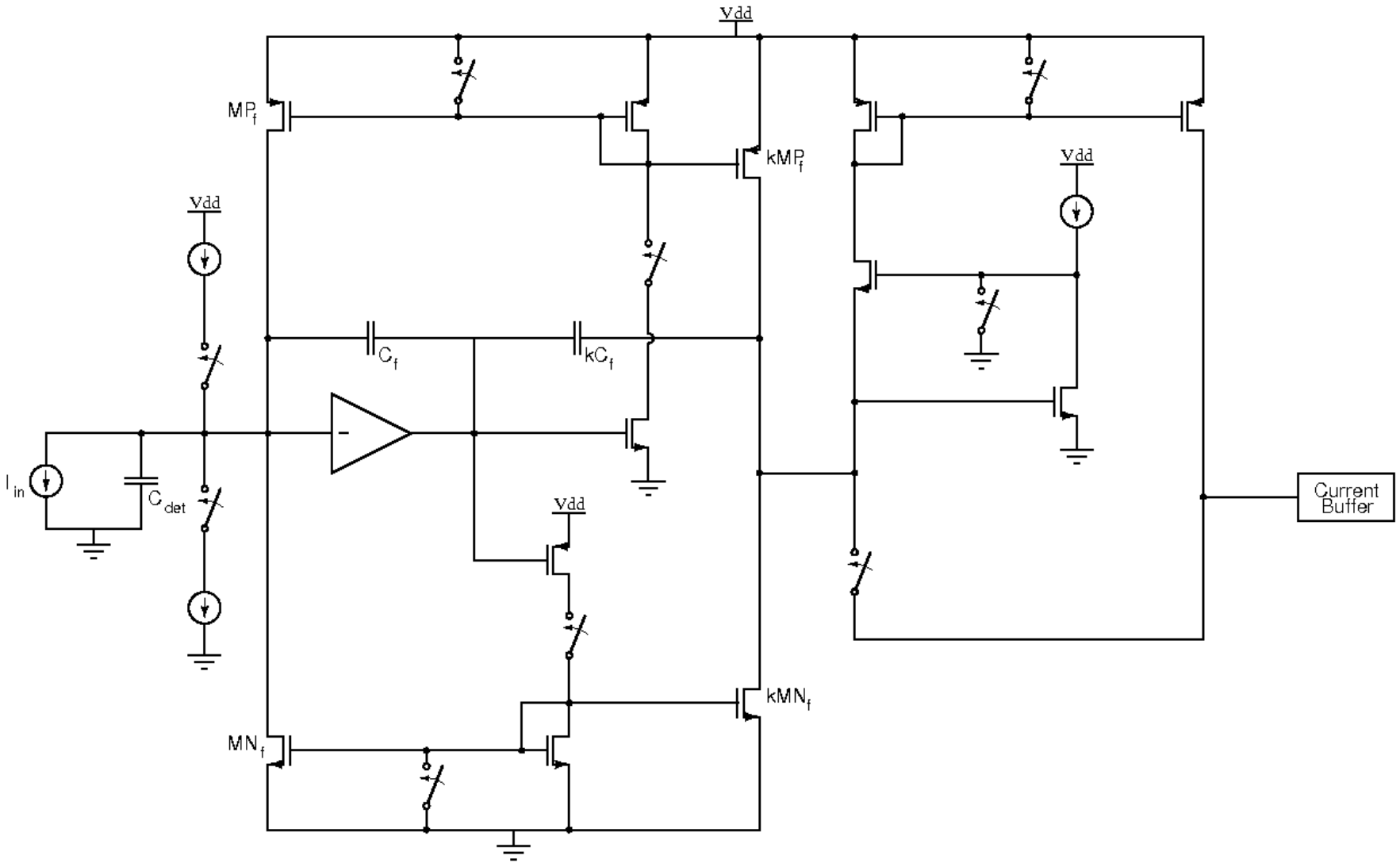
- Introduction of a dual-polarity capable architecture in the first stage *(based on the design made by the BNL group for ATLAS Muon Spectrometer Upgrade)*
- First attempts to optimize the ToT Stage in order to reduce the non-linearity observed for low charges
- Design of an hysteresis comparator in order to be less sensitive to the noise

BNL Architecture

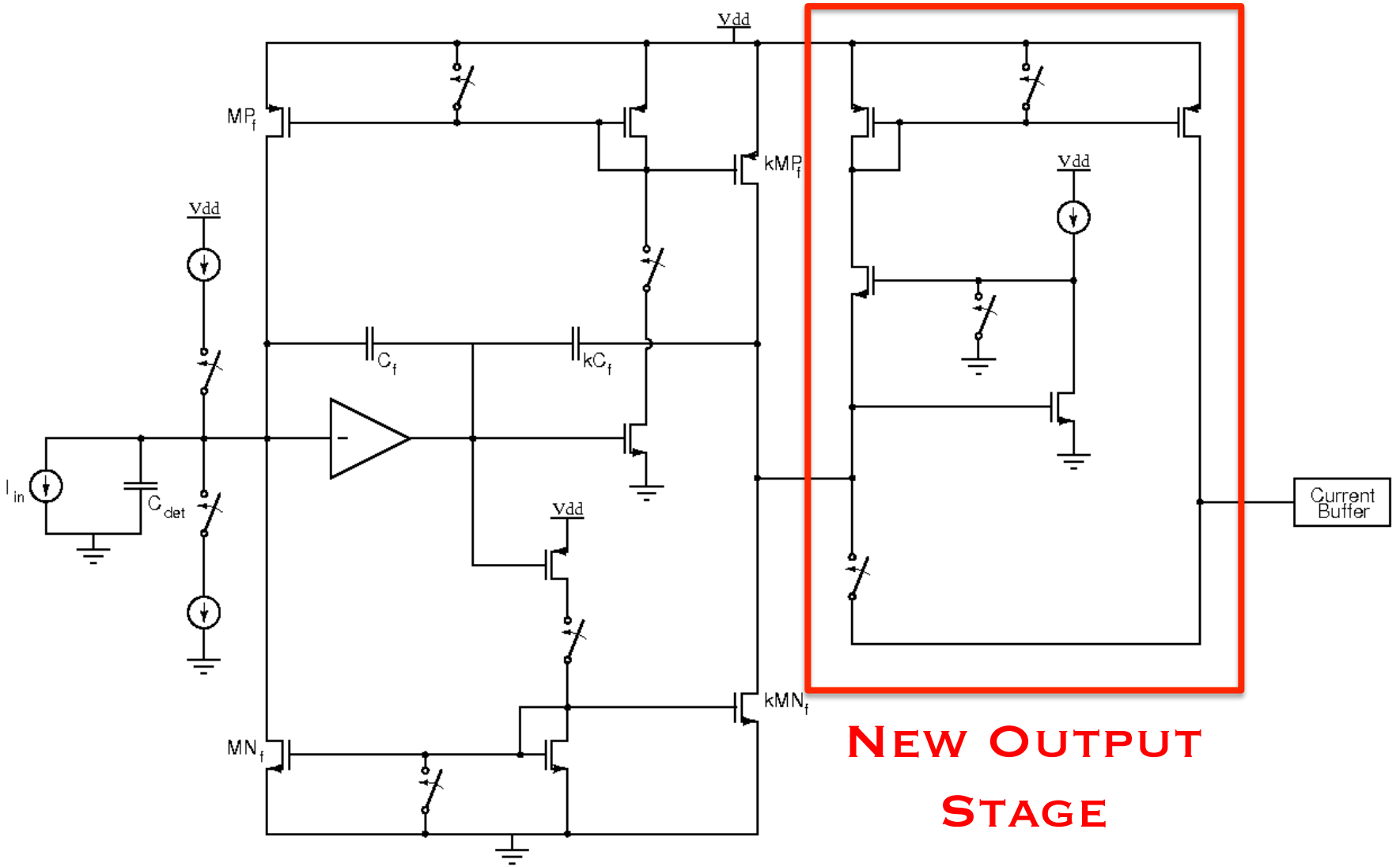


Slide from "VMM – a self-triggered front-end ASIC for ATLAS upgrades" by G. De Geronimo

PASTA Preamplifier Stage

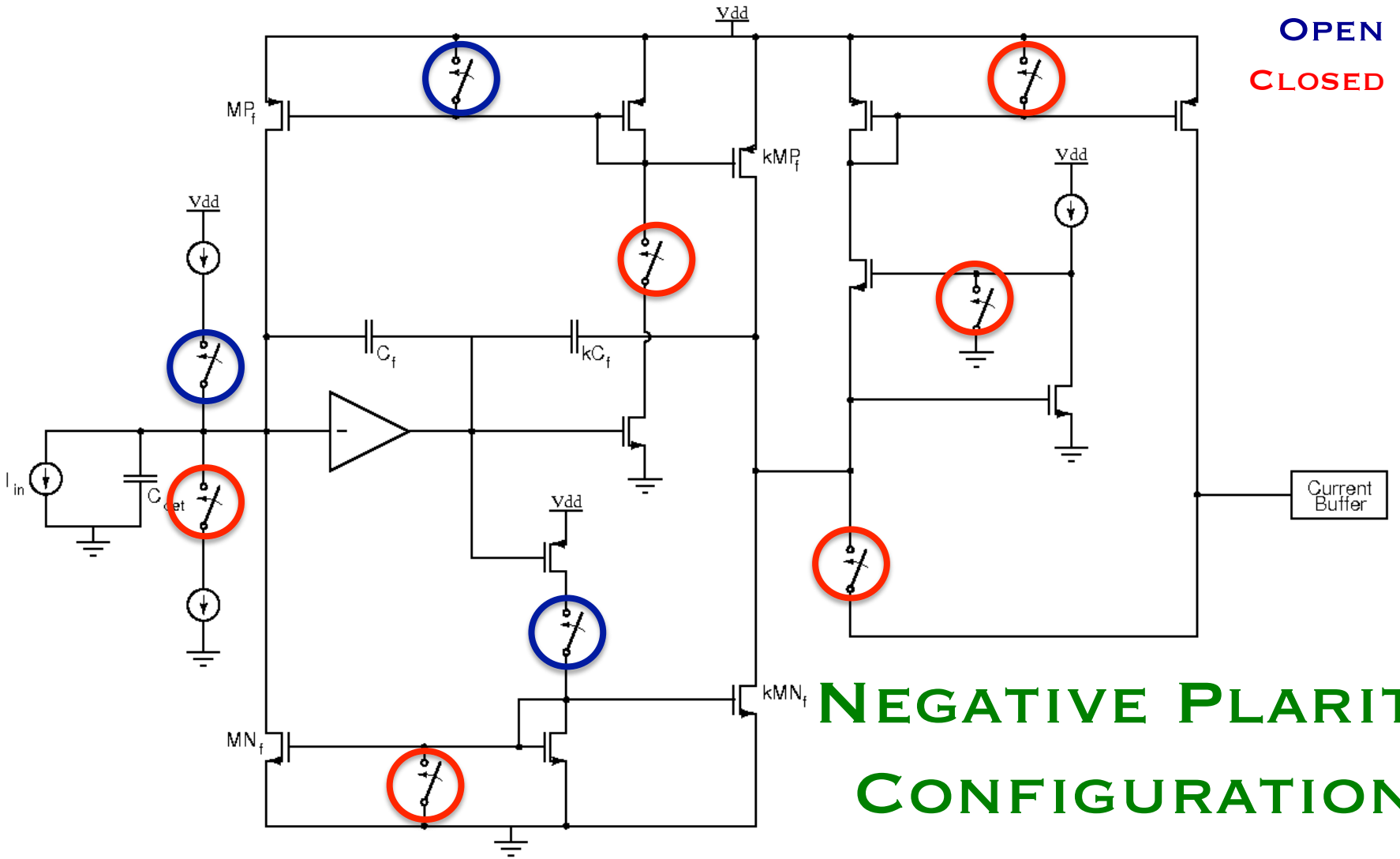


PASTA Preamplifier Stage



New Output Stage

PASTA Preamplifier Stage

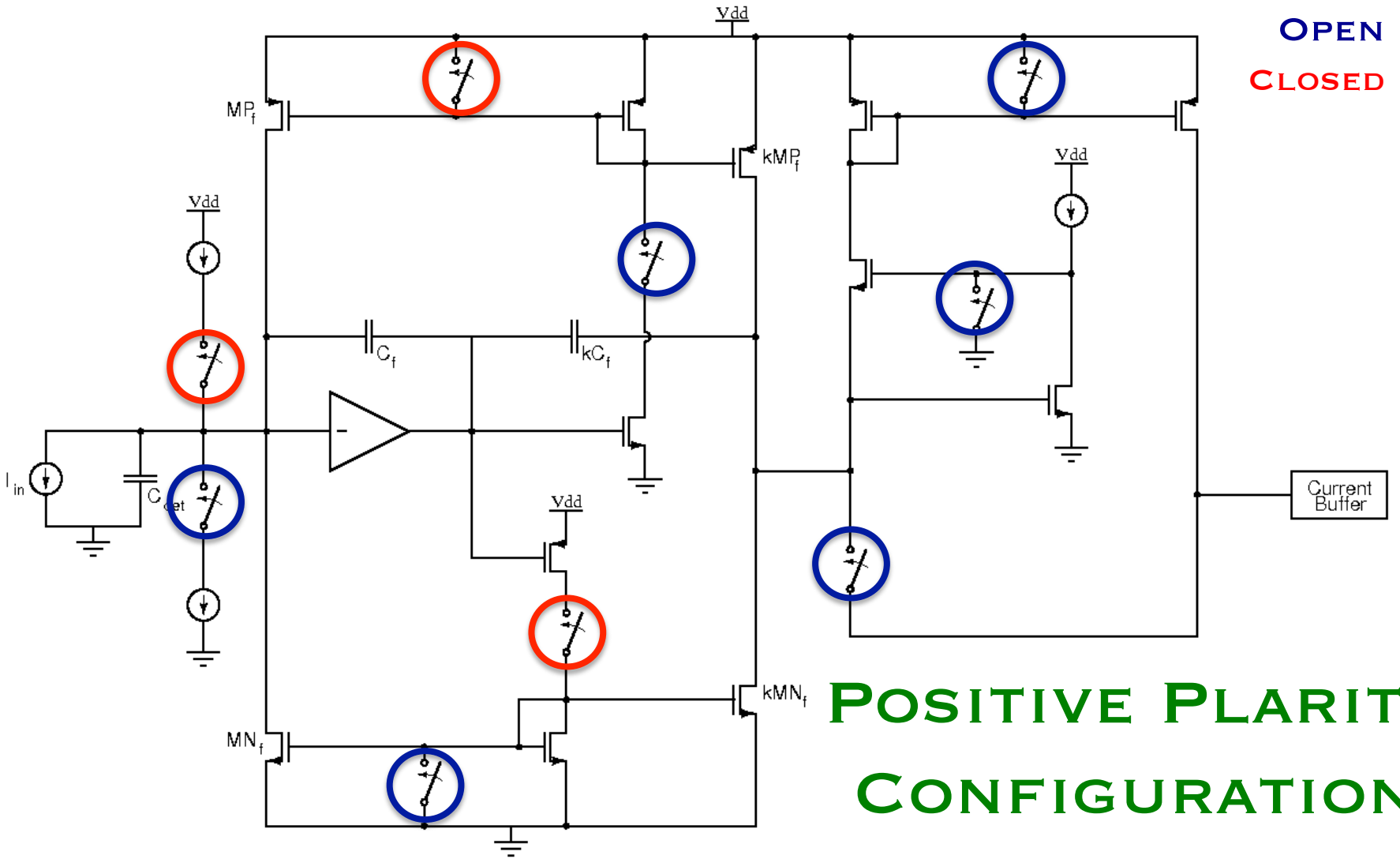


OPEN

CLOSED

NEGATIVE PLARITY CONFIGURATION

PASTA Preamplifier Stage



OPEN

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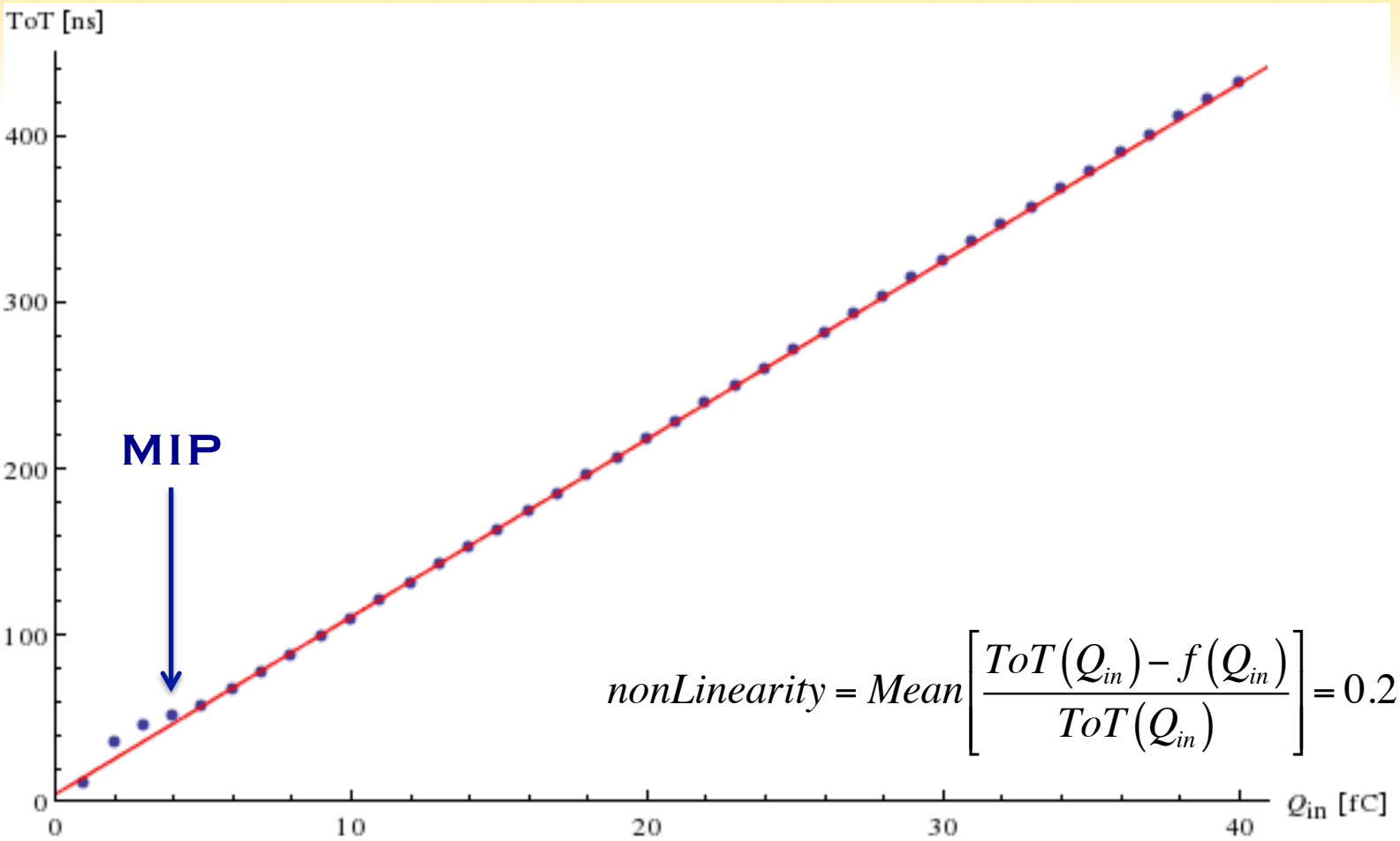
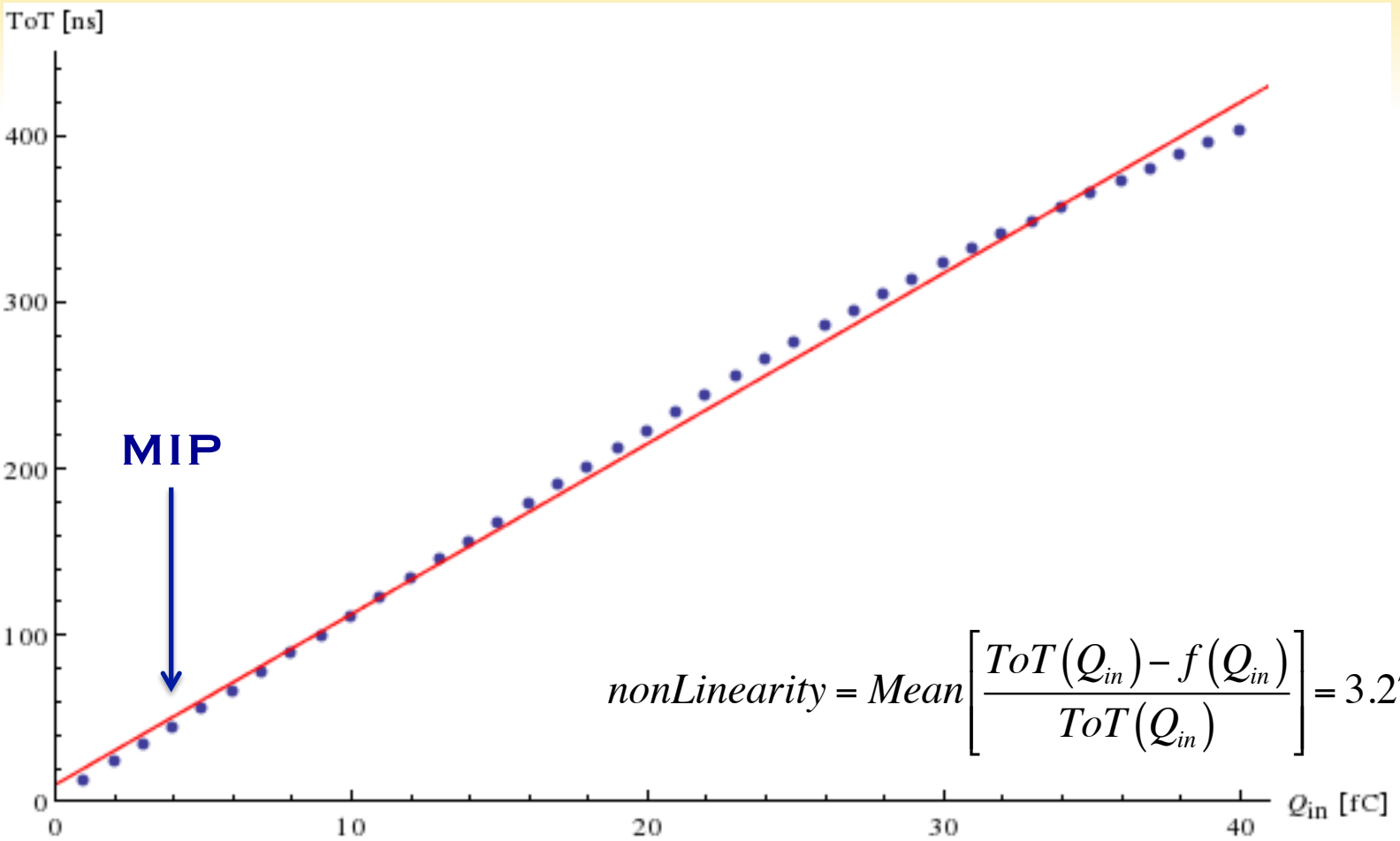
POSITIVE PLARITY CONFIGURATION

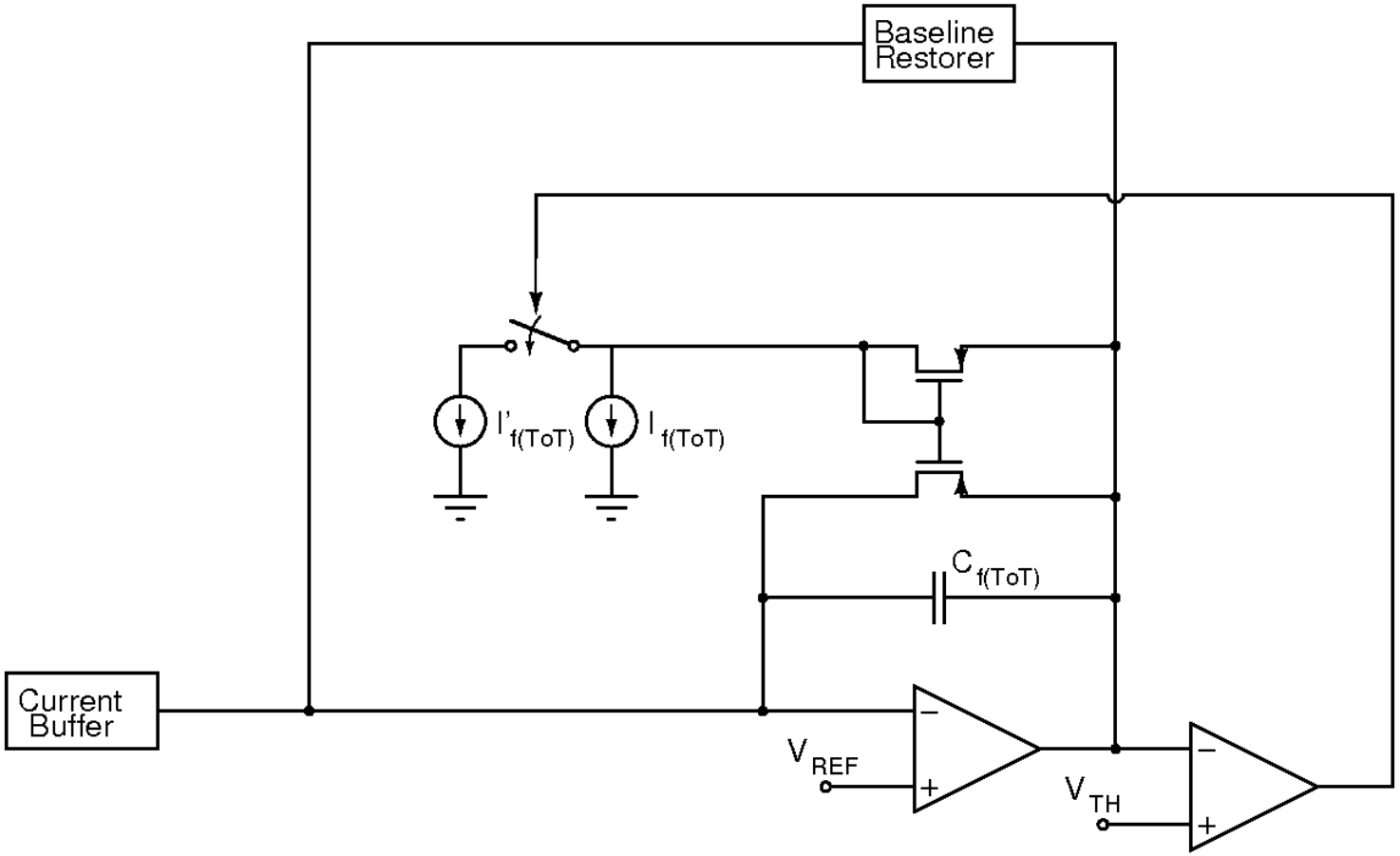
Negative Polarity Input: Linearity



Positive Polarity Input: Linearity



“Dynamic” ToT Stage



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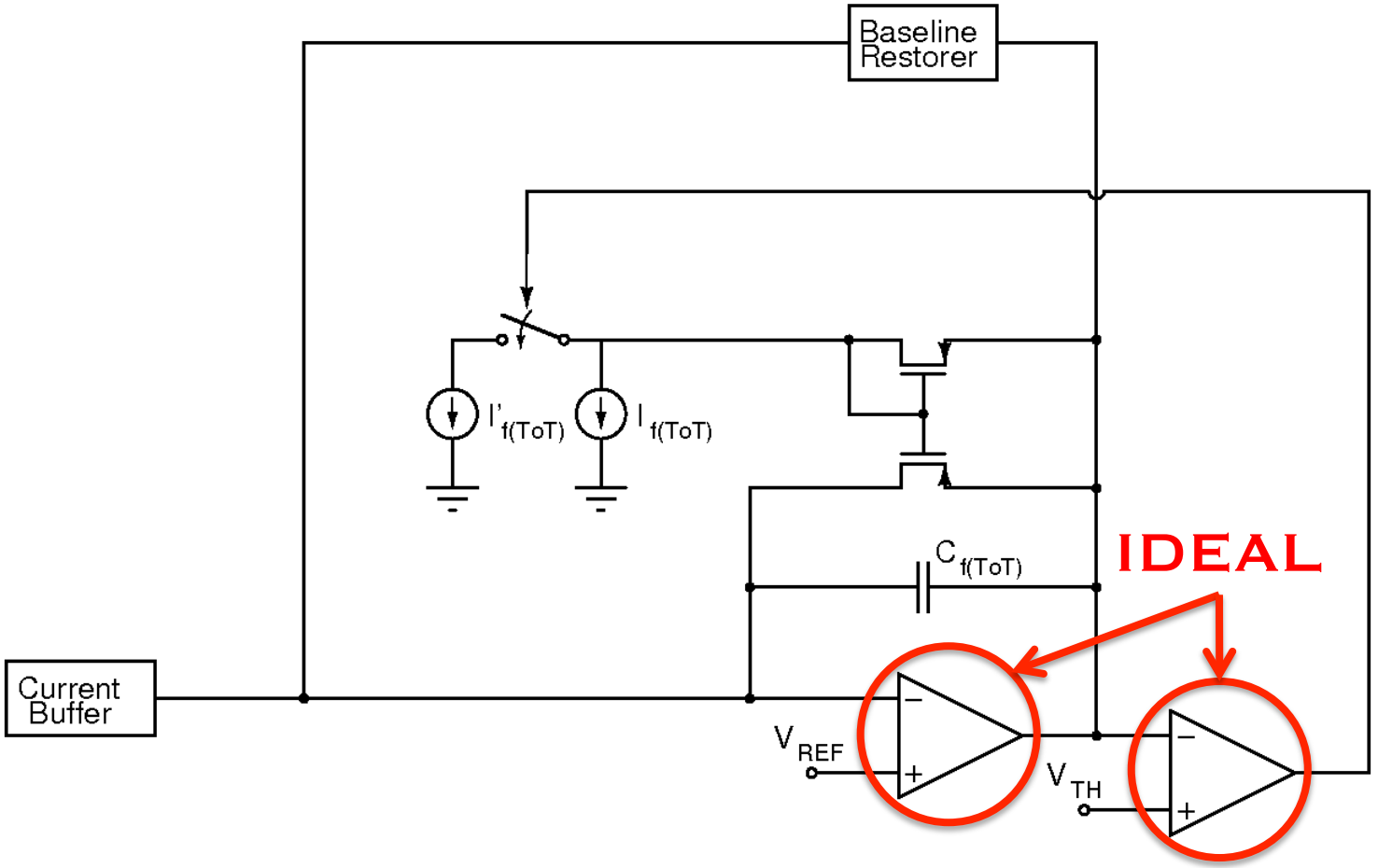
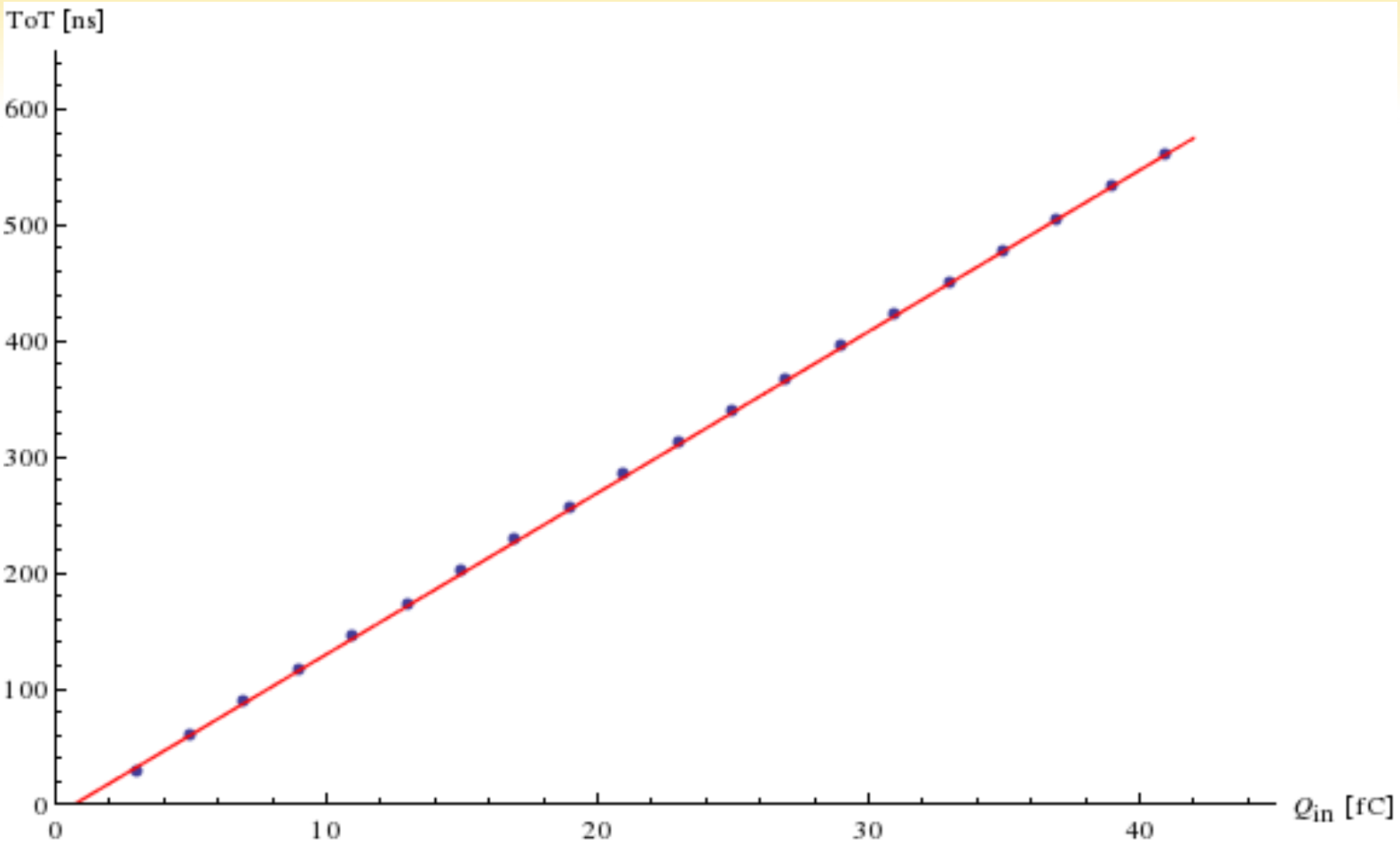


Negative Polarity Input



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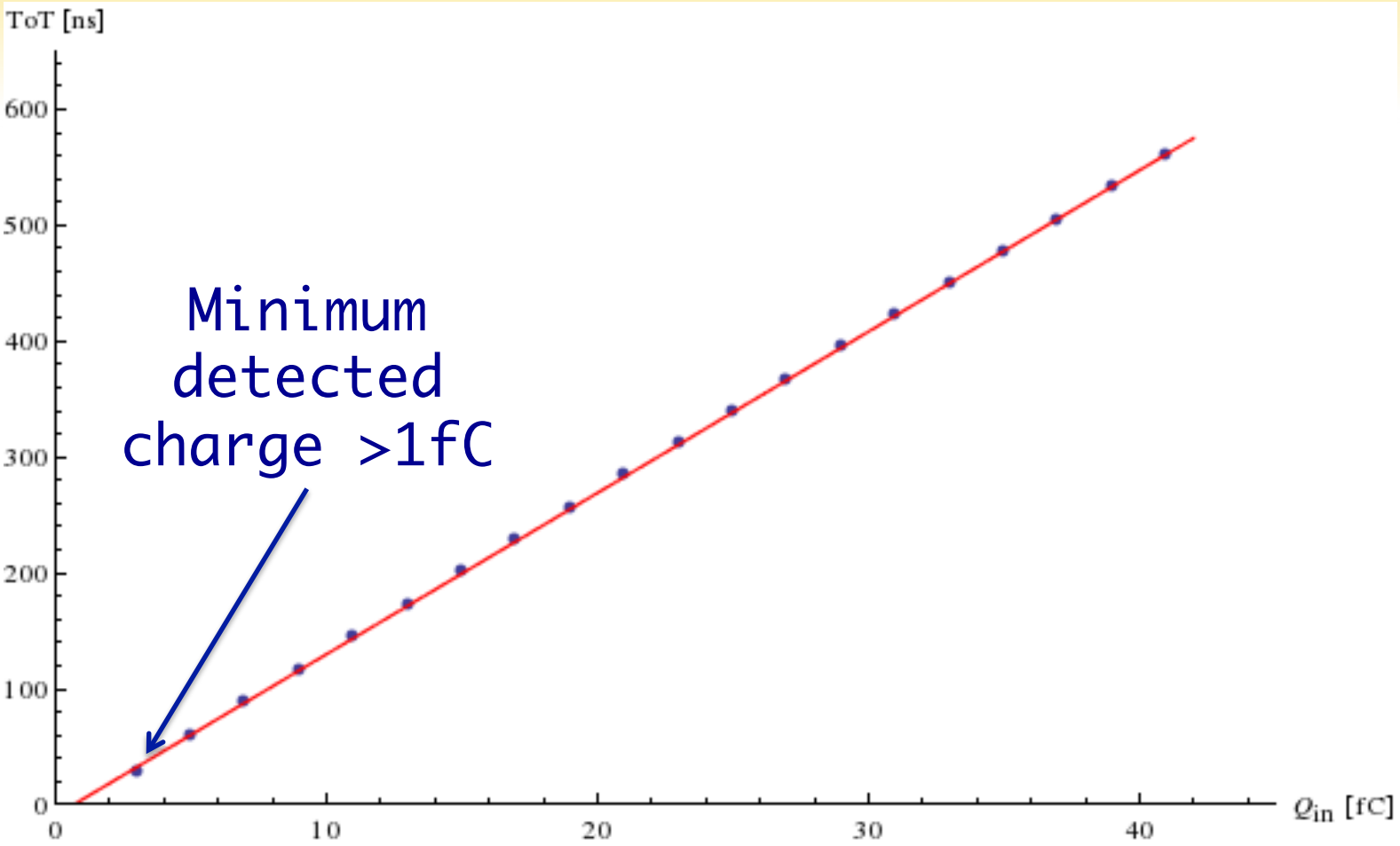

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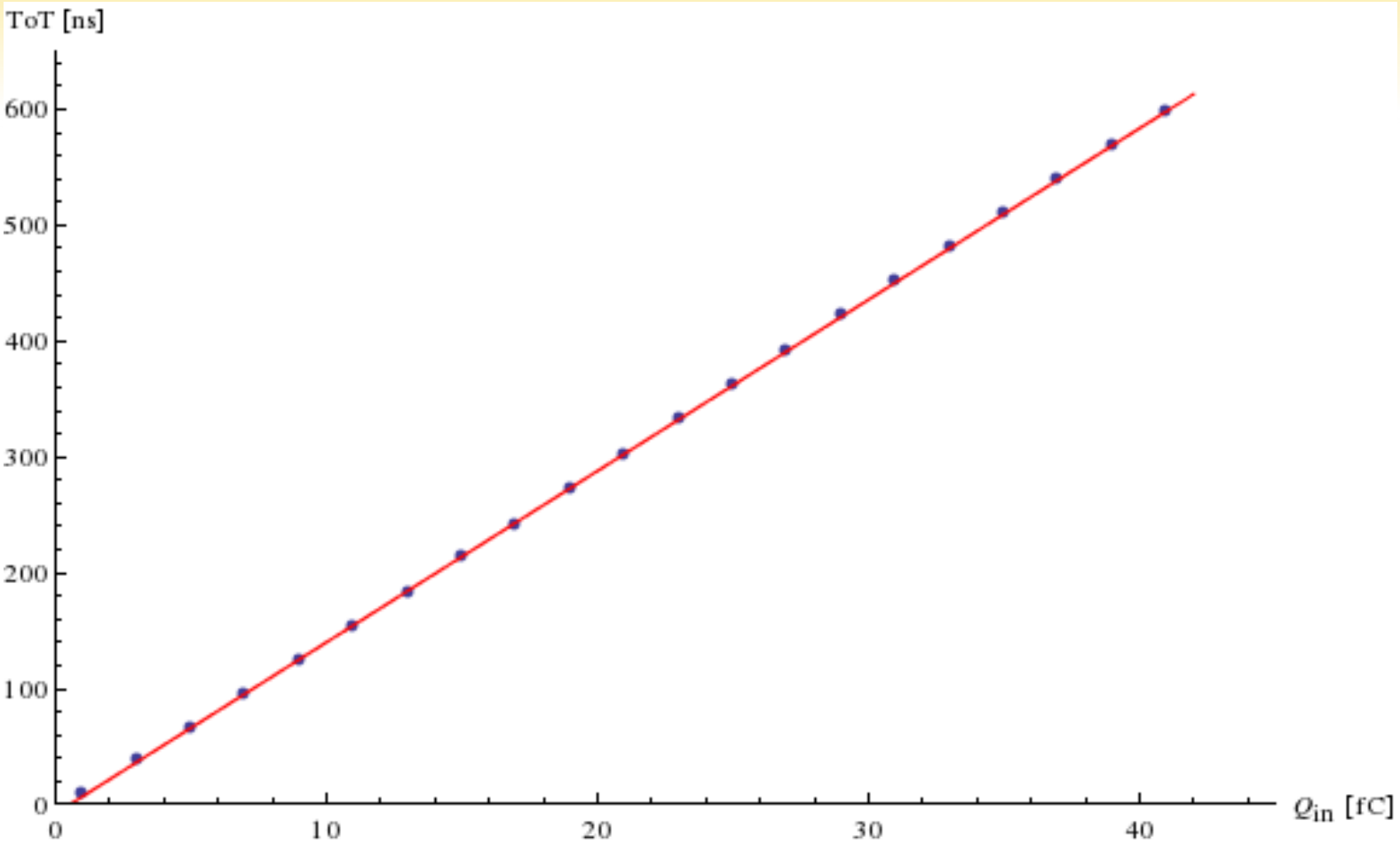

Details about the Threshold

- Considering a minimum event rate per channel equal to 1kHz, the threshold to have a noise frequency of 1% is:

$$V_{TH} = \sqrt{-2\ln(4\sqrt{3}\cdot t_{peak}\cdot f_n)}\cdot V_{n,rms}$$

Rice, S.O. (1944). "Mathematical Analysis of Random Noise"

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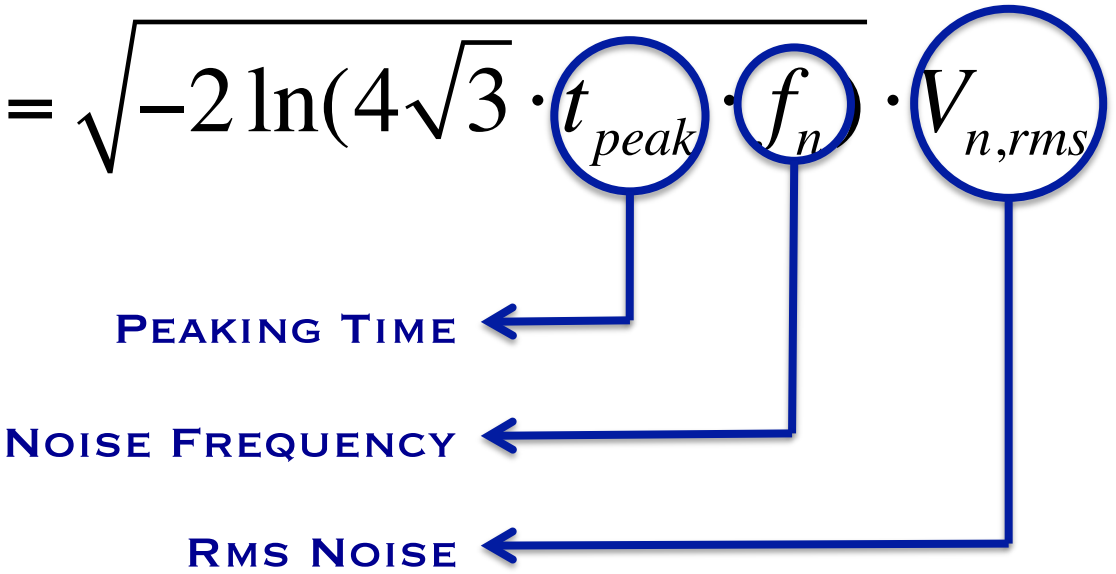

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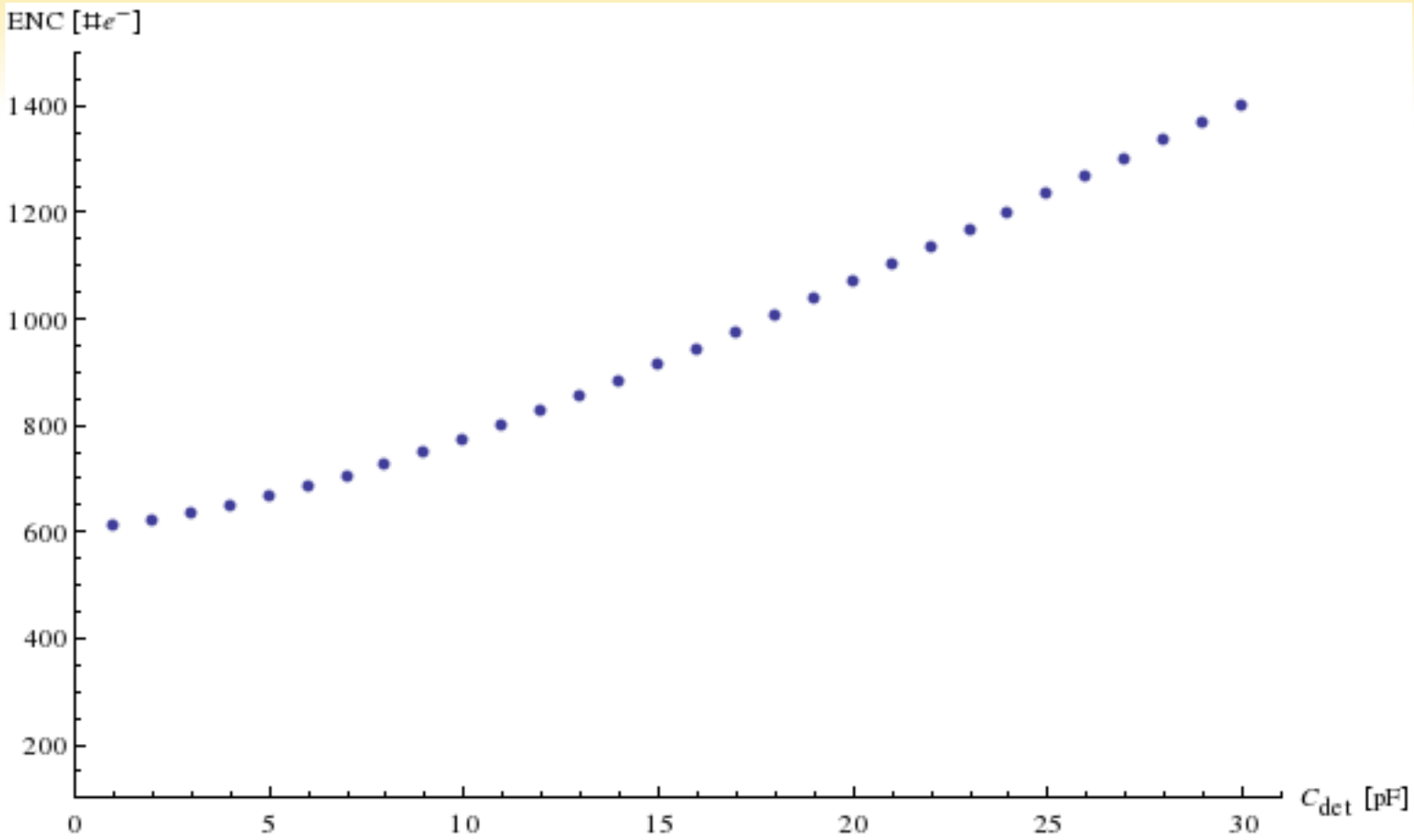

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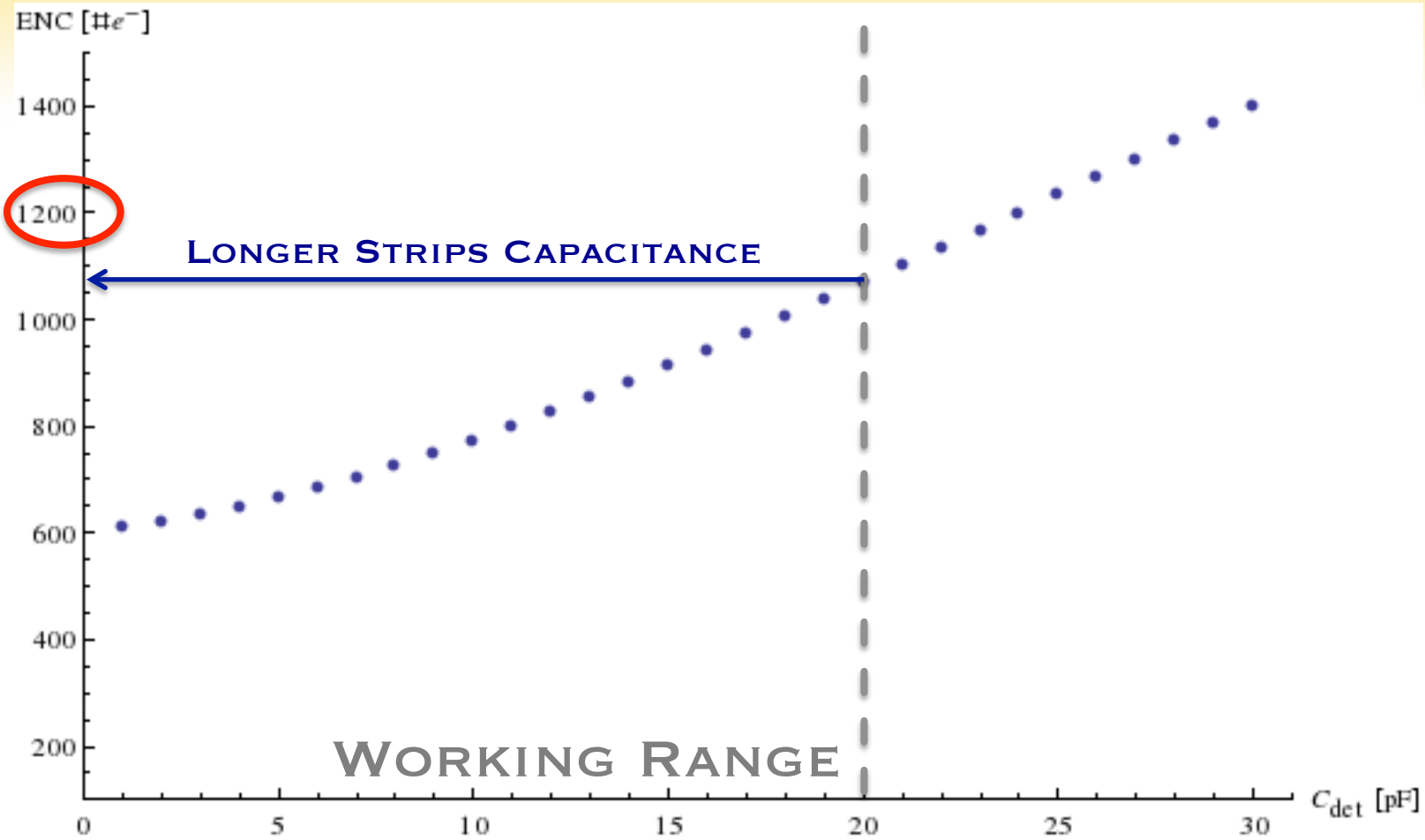

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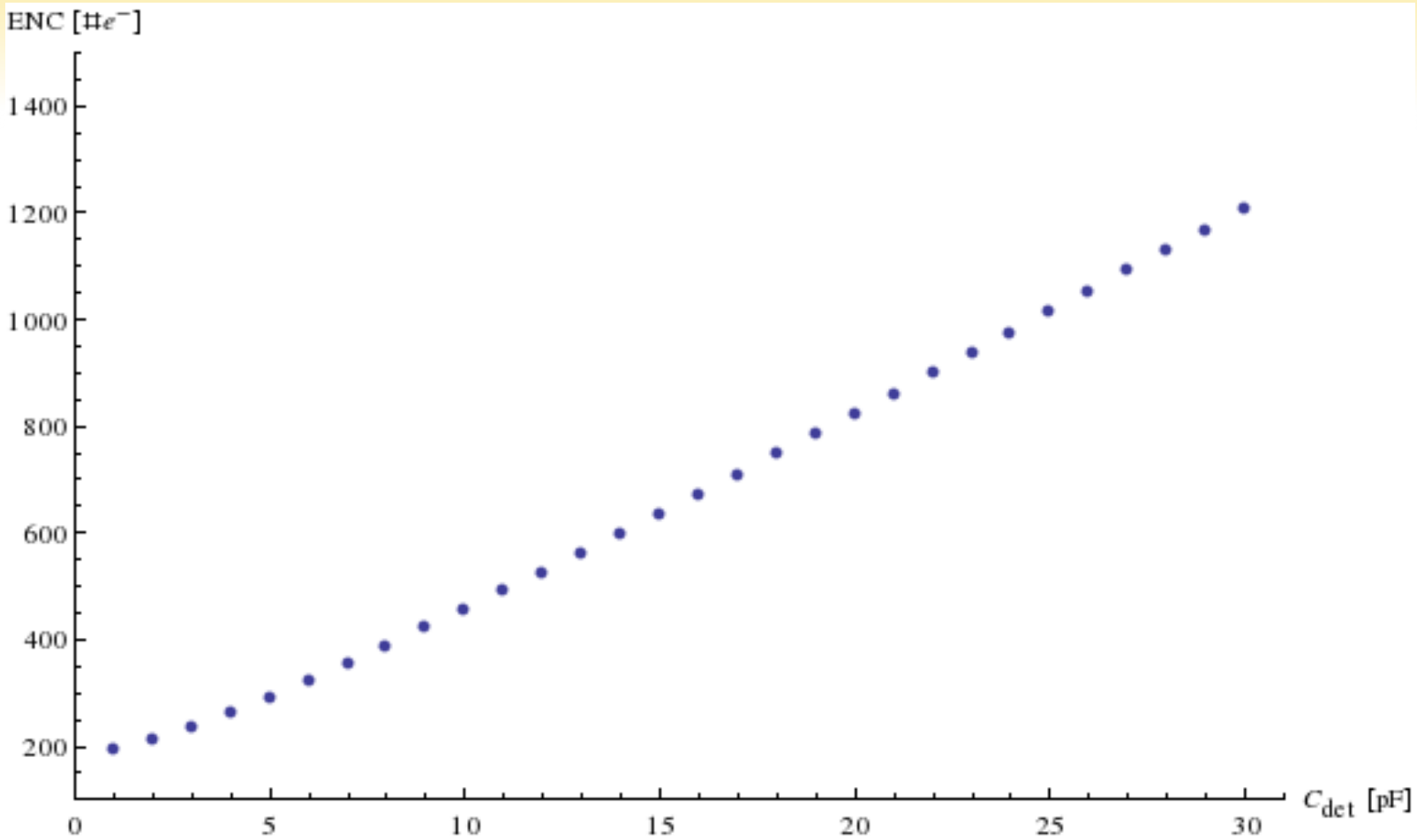

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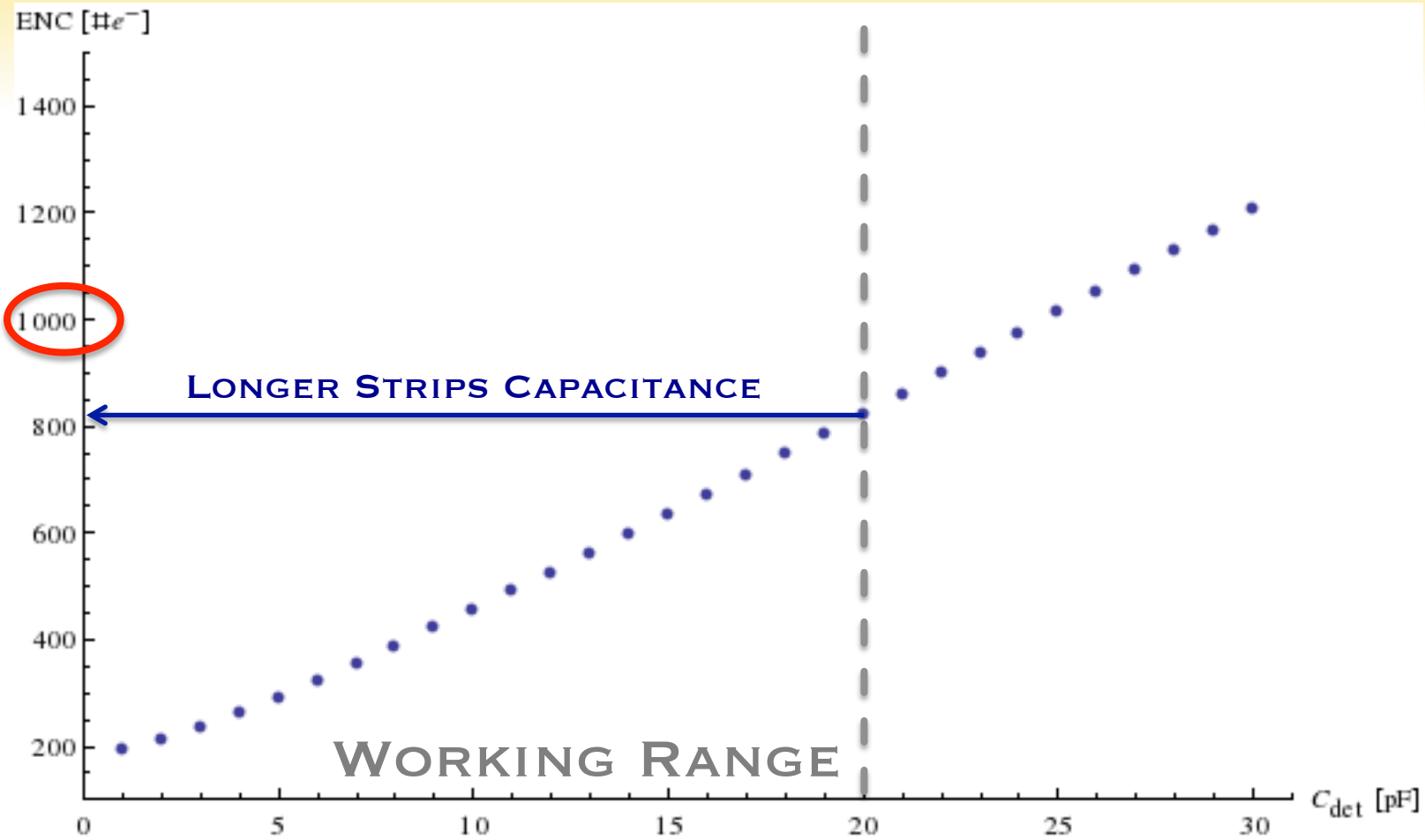

Some important parameters

Parameters (Q_{in}=1fC)	Negative Polarity Input	Positive Polarity input
ENC	1.1ke$^-$	800e$^-$
SNR (Q_{in}=4fC)	~ 52	~ 61
t_{peak}	21.6ns	23.9ns
Output rms Noise	1.6mV	3.8mV
Signal length (Q_{in}=40fC)	~430ns	~400ns

Old VS New chain

- ✓ Dual-polarity capability
- ✓ $ENC_{MAX}[C_{det}=20pF]$:

  ~1.4ke⁻ → ~1.1ke⁻ (ATLAS noise ~1.5ke⁻)

- ✗ Maximum signal length: x2 before

Conclusions and Perspectives

- First two stages: ready for layout
- Last stage: under study
- Comparator: layout done

- Understand key parameters
- Layout all the stages
- Submit

Conclusions and Perspectives

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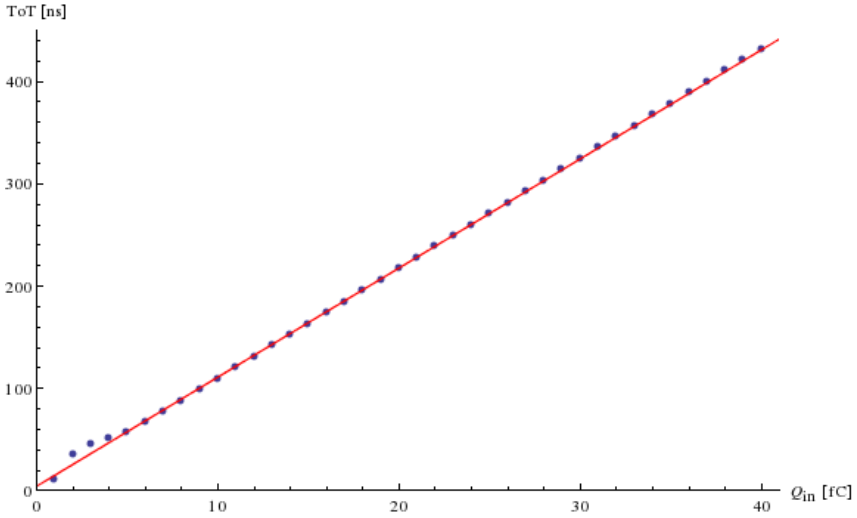
Thank you for your
kind attention

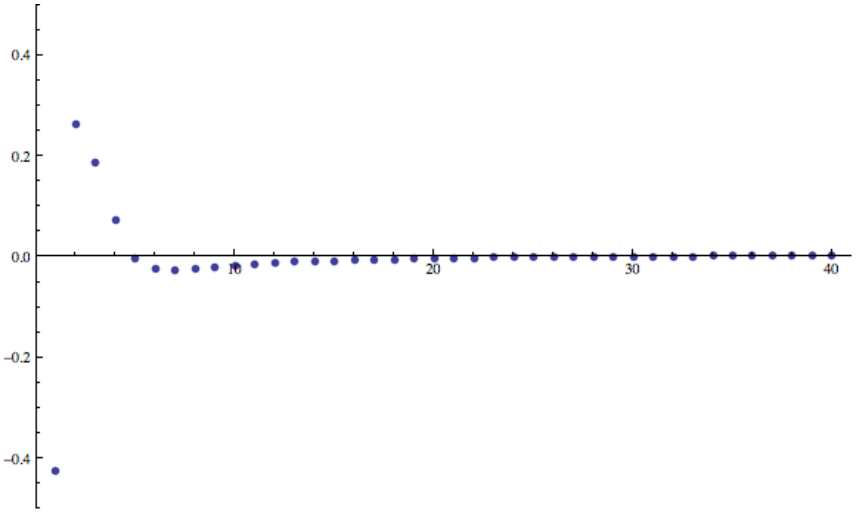
Backup Slides

NIP Configuration

Linearity

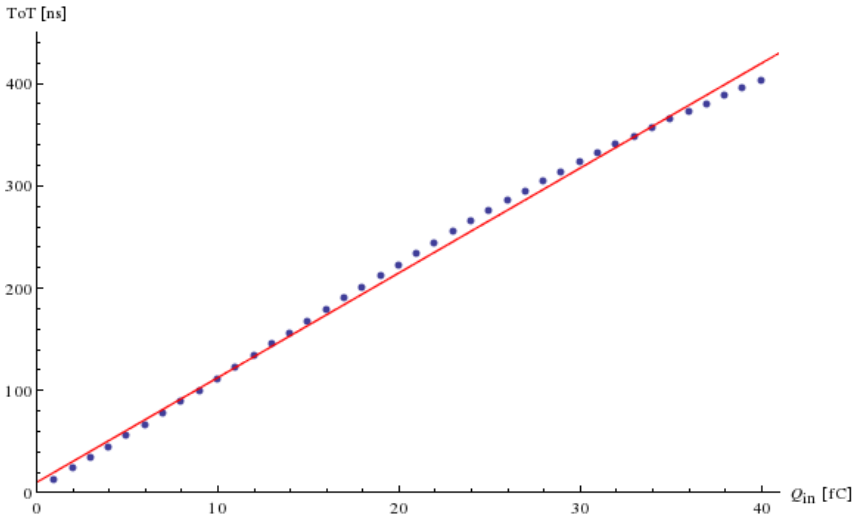


Residual Plot



PIP Configuration

Linearity



Residual Plot