PANDA FEE-DAQ Workshop

Sezione di Torino

Update on the electronics for the MVD pixel detector

G. Mazza
on behalf of the Torino MVD pixel group

Pixel Detector

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Pixel size	*100 × 100 μm²*
Chip active area	*11.4 × 11.6 mm²* *(116 rows, 110 columns)*
dE/dx measurement	*ToT, 12 bits dynamic range*
Max input charge	*50 fC*
Noise floor	*<32 aC (200 e⁻)*
Input clock frequency	*155.52 MHz*
Time resolution	*6.43 ns (1.86 ns r.m.s.)* *12.86 ns (3.71 ns r.m.s.)*
Power consumption	*< 800 mW/cm²*
Max event rate	*6.1 · 10⁶*
Total ionizing dose	*< 100 kGy*

Module readout

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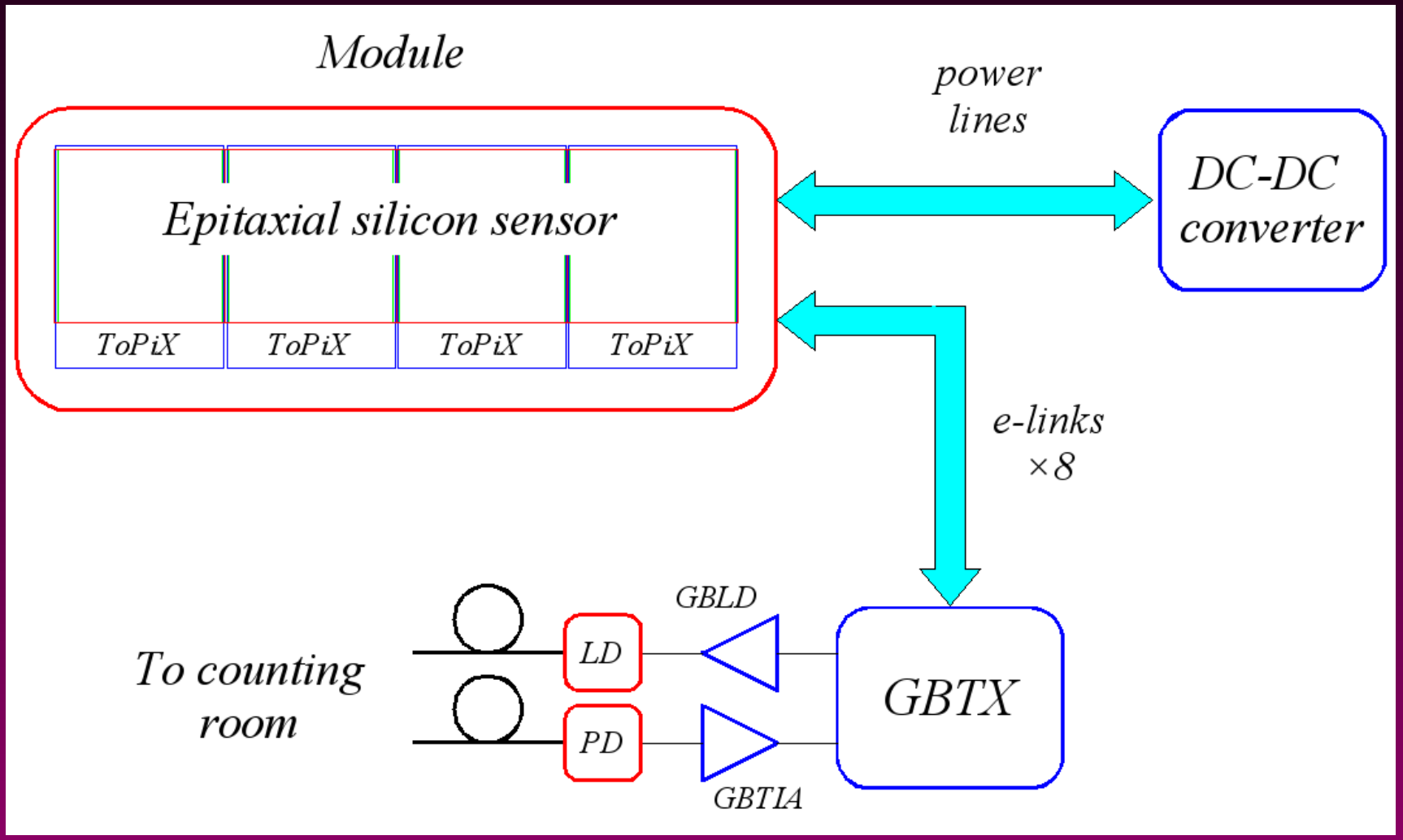

ToPiX v4

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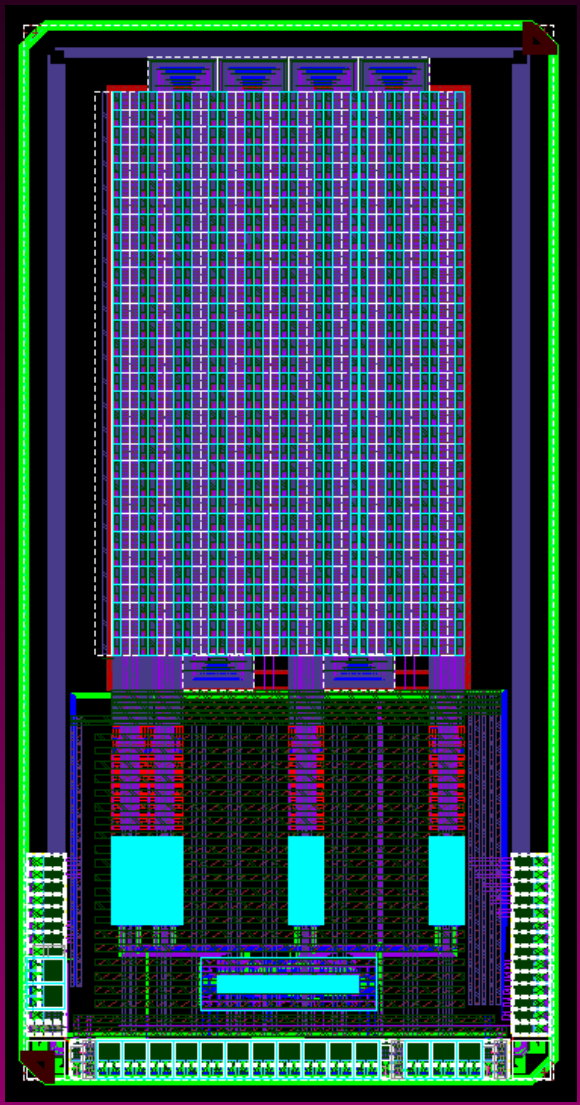

- Size : 3 mm × 6 mm
- CMOS 130 nm
- 640 pixel cells, 2×2×128 and 2×2×32 columns
- Hamming encoding and TMR pixel logic protection schemes
- Compatible with v3 sensors
- Clock frequency 160 MHz
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT-compatible SLVS I/O
- *Submitted on Nov 18th 2013*

LVDS - SLVS

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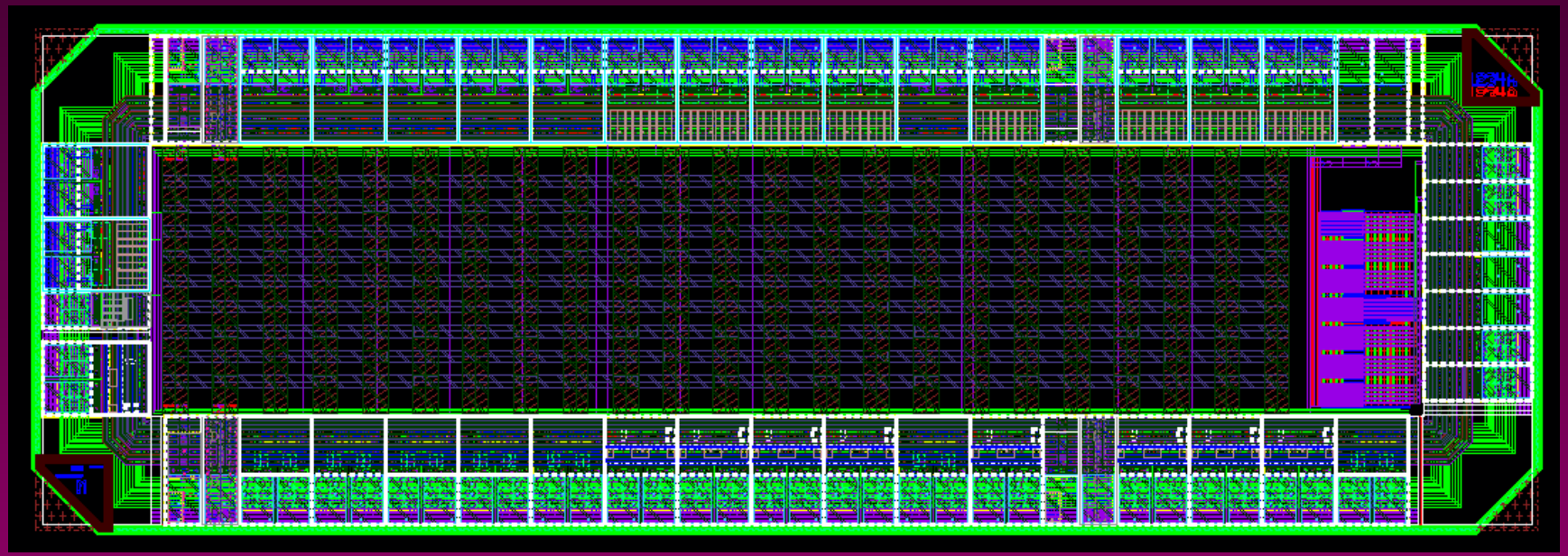
- Size : 3 mm × 1 mm
- CMOS 130 nm
- Pinout matches ToPiX v4 one
- 7 LVDS in – SLVS out
- 9 SLVS in – LDVS out
- *Submitted on Nov 18th 2013*



Analog cell

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Three improvements :

- Analog gain *(not ToT gain)* increase for better linearity in the sub 1 fC region
- Radiation tolerance of the clipping circuit
- Threshold control DAC linearization

Analog gain

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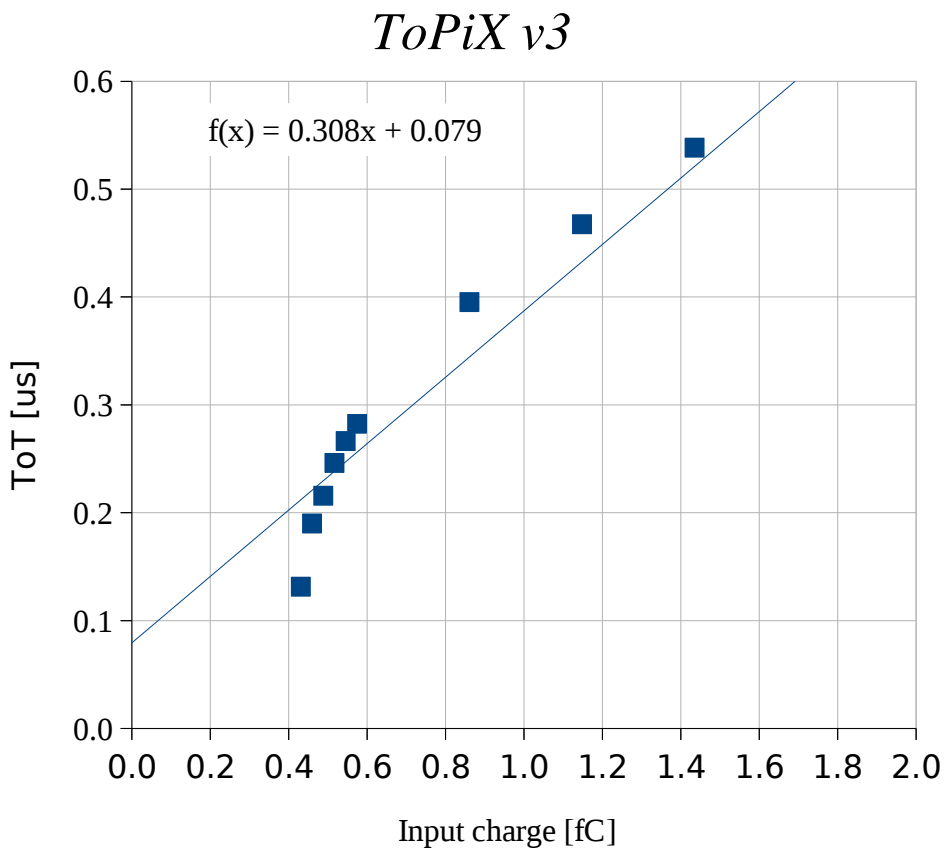

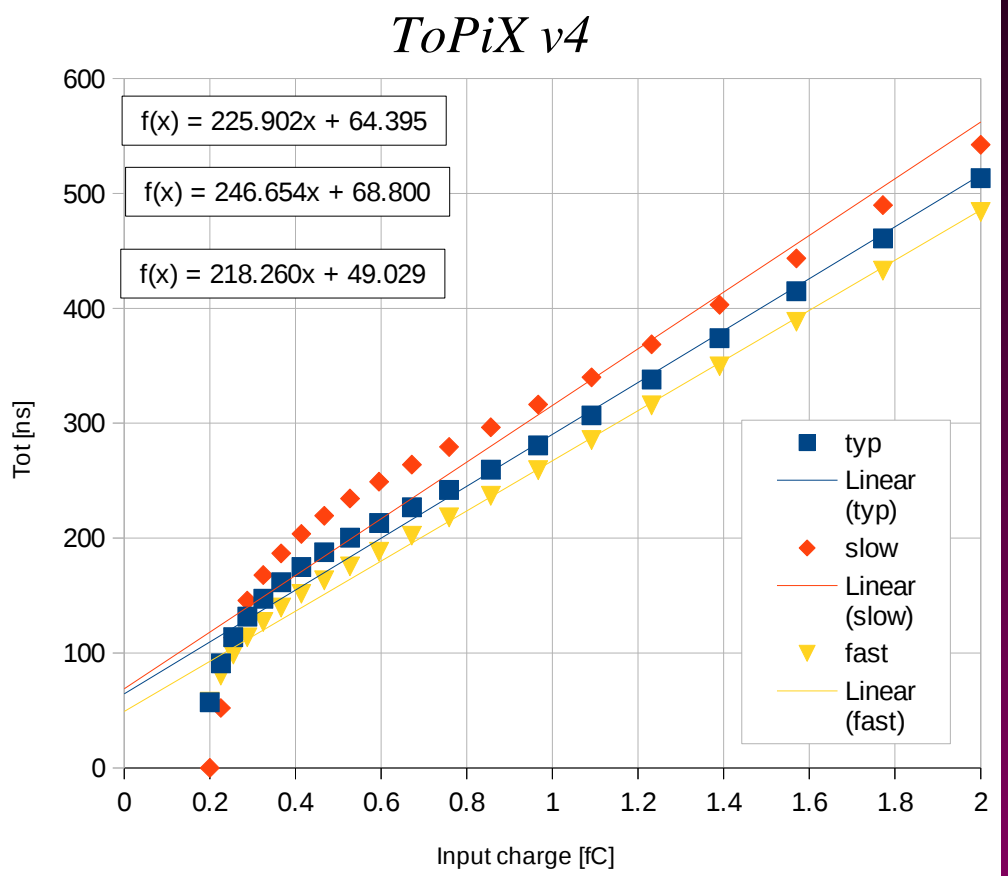

Analog gain : 76 mV/fc (s)
66 mV/fC (m)

Analog gain : 122 mV/fC (s)

Analog gain - full range

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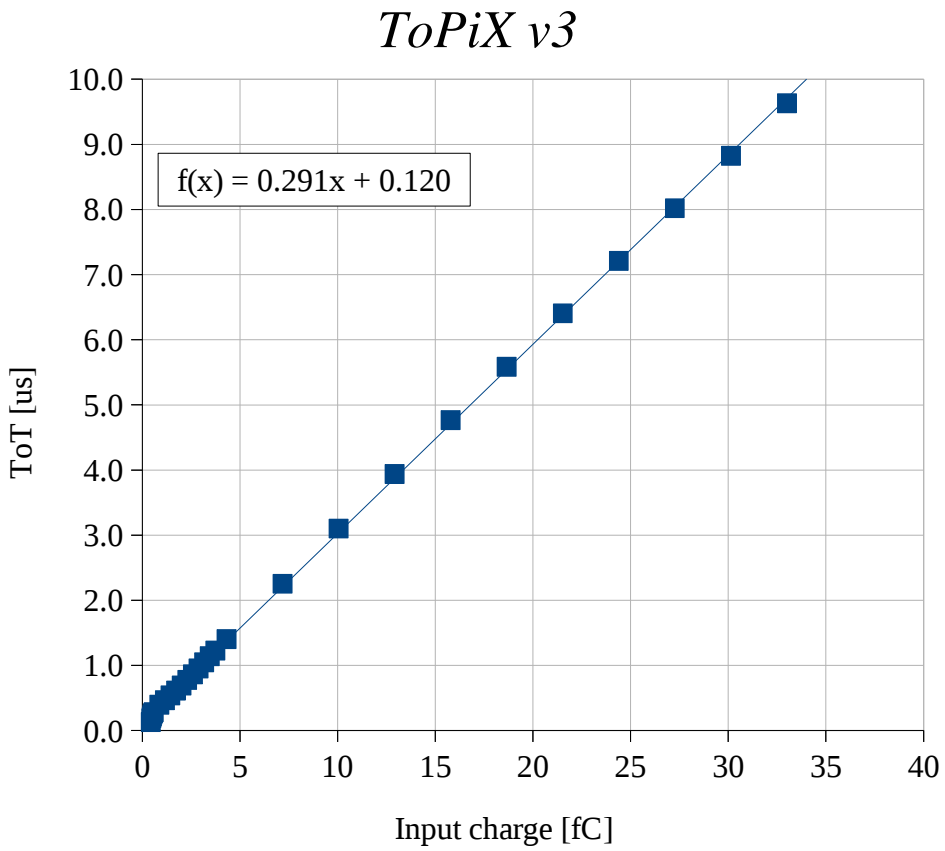

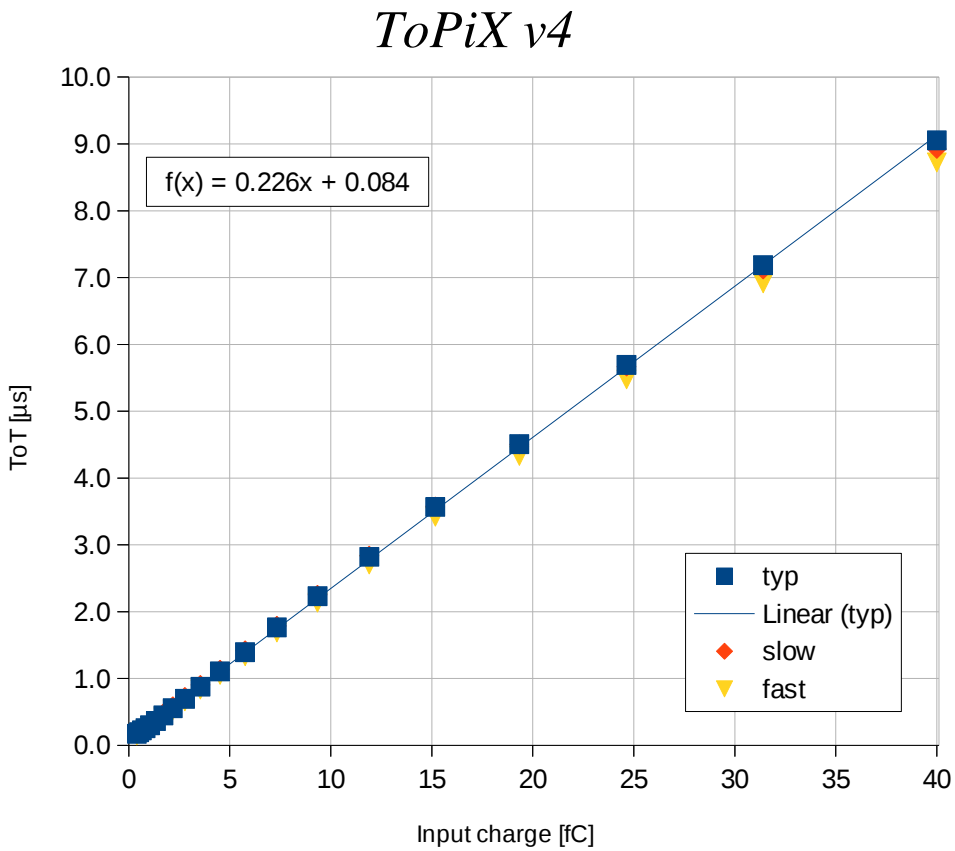

Clipping circuit

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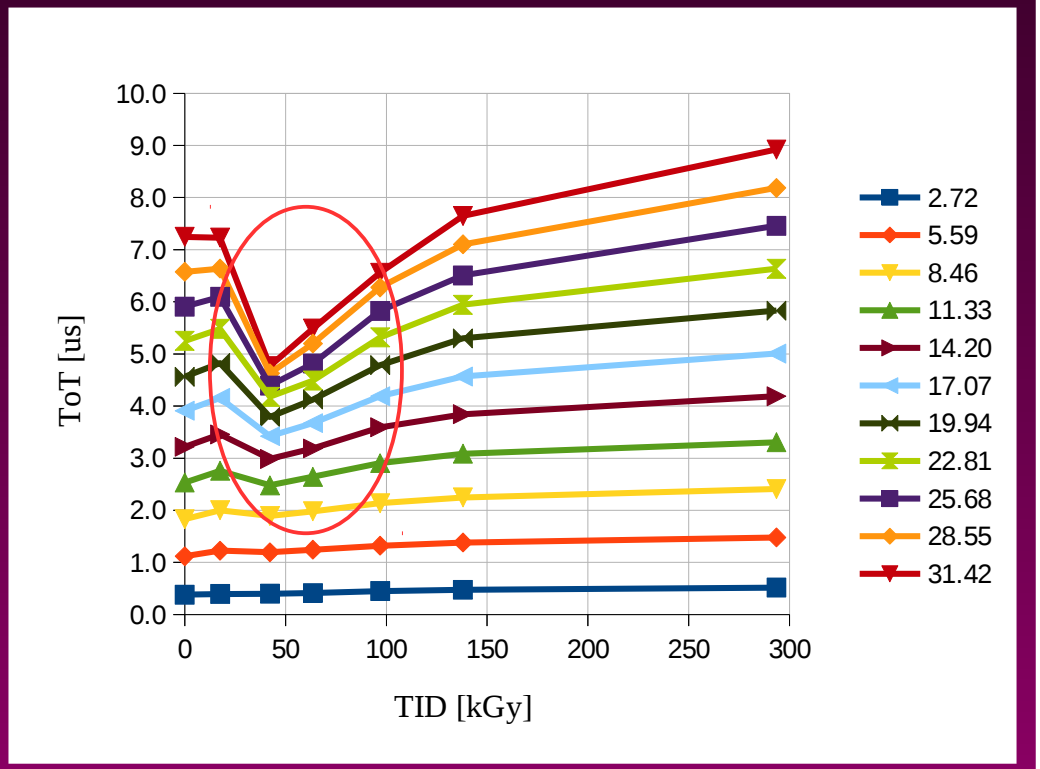
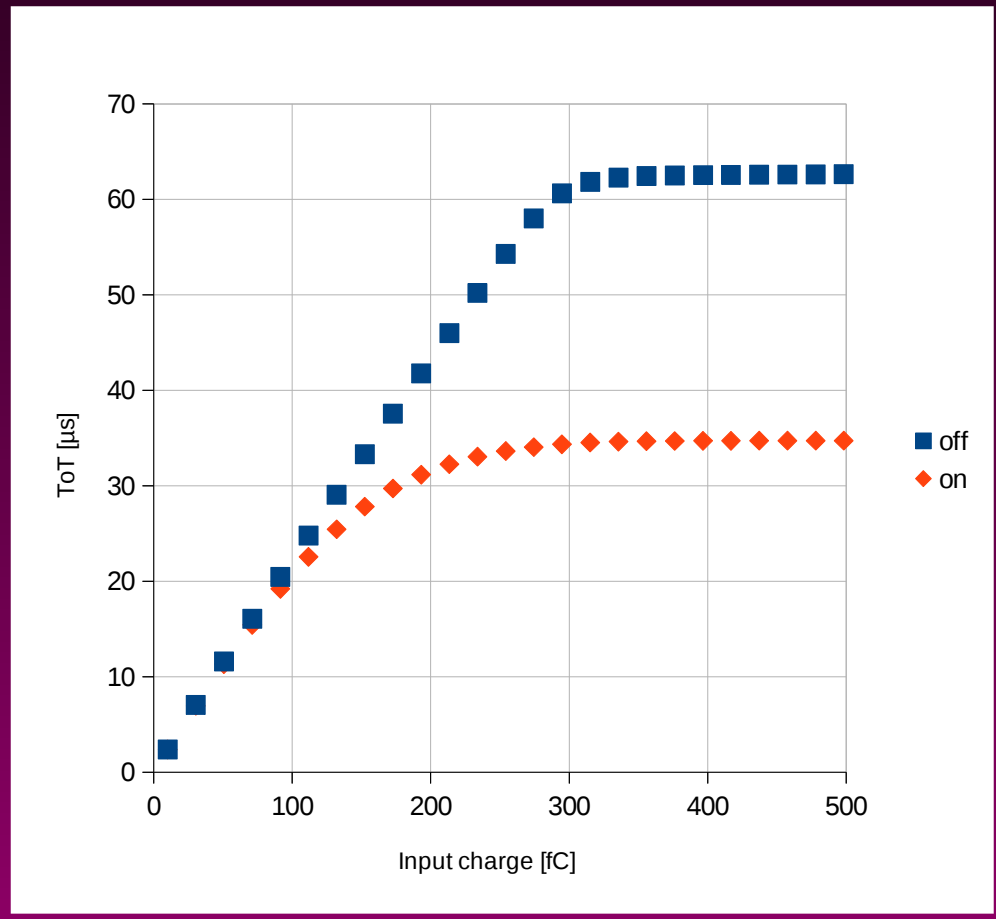
- nMOS-based clipping circuit had problem with irradiation
- New pMOS based circuit





Threshold linearization

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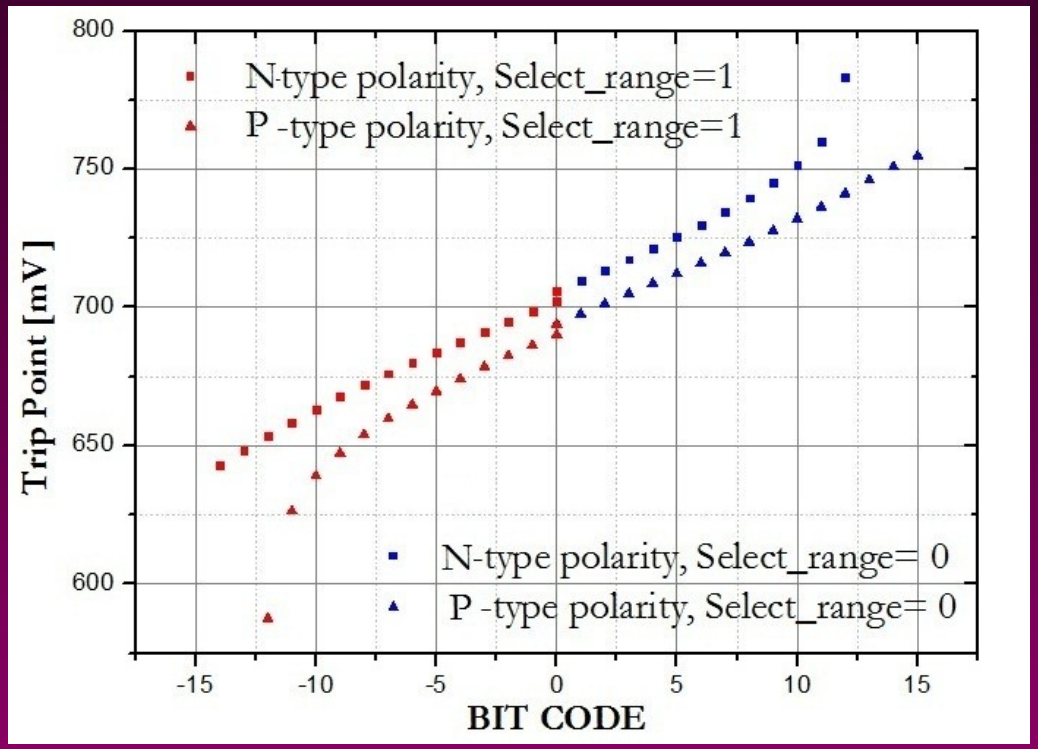
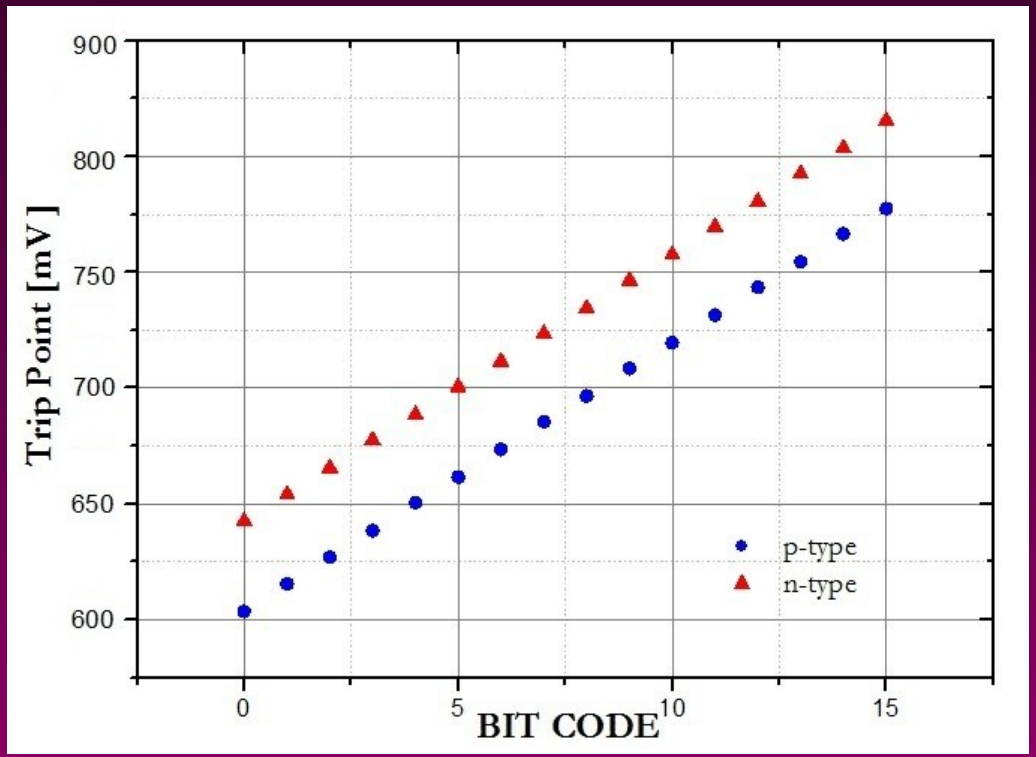
- DAC threshold control is via current injection → control is not linear
- New I-V converter circuit introduced in the pixel cell (*J. Olave*)





Pixel cell

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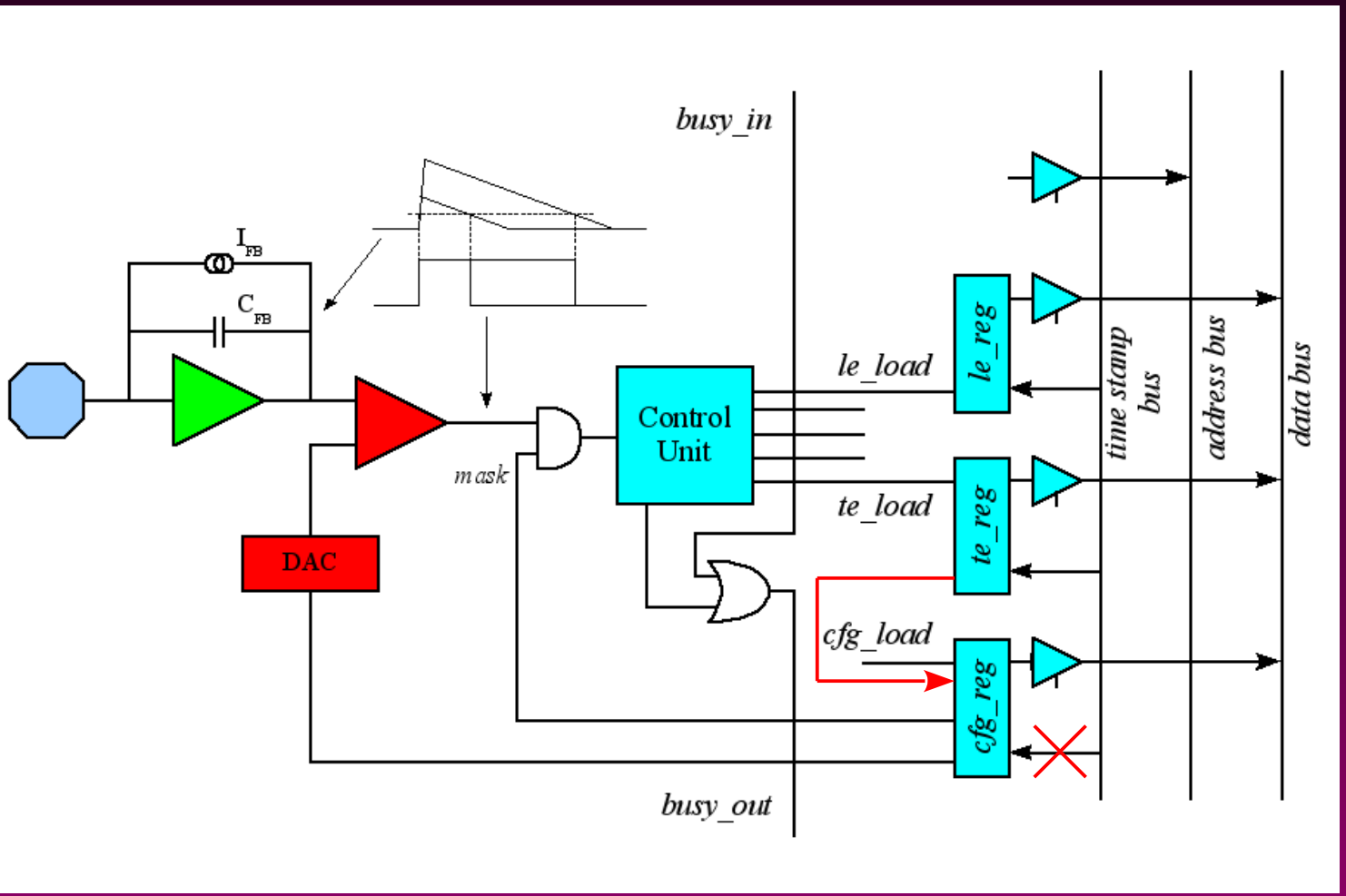

le_reg and te_reg are implemented via DICE-protected latches

cfg_reg is implemented with TMR/Hamming corrected DFF

Time stamp bus is NOT buffered at the pixel level

Pixel cell SEU protection

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- Leading edge and trailing edge registers will use latches with DICE scheme
  - 12 bits register size : 4.8 µm × 98.4 µm
- Configuration register will use DFF. Two possible protection schemes :
  - ✔ Hamming encoding with self correction
  - ✔ Triple redundancy
- Automatic P&R for control logic and configuration register over an area of 39.2 µm × 98.0 µm. Occupancy is 82% for Hamming encoding and 90% for TMR.
- Total on-pixel digital area : 50 µm × 100 µm (as in ToPiX v3)

New line driver

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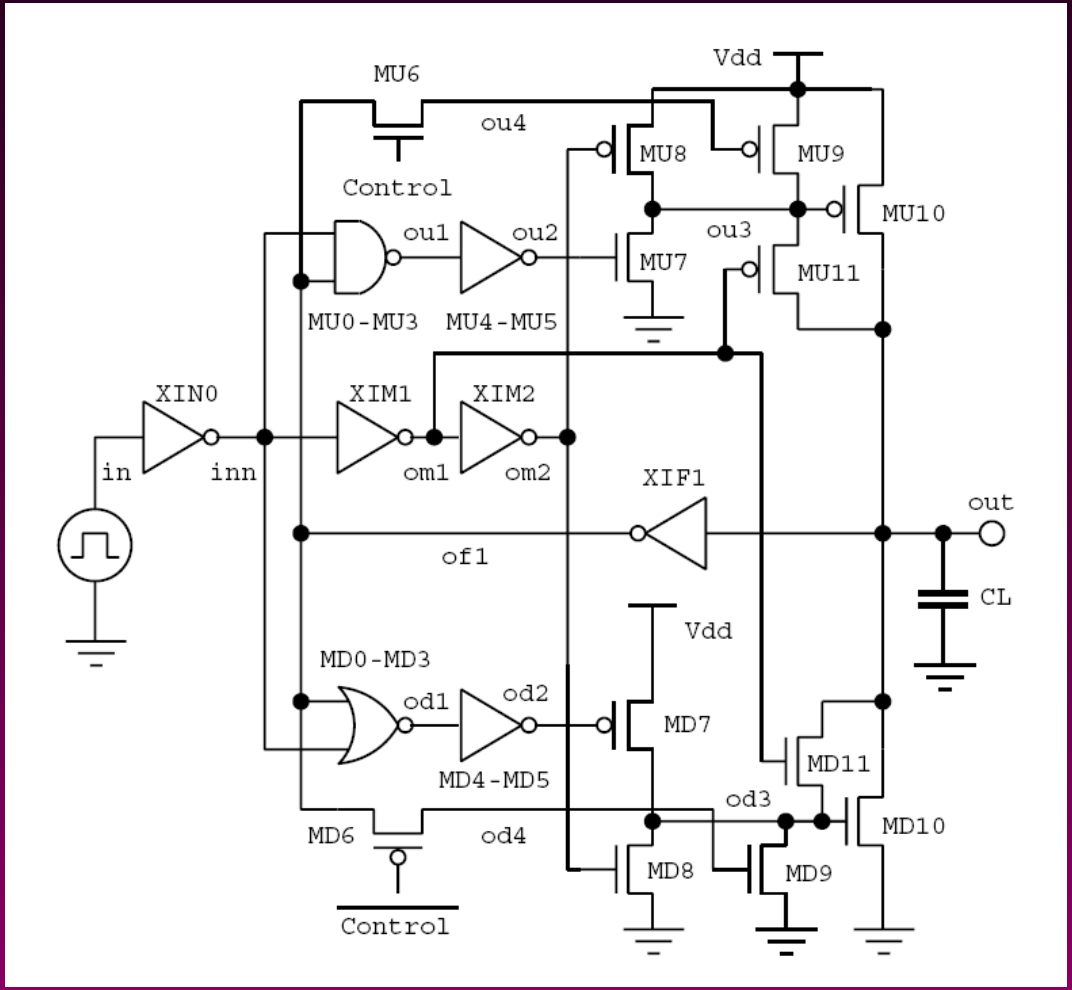
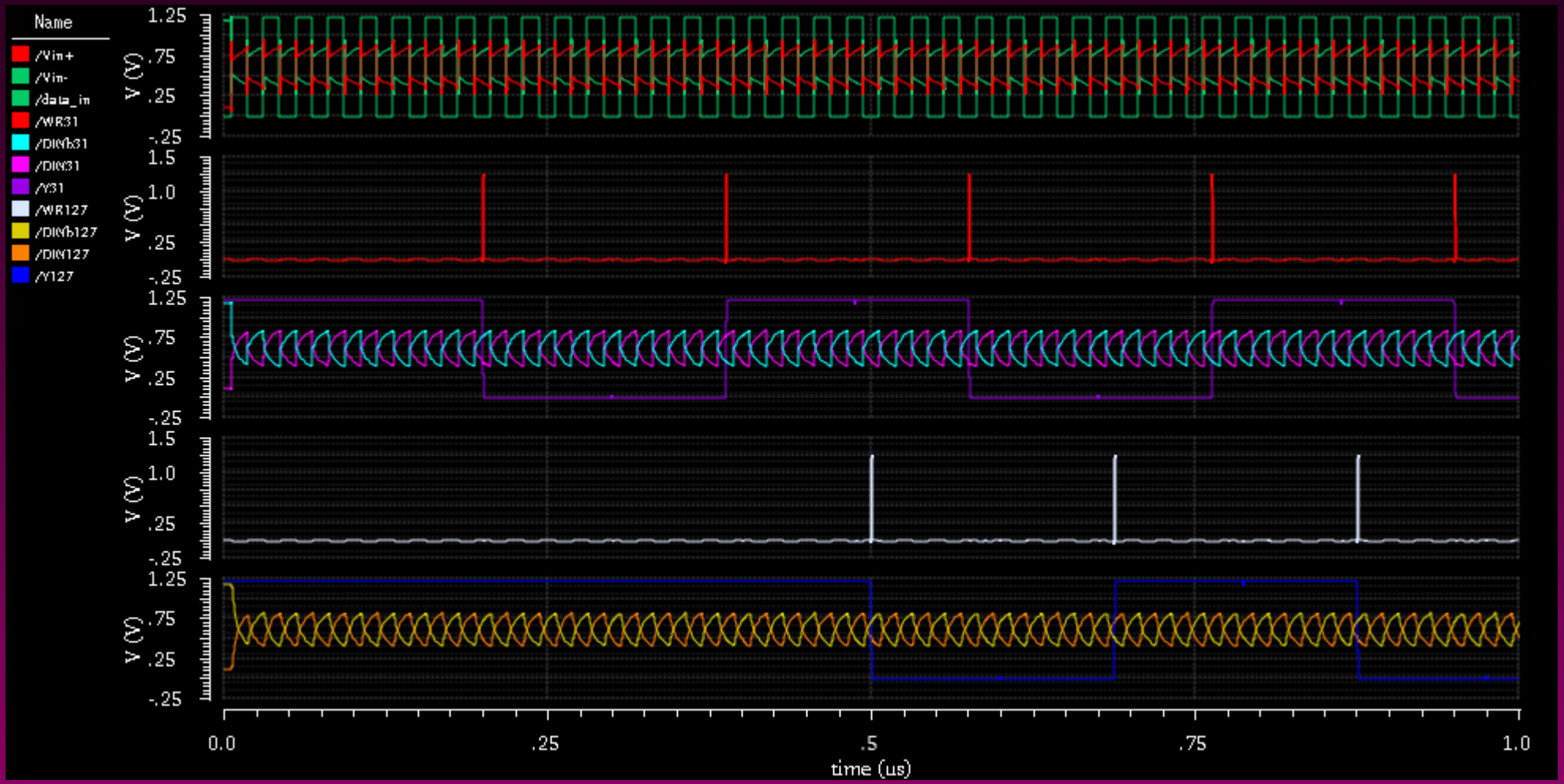


Provides both reduced voltage swing and pre-emphasis or full voltage swing

J.C.Garcia, J.A.Montiel, S.Nooshabadi
Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects
ISCAS 2007

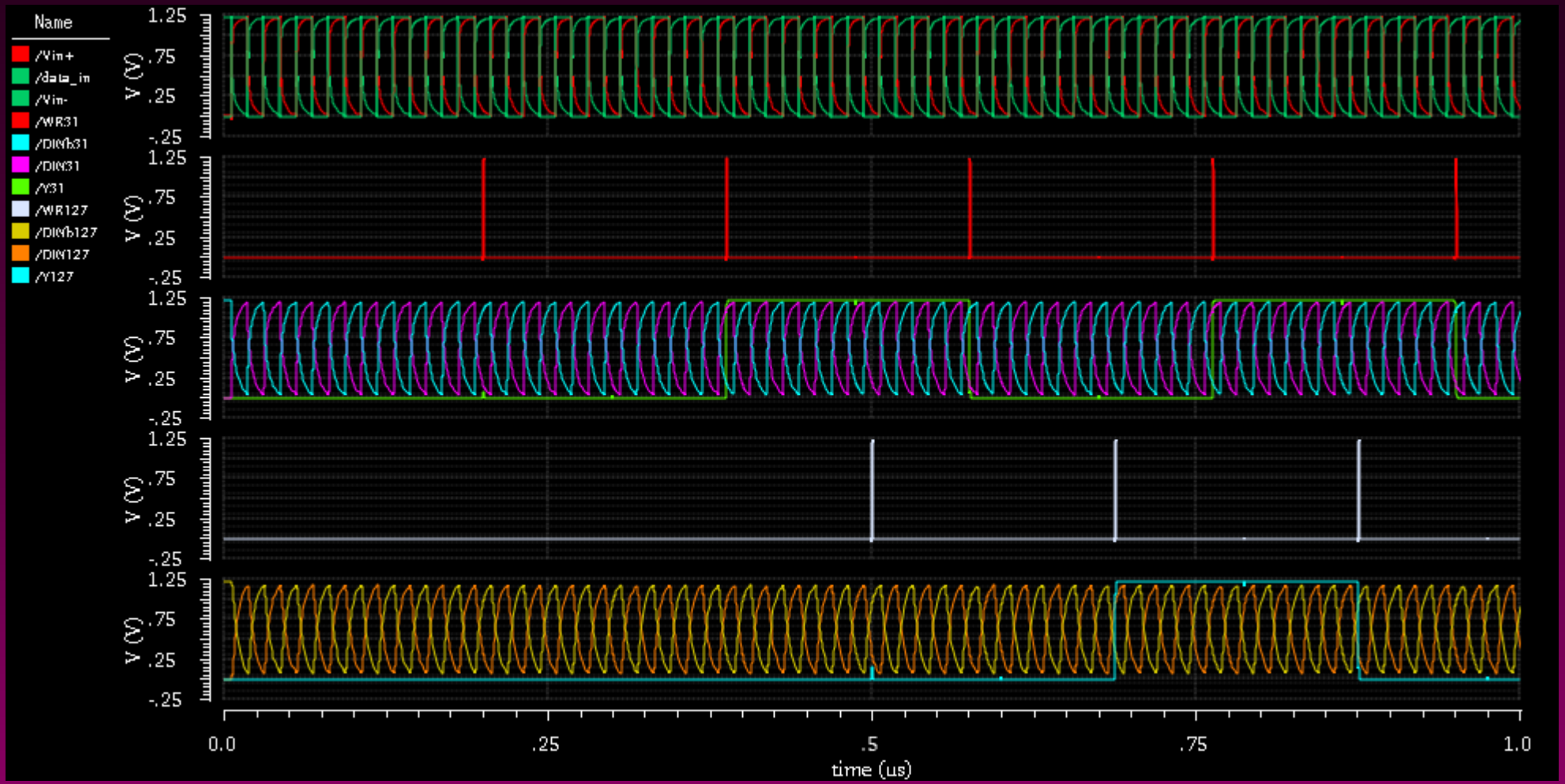
Time stamp transmission - pe

Sezione di Torino



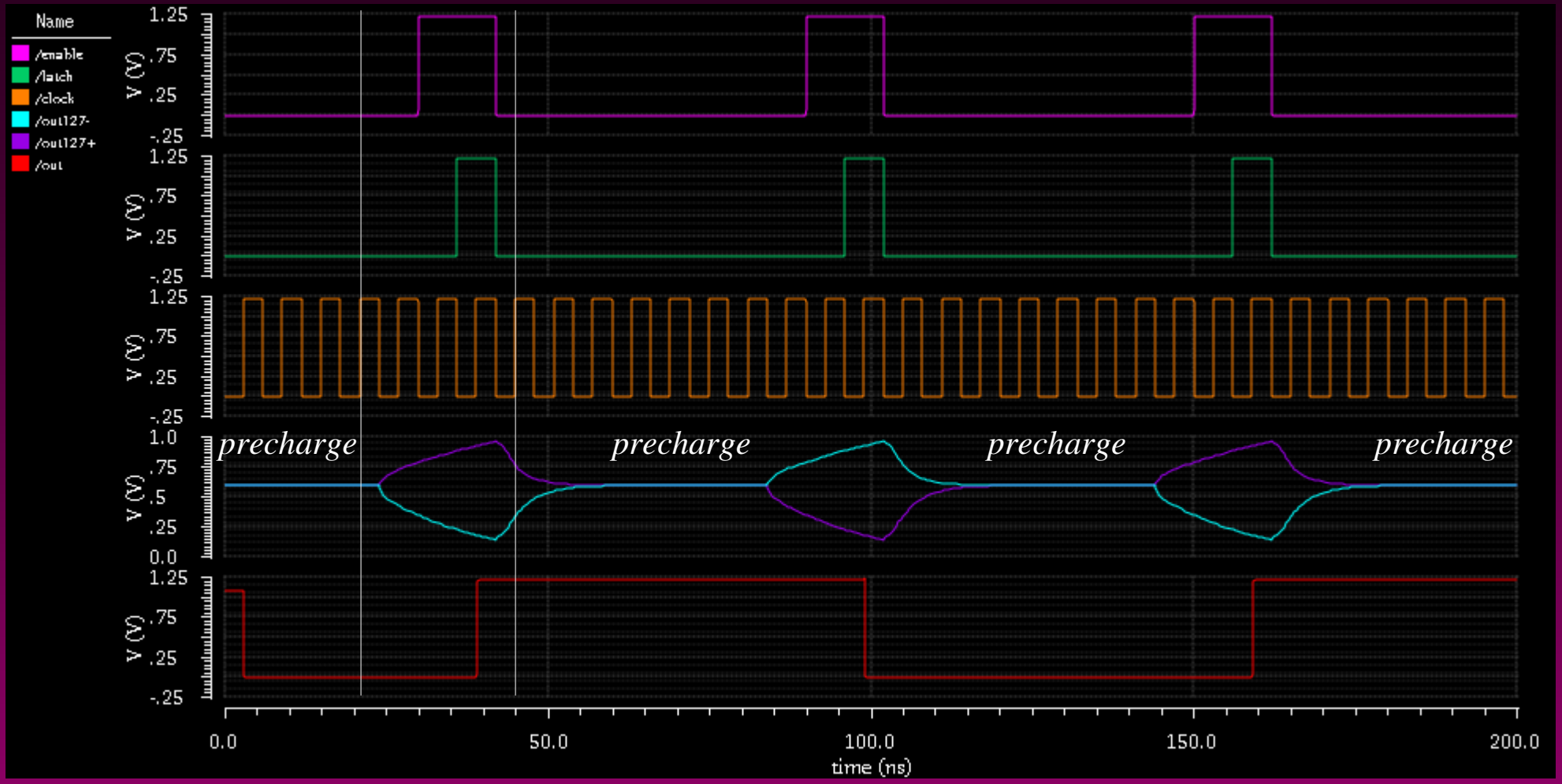
Time stamp transmission - no pe

Sezione di Torino



Bus readout

Sezione di Torino



Data format

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2	12	8	12	6	
01	Chip address	FC	Not used	ECC	*Frame header packet*

2	14	12	12	
11	Pixel address	Leading edge time	Trailing edge time	*Data packet*

2	16	16	6	
10	# of events	CRC	ECC	*Frame trailer packet*

2	38	
00	idle code (Hex 3A55AA55AA)	*Idle packet*

Other features

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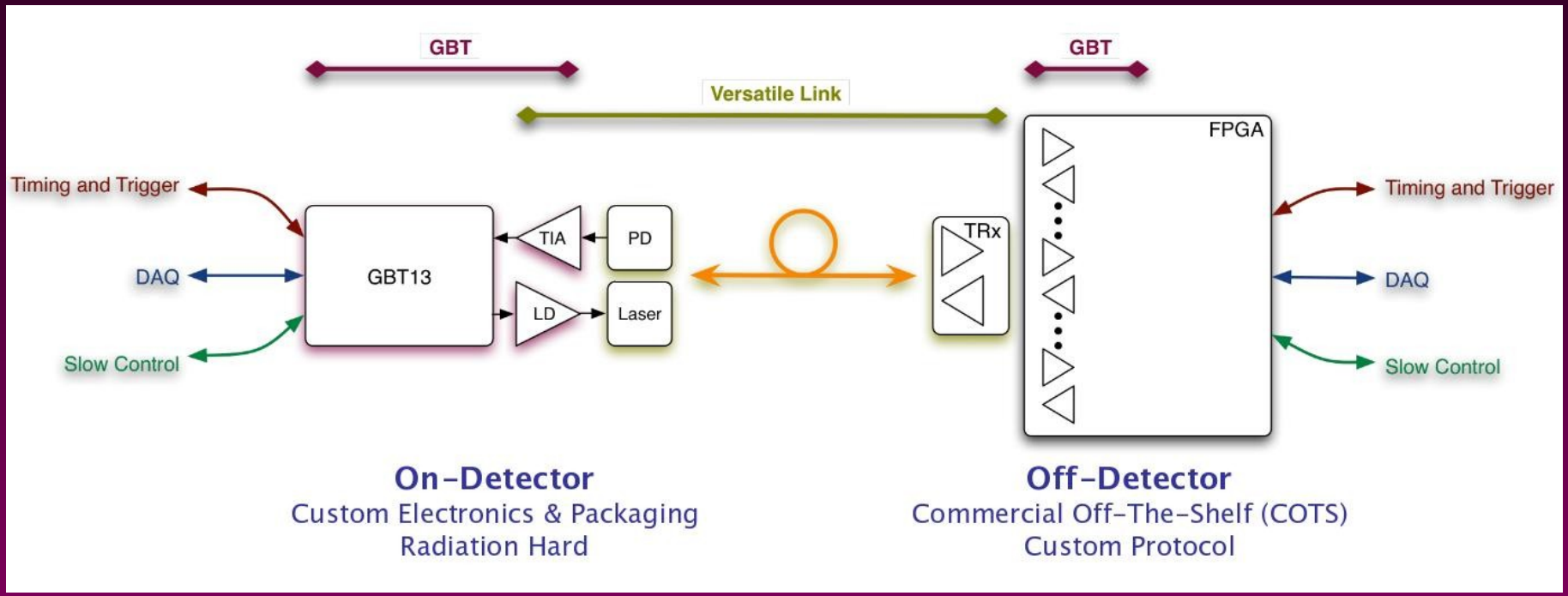
Output frequency	*160 Mb/s*	*320 Mb/s*
Time stamp counter frequency	*160 MHz*	*80 MHz*
Time stamp mode	*Binary*	*Gray*
Idle packet	*off*	*on*
Analog timeout	*off*	*on*
Detector type	*n-type*	*p-type*
SLVS current control	*0000 (max)*	*1111 (off)*
Driver pre-emphasis	*off*	*on*

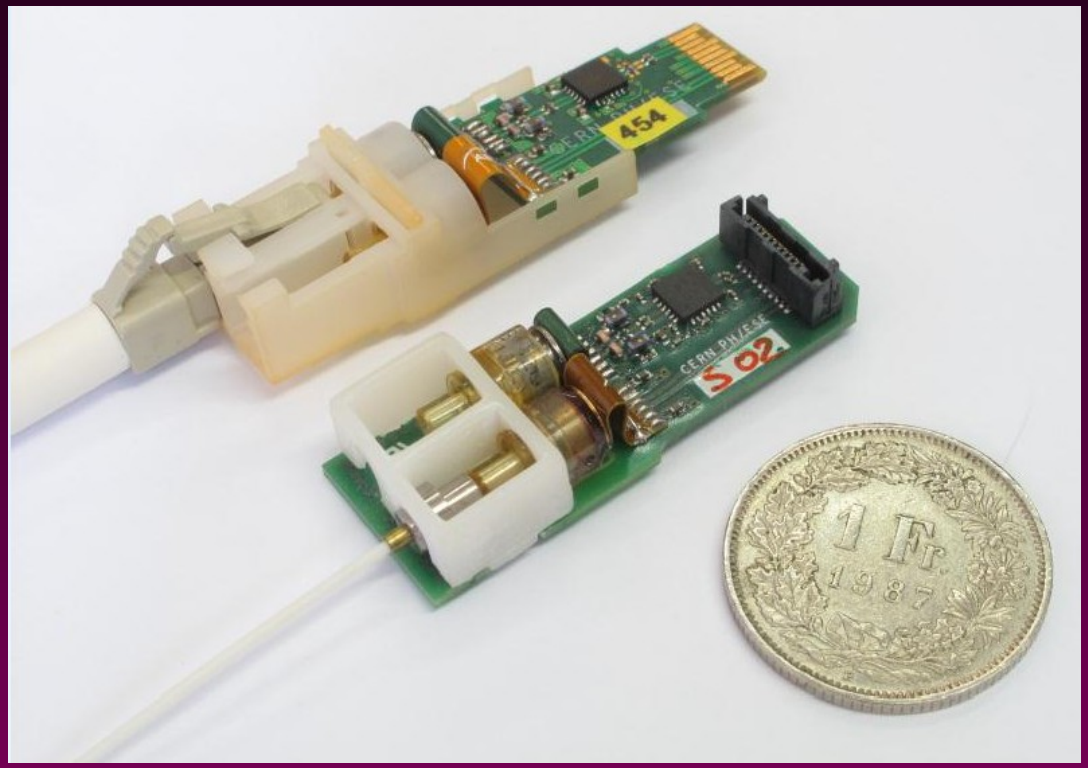
GBT

Sezione di Torino



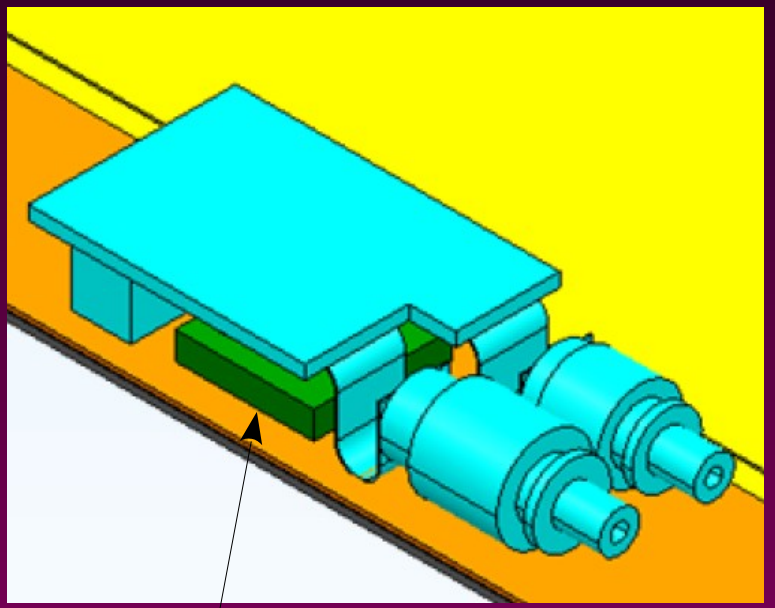
GBT components

Sezione di Torino



Versatile Transceiver
$50\times14\times10$ mm^3
$45\times15\times8$ mm^3
(F.Vasey, J.Troska, C.Soos)

Proposed arrangement for CMS tracker (C.Soos)



GBTx 10×10 mm^2
(P.Moreira et al.)

GBT status

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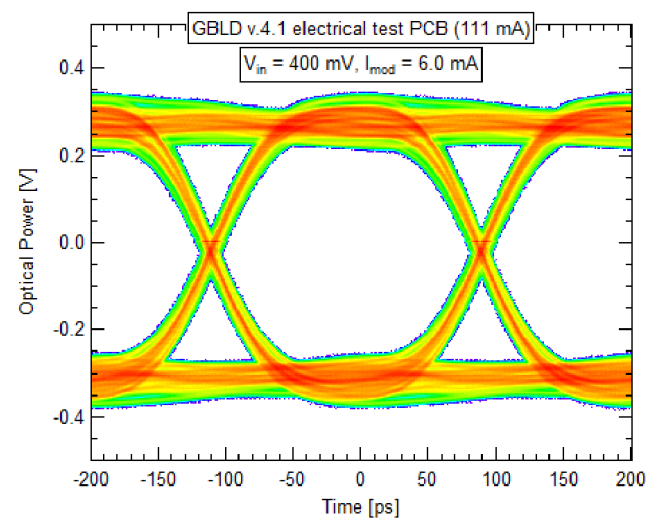
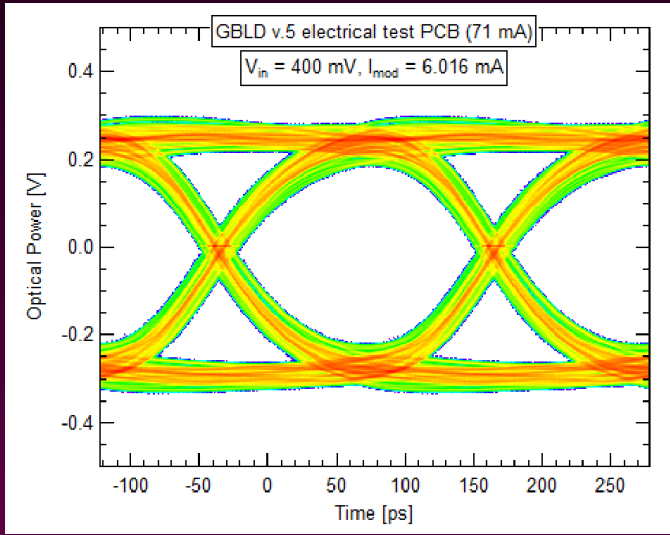
- GBTX :
  - Final chip received, tests ~ ok. Production in 2h2014.
  - Max power consumption 2.2 W (with all functionality on)
- GBTIA :
  - Ready for production in 2h2014
- GBLD :
  - Current version (GBLD v4) can work up to 10 Gb/s with a power consumption of ~300 mW (with VCSELs)
  - A low power version (GBLD v5) targeted at VCSELs can work up to 5 Gb/s with a power consumption of ~200 mW (with VCSELs)
  - GBLD v4 will be produced in 2h2014

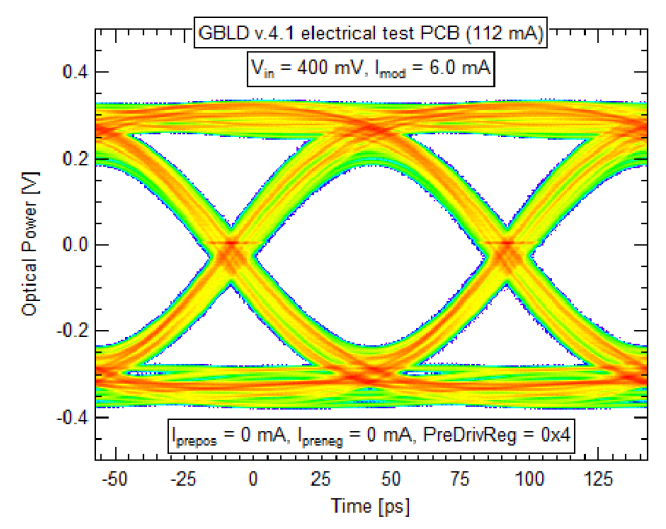
GBLD v4.1 & v5

Sezione di Torino

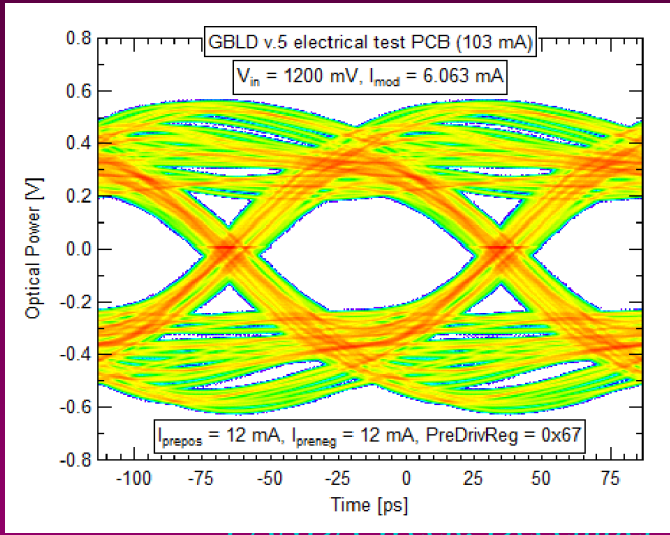


5 Gb/s





10 Gb/s



GBT plans

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- GBT chipset production foreseen in 2h 2014
- To be installed by LHC experiments during LS2 (2018)
- LpGBT : low power GBT
  - Target power consumption : 500 mW *(75% reduction !)*
  - Technology : CMOS 65 nm
  - 2 GBTX versions (LpGBT with SerDes only and full GBTX)
  - High bandwidth (4.8 Gb/s downlink, 4.8/9.6 Gb/s uplink)
  - Development will start in 2014
  - *Not yet an approved project...*

Power regulator

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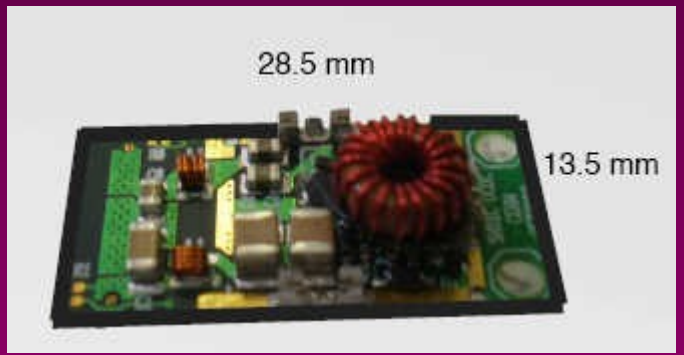
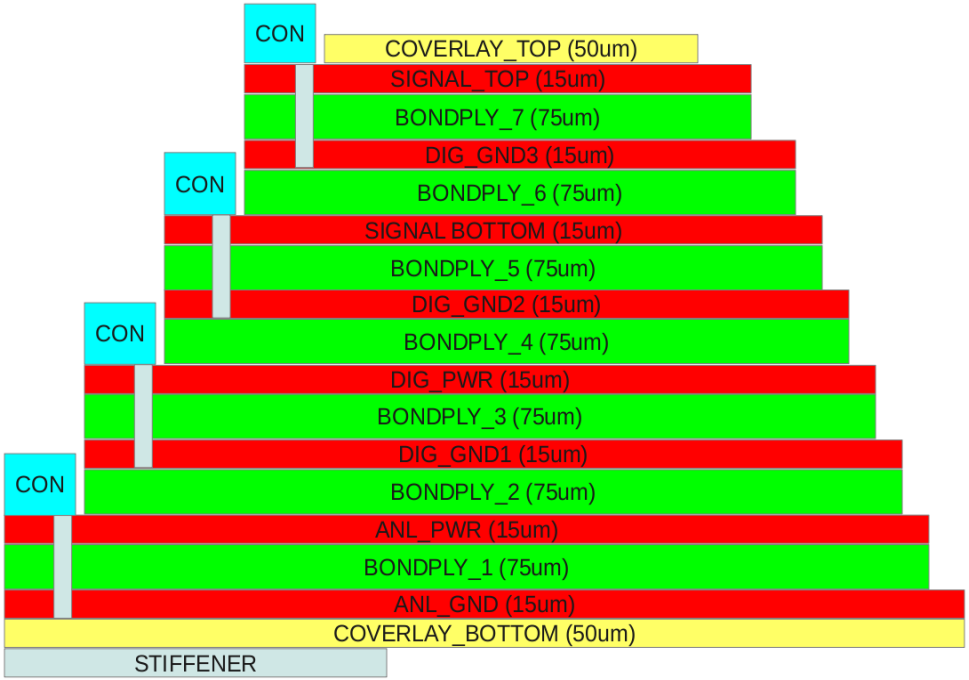
- ToPiX power supply 1.2 V – I_{DC} ~ 1 A (estimated)

  → *voltage drop on cables is not negligible*

- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- Current CERN version : V_{IN} 10÷12 V, V_{OUT}=1.2÷3.3 V, I_{OUT} < 3 A
- V_{OUT}= 1.5 V, I_{OUT} < 3-4 A now avail.
- Tests with ToPiX v3 ongoing



Hybrid bus



The aluminum hybrid bus for the largest super module manages 6 readout circuits; the purchasing order for some samples was placed at CERN.

Conclusions

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- ToPiX v4 has been submitted to foundry on Nov 18th
- Projected delivery date : Feb 14th 2014
- GBT project toward mass production in 6 months
- Tests on voltage regulators ongoing
- Low mass cables : prototype sent to CERN for production

KEEP
CALM
AND
NEVER SAY NO
TO PANDA

MVD Meeting

Sezione di Torino

Backup slides

ToPiX v3

Sezione di Torino

- Layout submitted on February 7th – received May 16th 2011
- 4.5x4 mm^2 die area
- CMOS 0.13 µm DM technology
- Triple redundancy-based SEU protection
- End of column logic
- 160 Mb/s SLVS serial output
- Pads for bump bonding

ToPiX v3 layout

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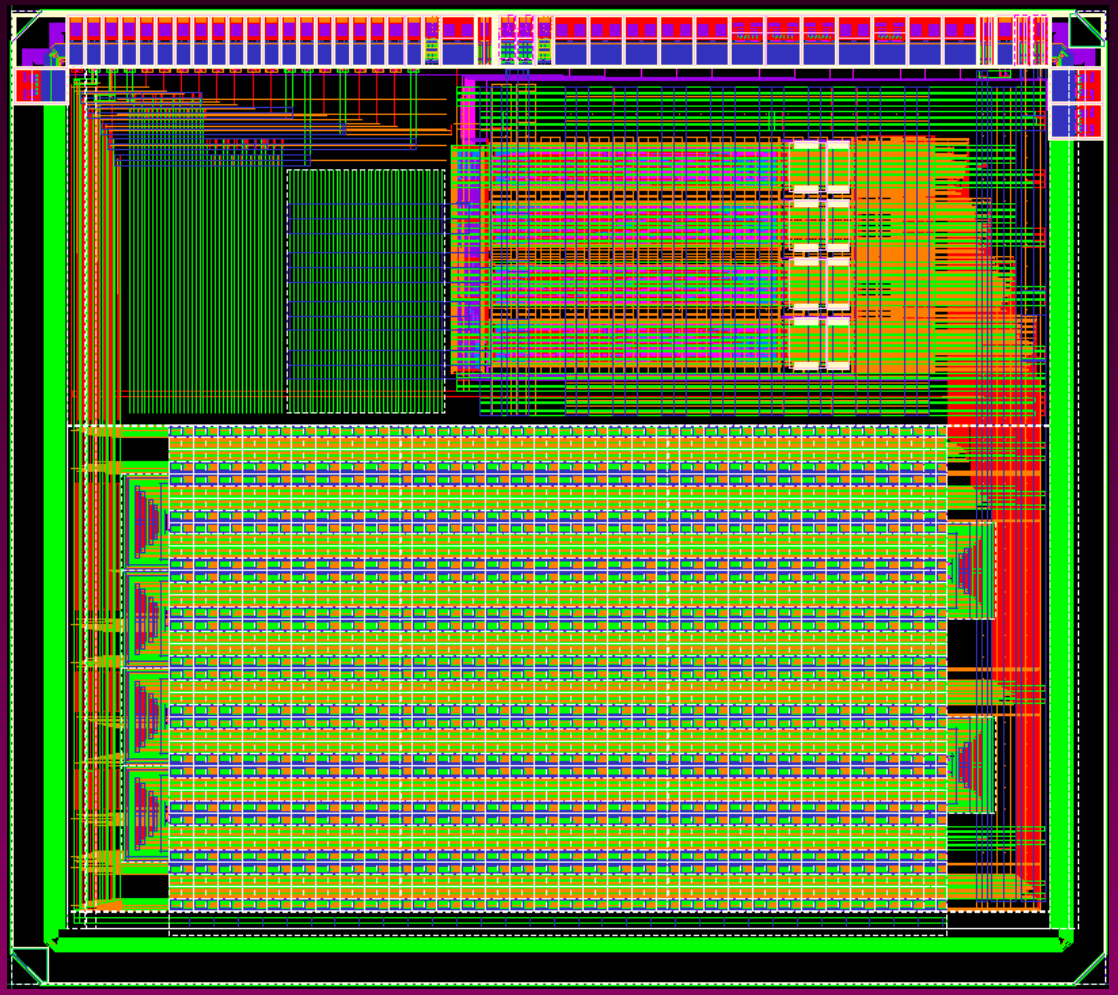

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

TID tests - ToT

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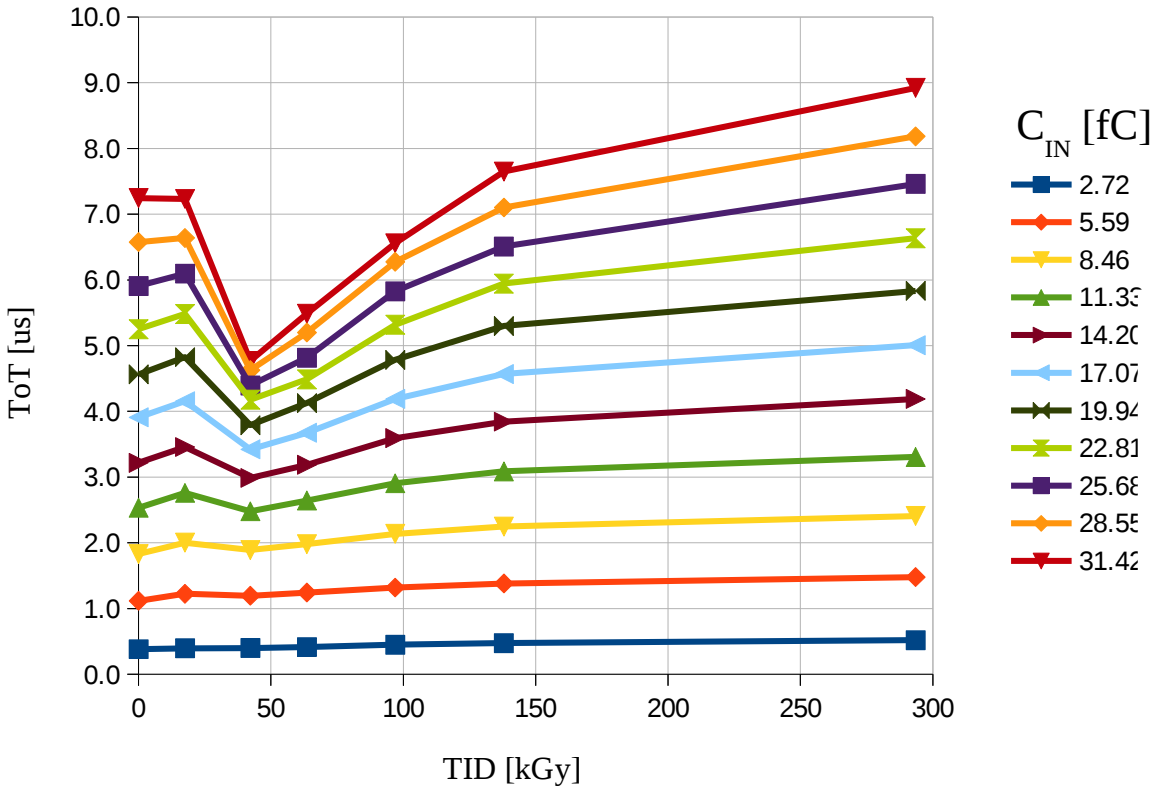
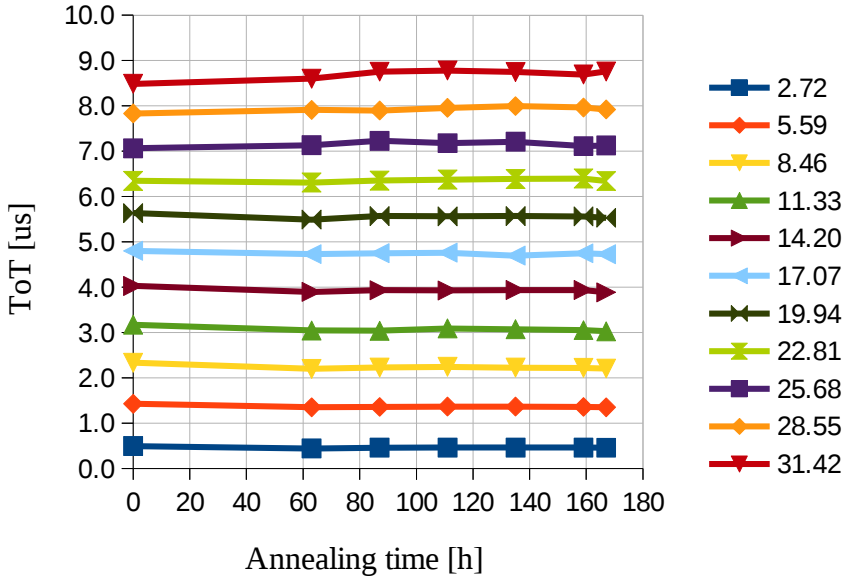
During irradiation



Annealing @ 80 °C



Probably due to effects in the clipping circuit

ToPiX test results

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- At 160MHz can only read and program first ~32 pixels of each column
- At 50MHz (with pre-emphasis disabled) full operation
- S-curve working well (programmable internal test pulse)
- Baseline measurements ok
- On-pixel DACs characterised and correction applied
- Transfer function measurements in good agreement with simulations
- Acquisition system is working (4 boards)
- Tested in beam tests at CERN SPS and Julich COSY facilities
- TID (@X ray-CERN) and SEU (@SIRAD-LNL) tests done

Open issues

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- Clock frequency
- Power consumption
- Radiation tolerance
  - TID effects
  - SEU effects

Full chip estimate

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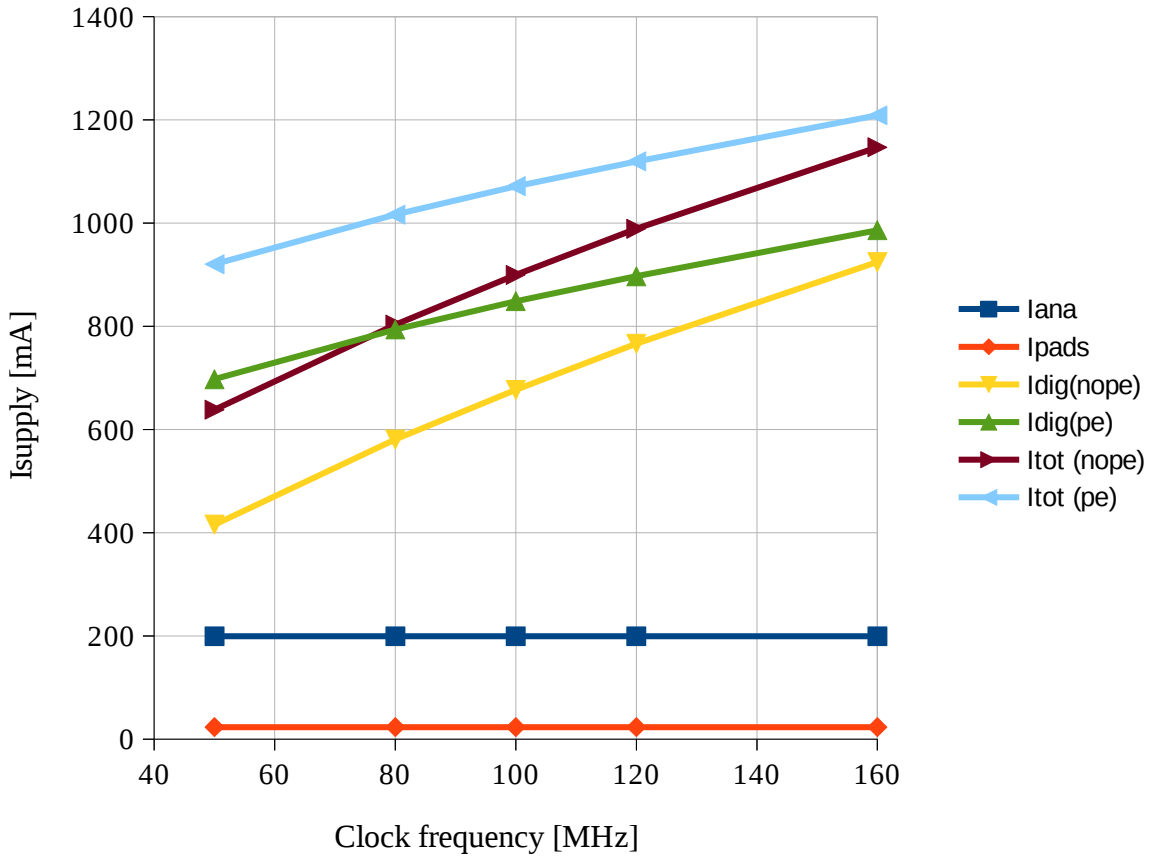

- Very rough estimate
- Still room for improvements (ToPiX v3 not really designed having low power in mind...)
- Time stamp column drivers taken from NA62 GtkTo → room for improvement
- *However, power is dominated by digital logic, therefore it is* $\propto$ *fclock*

GBLD I2C SEU results

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