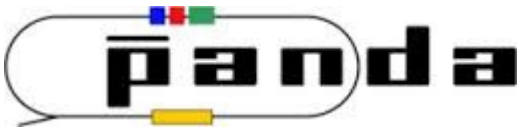
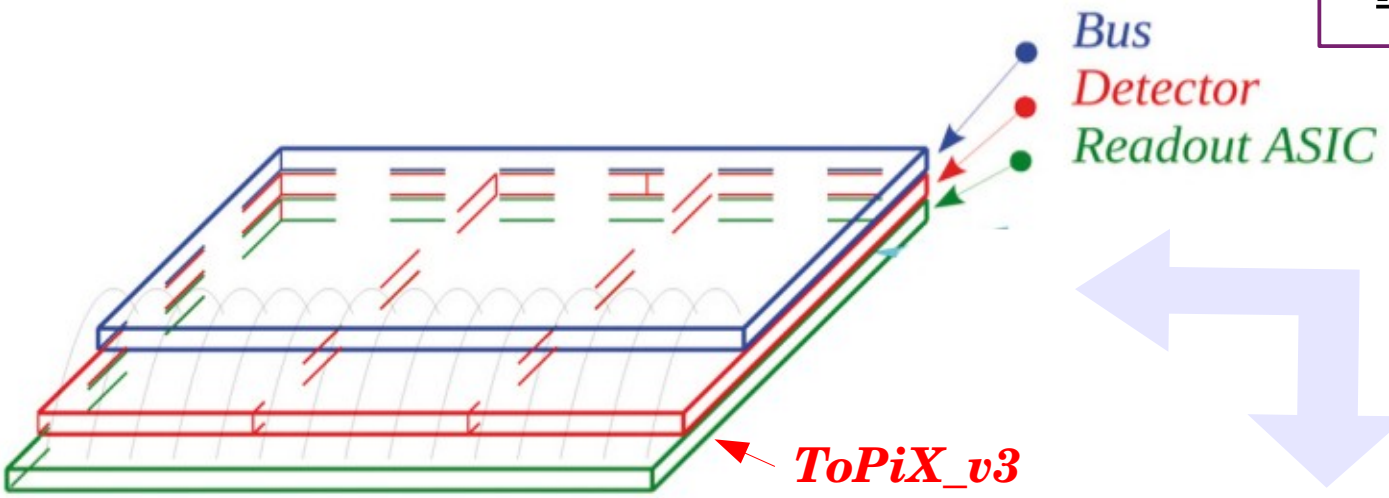
Study of Radiation Effects on Prototypes of the $\bar{P}$ANDA Micro Vertex Detector.

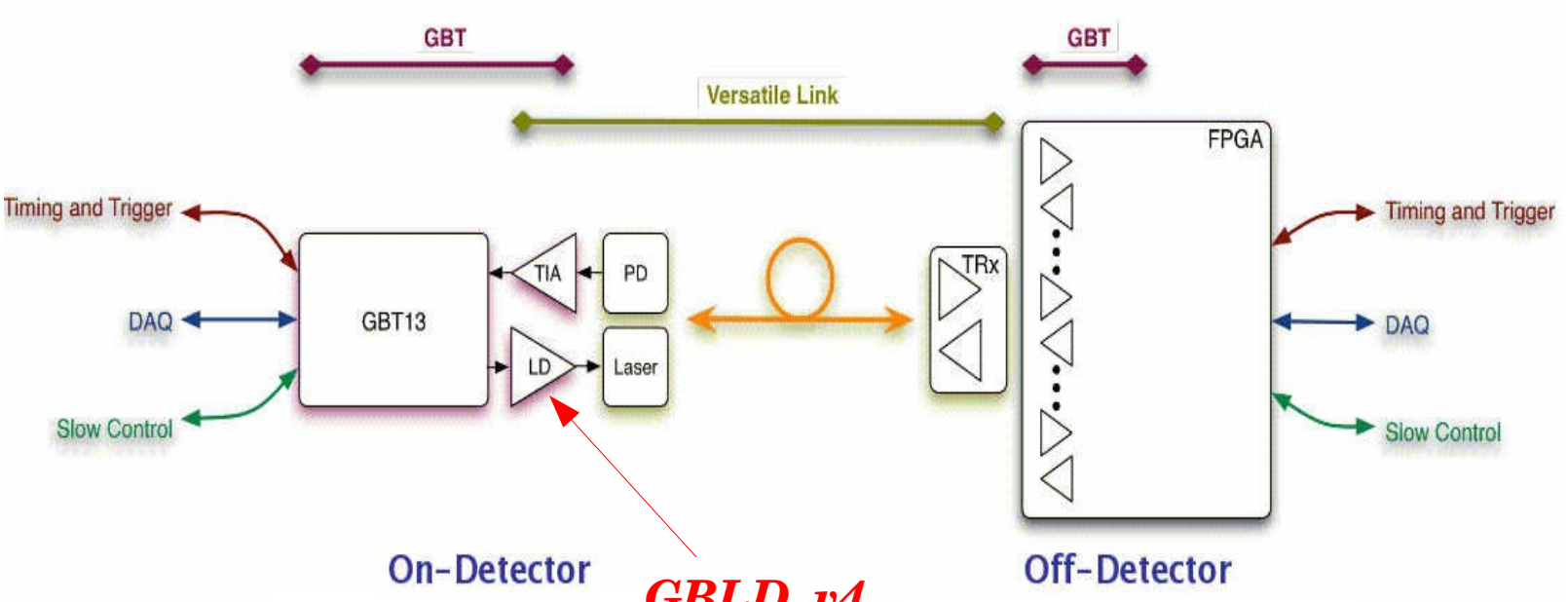
Ilaria Balossino
on behalf of the Turin MVD pixel group



Pixel Readout Scheme

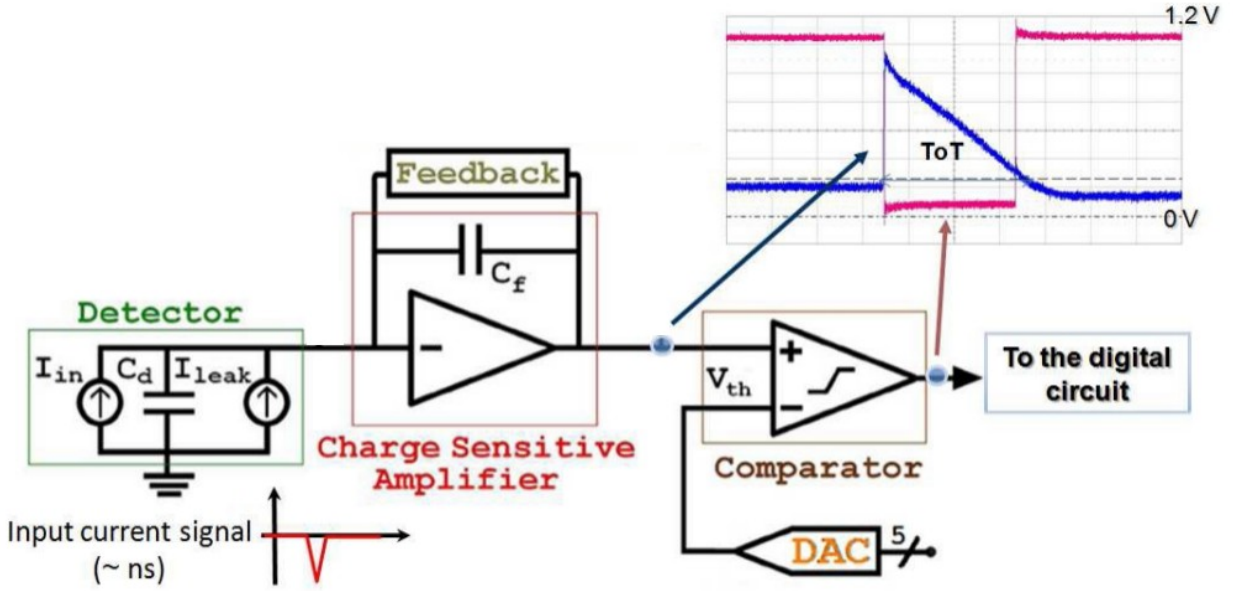


GigaBit Transceiver



GBLD_v4
Laser-Driver ASIC

TOPIX

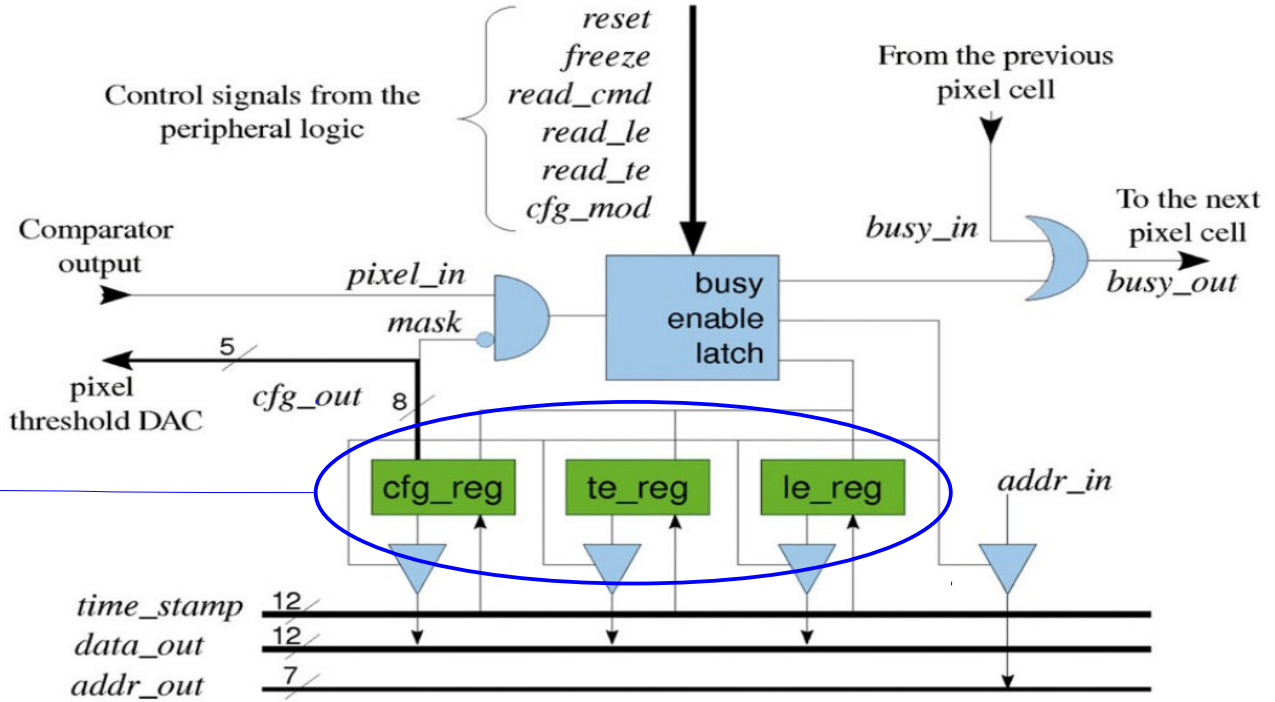


Prototype

5 mm x 4 mm;

pixel cells 100 µm x 100 µm .

Pixel Control Logic



SEU Protection

Triple **M**odular **R**edundancy

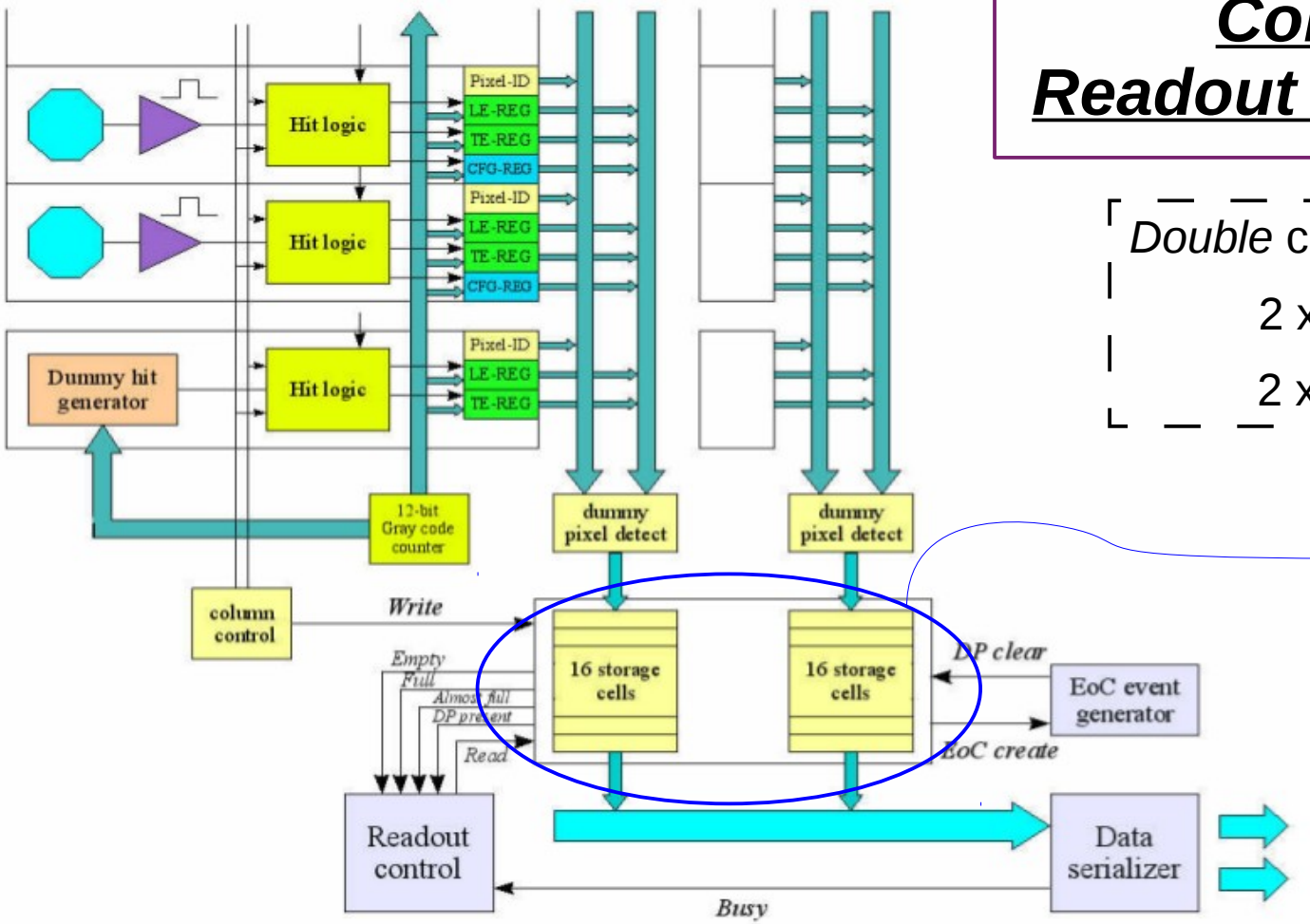
3-latches

Column Readout Schematic

Double columns :

2 x 128 cells;

2 x 32 cells;



SEU Protection

Hamming encoded

D-type Flip Flops

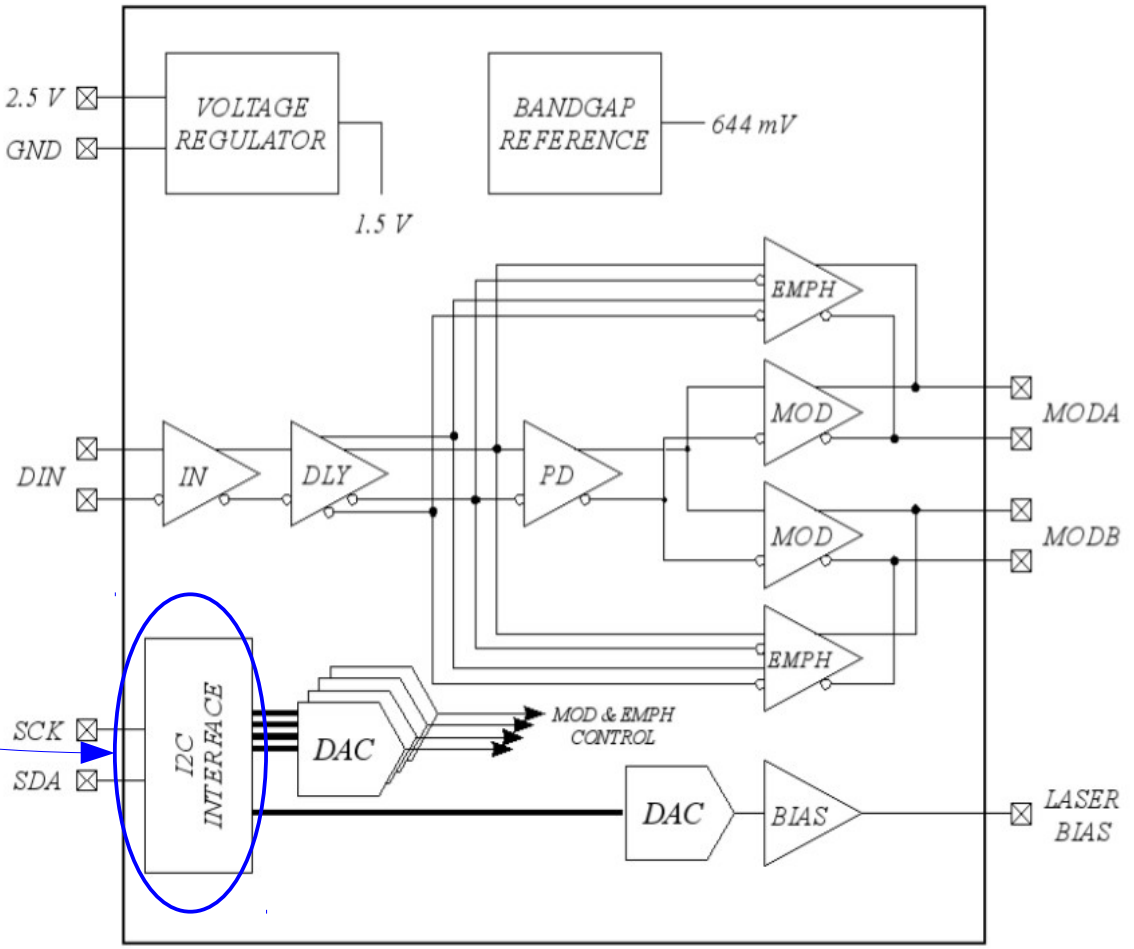
TOPIX

frame header	2	12	8	12	6
	header	chip address	frame counter	not used	ECC
event data 0					
:					
event data i	2	14	12	12	
	header	pixel address	leading edge time	trailing edge time	
:					
event data n					
frame trailer	2	16	16	6	
	header	number of events	CRC	ECC	

GBLD

Laser-Driver ASIC

Bit Rate	5 Gb/s
Power supply	Single, 2.5V
Control interface	I^2C
SEU protection	TMR with self correction

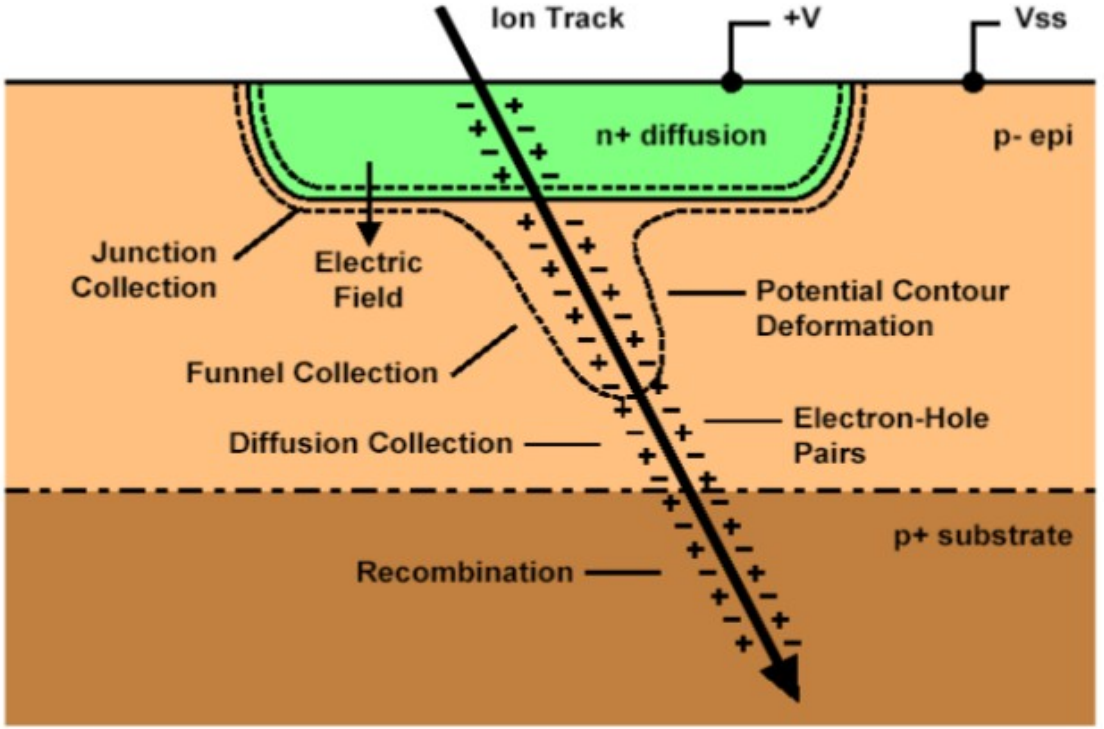


Charge particle

Radiation Damage

Ionization

Single Event Effects



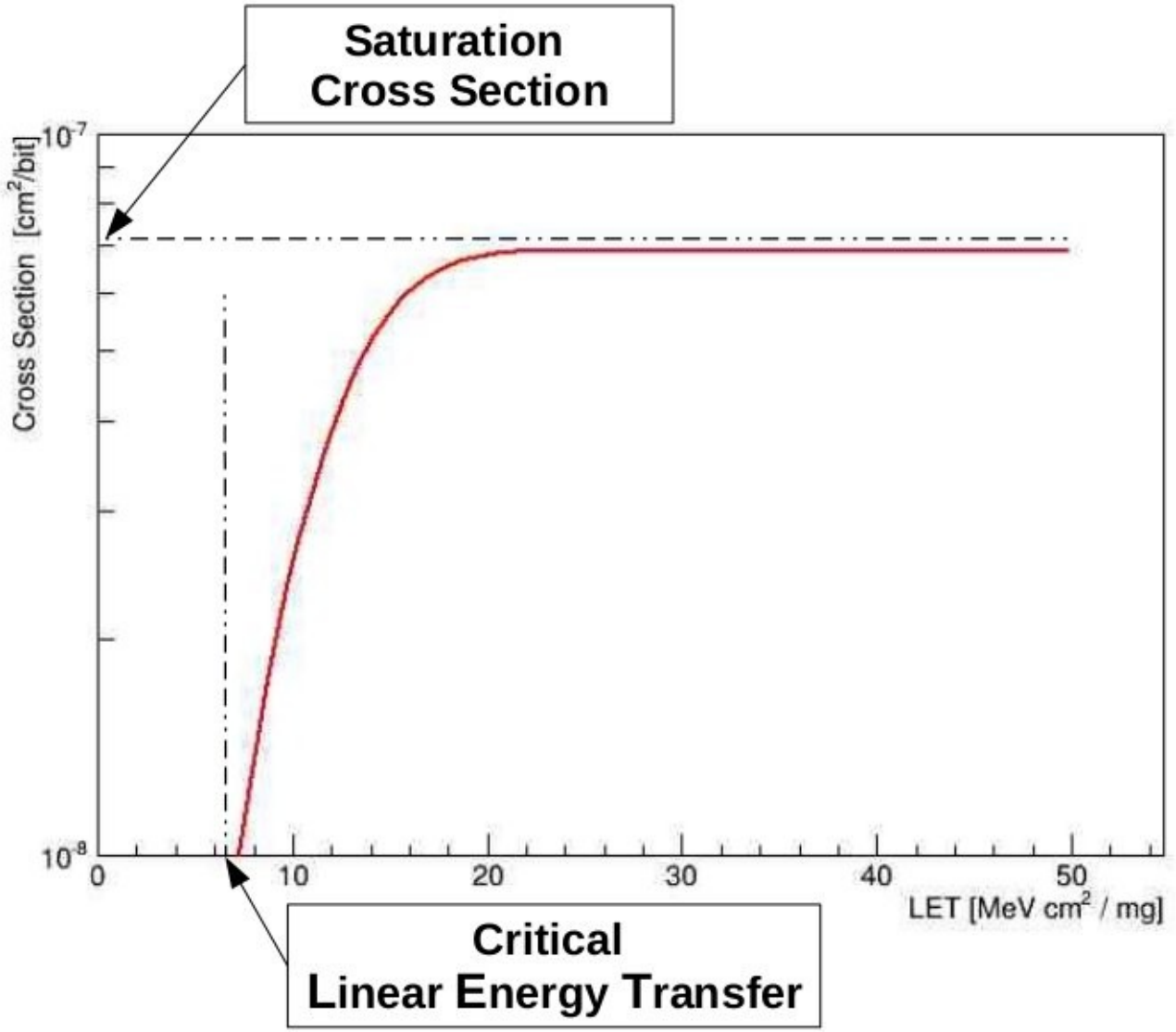
Single Event Upset
change of a state
0 → 1 or viceversa

Single Event Latchup

Single Event Burnout

Single Event Gate Rapture

Weibull Function



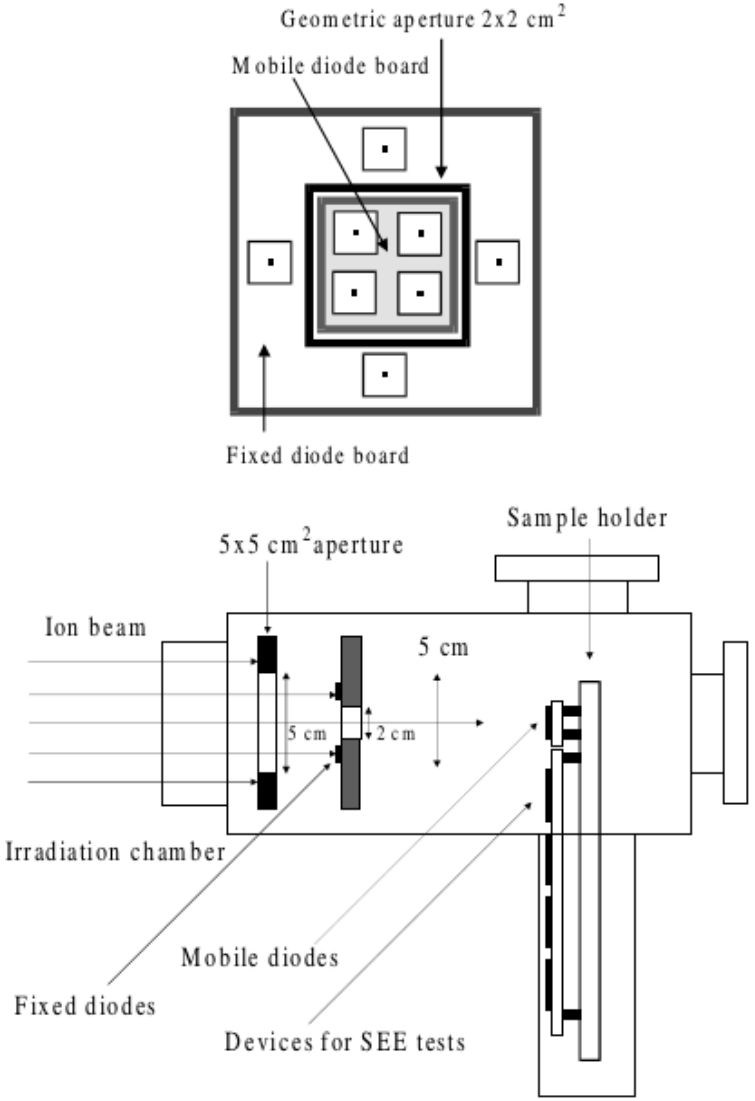
$$\sigma = \frac{N_{SEU}}{N_S \cdot \Phi_{inc}}$$

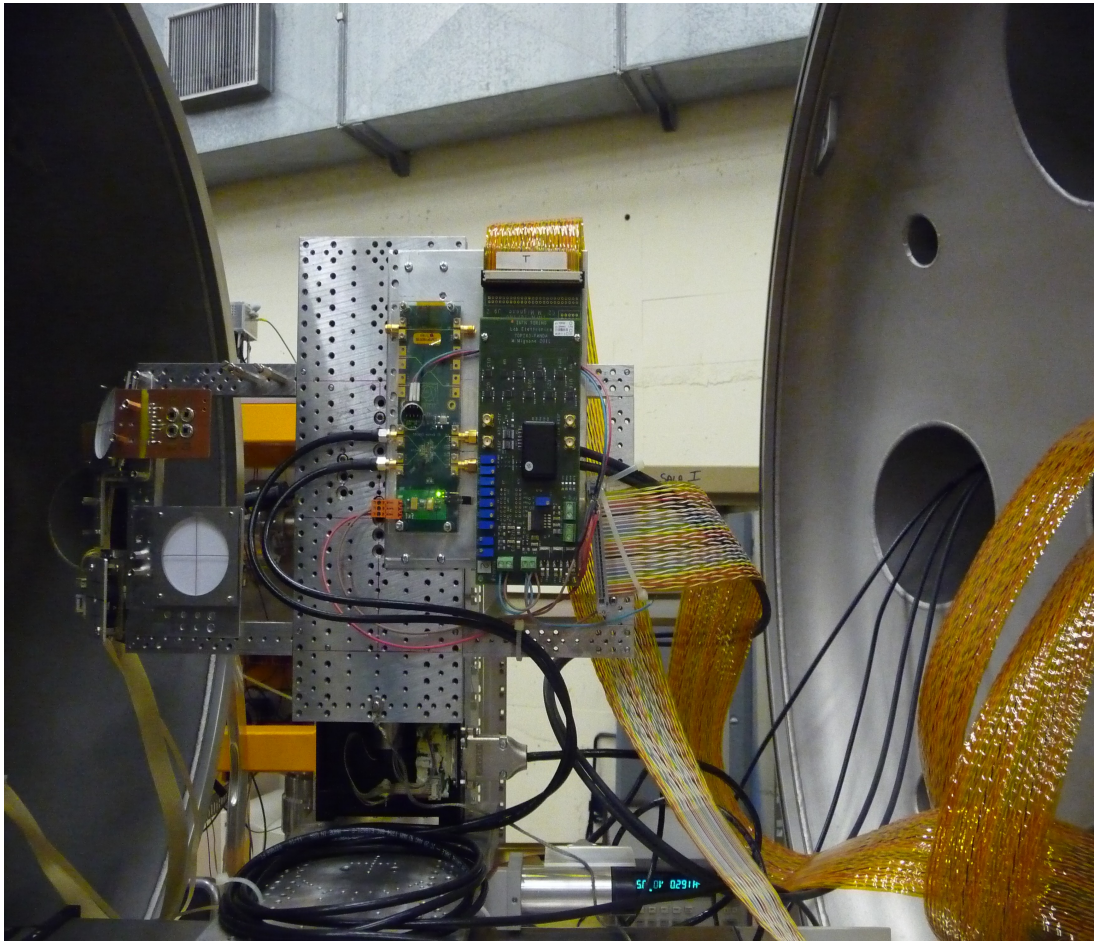
$$\sigma = \sigma_{sat} \cdot \left\{ 1 - e^{-\left\{ \frac{L - L_{th}}{W} \right\}^s} \right\}$$

On-line beam monitoring system

SIRAD irradiation facility

INFN National Laboratory of Legnaro (Padova, Italy)





Test RUN

TOPIX

ION	ENERGY ION [MeV]	ANGLE [°]
Br	264,00	0 20 30
Cl	196,79	0
Cl	159,41	0 20 30
F	110,66	0 20 30
O	100,91	0
Ni	246,00	0
Si	146,41	0 20 30

GBLD

ION	ENERGY ION [MeV]	ANGLE [°]
Br	264,00	0 20 30
Cl	196,79	0
Cl	159,41	0 20 30
F	110,66	0 20 30
Ni	246,00	0
Si	146,41	0 20 30

Dosimetry

Flux

Fluence

External Diodes

Internal Diodes

```
21:05:53        SIRAD Session Manager (RREACT) 0.6.9
21:05:53        Counter logfile
21:05:54        ----------------------------------
21:05:54        Counter log of session:5 topix 042
21:05:54        First access: Time:9:05:54 PM, Date: 11/4/12
21:05:54
21:05:54        Counter started by: root
21:05:54        Flux:   1.8251e+03      1.6601e+03      2.5201e+03      2.8201e+03      1.5051e+03      1.6951e+03      2.1551e+03      2.2201e+03
21:05:55        Flue:   1.4690e+03      1.2730e+03      2.0900e+03      2.3250e+03      1.3870e+03      1.5250e+03      1.6820e+03      1.7200e+03
21:06:00        Flux:   1.4950e+03      1.2000e+03      2.1100e+03      2.4050e+03      1.6000e+03      1.6900e+03      1.7700e+03      1.8350e+03
21:06:00        Flue:   1.0871e+04      9.1170e+03      1.4376e+04      1.6713e+04      9.9630e+03      1.0762e+04      1.2621e+04      1.2467e+04
21:06:05        Flux:   1.9649e+03      1.3499e+03      2.3149e+03      2.8049e+03      1.6349e+03      1.8149e+03      2.1499e+03      2.0649e+03
21:06:05        Flue:   2.0554e+04      1.7072e+04      2.6766e+04      3.1126e+04      1.8922e+04      2.0332e+04      2.3469e+04      2.3549e+04
21:06:10        Flux:   1.7700e+03      1.3750e+03      2.1550e+03      2.5550e+03      1.5200e+03      1.4250e+03      1.9500e+03      1.8600e+03
21:06:10        Flue:   3.1103e+04      2.5669e+04      4.0416e+04      4.7047e+04      2.8266e+04      3.0785e+04      3.5440e+04      3.5422e+04
21:06:16        Flux:   1.8950e+03      1.6100e+03      2.1600e+03      3.1250e+03      1.6850e+03      1.8250e+03      2.2800e+03      2.2850e+03
21:06:16        Flue:   4.1314e+04      3.4086e+04      5.3468e+04      6.2575e+04      3.7620e+04      4.0691e+04      4.7425e+04      4.6864e+04
21:06:21        Flux:   2.1250e+03      1.6650e+03      2.9600e+03      3.2250e+03      1.8350e+03      1.9600e+03      2.3350e+03      2.1300e+03
21:06:21        Flue:   5.1306e+04      4.2406e+04      6.6708e+04      7.8172e+04      4.7004e+04      5.0463e+04      5.9163e+04      5.8557e+04
21:06:26        Flux:   1.9201e+03      1.8051e+03      2.4351e+03      2.9751e+03      1.7751e+03      2.0051e+03      2.3301e+03      2.2951e+03
21:06:26        Flue:   6.1936e+04      5.1109e+04      8.0394e+04      9.4058e+04      5.6656e+04      6.0816e+04      7.1498e+04      7.0672e+04
21:06:32        Flux:   1.6250e+03      1.5100e+03      2.3200e+03      2.7950e+03      1.8600e+03      1.7900e+03      2.0650e+03      2.1250e+03
21:06:32        Flue:   7.1853e+04      5.9532e+04      9.3574e+04      1.0946e+05      6.6100e+04      7.0830e+04      8.3431e+04      8.2133e+04
21:06:37        Flux:   2.0450e+03      1.7800e+03      2.9100e+03      3.2550e+03      1.9400e+03      2.0500e+03      2.3550e+03      2.2700e+03
21:06:37        Flue:   8.2811e+04      6.8775e+04      1.0799e+05      1.2636e+05      7.6084e+04      8.1761e+04      9.6276e+04      9.4613e+04
21:06:42        Flux:   1.8649e+03      1.4899e+03      2.5799e+03      3.0749e+03      1.7749e+03      2.0499e+03      2.1199e+03      2.2499e+03
21:06:42        Flue:   9.2077e+04      7.6540e+04      1.2026e+05      1.4065e+05      8.4584e+04      9.1064e+04      1.0708e+05      1.0520e+05
21:06:48        Flux:   1.9700e+03      1.8450e+03      2.9850e+03      2.9950e+03      2.0300e+03      2.1650e+03      2.1400e+03      2.1850e+03
21:06:48        Flue:   1.0248e+05      8.5317e+04      1.3417e+05      1.5656e+05      9.4355e+04      1.0147e+05      1.1935e+05      1.1707e+05
21:06:53        Flux:   1.9350e+03      1.6750e+03      2.5000e+03      2.9800e+03      1.7050e+03      2.1100e+03      2.2350e+03      2.2950e+03
21:06:53        Flue:   1.1314e+05      9.4411e+04      1.4830e+05      1.7295e+05      1.0423e+05      1.1229e+05      1.3197e+05      1.2931e+05
21:06:58        Flux:   1.9999e+03      1.5999e+03      2.3549e+03      3.1149e+03      1.9099e+03      1.8899e+03      2.3699e+03      2.2899e+03
21:06:58        Flue:   1.2303e+05      1.0271e+05      1.6145e+05      1.8815e+05      1.1352e+05      1.2225e+05      1.4371e+05      1.4079e+05
21:07:04        Flux:   2.0800e+03      1.7250e+03      2.6500e+03      3.1100e+03      1.8600e+03      2.0150e+03      2.4550e+03      2.1400e+03
21:07:04        Flue:   1.3330e+05      1.1121e+05      1.7478e+05      2.0387e+05      1.2281e+05      1.3242e+05      1.5569e+05      1.5240e+05
21:07:09        Flux:   1.7450e+03      1.4850e+03      2.5400e+03      2.7700e+03      1.7400e+03      1.9500e+03      2.1300e+03      2.2550e+03
21:07:09        Flue:   1.4377e+05      1.1987e+05      1.8864e+05      2.1967e+05      1.3245e+05      1.4280e+05      1.6786e+05      1.6427e+05
21:07:14        Flux:   1.9899e+03      1.3699e+03      2.6499e+03      2.7649e+03      1.9799e+03      1.7199e+03      1.9949e+03      2.2249e+03
21:07:14        Flue:   1.5332e+05      1.2795e+05      2.0135e+05      2.3462e+05      1.4144e+05      1.5254e+05      1.7919e+05      1.7548e+05
21:07:20        Flux:   1.8300e+03      1.6500e+03      2.4800e+03      2.8300e+03      1.7800e+03      1.9500e+03      2.4350e+03      2.4650e+03
21:07:20        Flue:   1.6377e+05      1.3680e+05      2.1493e+05      2.5065e+05      1.5124e+05      1.6299e+05      1.9139e+05      1.8754e+05
21:07:25        Flux:   1.9200e+03      1.6850e+03      2.6550e+03      2.9900e+03      1.7350e+03      1.9200e+03      2.3250e+03      2.0700e+03
21:07:25        Flue:   1.7470e+05      1.4570e+05      2.2894e+05      2.6696e+05      1.6115e+05      1.7371e+05      2.0380e+05      1.9969e+05
21:07:30        Flux:   1.9951e+03      1.8451e+03      2.7151e+03      2.9401e+03      1.8451e+03      2.3301e+03      2.5501e+03      2.5401e+03
21:07:30        Flue:   1.8559e+05      1.5463e+05      2.4342e+05      2.8345e+05      1.7093e+05      1.8477e+05      2.1661e+05      2.1191e+05
21:07:36        Flux:   2.0200e+03      1.7300e+03      2.6400e+03      2.9900e+03      1.8950e+03      2.1400e+03      2.4750e+03      2.0550e+03
21:07:36        Flue:   1.9581e+05      1.6332e+05      2.5698e+05      2.9934e+05      1.8062e+05      1.9510e+05      2.2882e+05      2.2373e+05
21:07:41        Flux:   1.8849e+03      1.6049e+03      2.4999e+03      2.7299e+03      1.8999e+03      1.7749e+03      2.1399e+03      2.2799e+03
21:07:41        Flue:   2.0644e+05      1.7226e+05      2.7104e+05      3.1568e+05      1.9053e+05      2.0576e+05      2.4146e+05      2.3609e+05
21:07:43        Counter: counter stopped!
21:07:43        Counter:    elapsed time: 110s
21:07:43        Counter:    estimated central fluence: 244.025000kcts
```

$$FLUENCE = R_{internal} \cdot \cos\left(\vartheta_{incidence}\right) \cdot D_{diodes} \cdot F_{run}$$

$$\frac{\Sigma F_{external\ diodes}}{\Sigma F_{internal\ diodes}}$$

$$F_{stop} - F_{start}$$

TOPIX

```
--------------------------------
Run start
20:07:46.045 02/11/2012
Reference events
00000010001111111110101000101100 0
00000000001111111110101000101100 0
00000001001111111111001000110011 1
00000000001111111110101000101011 0
Clock frequency
50.0
Locked ok
--------------------------------
```

```
--------------------------------
Run end
21:10:45.733 02/11/2012
Measurement cycles
1581
Pixreg errors
13663
SEU counter
47159646
SEU edge counter
3628
FIFO bit errors
30794
Average cycle time
2390.7
--------------------------------
```

Output File

```
Event 8
Time 08:02:39.160 PM 02-Nov-12
Pixreg errors 2
SEU counter 595
SEU edge counter 3
Events 31 32 32 31
Bit errors 0 0 0 0
C0 31
00000010001111111101010001010111 482480 854
...
00000010001111111101010001010111 482481 1738
C1 32
00000000001111111101010001010111 482480 937
...
10111000111100111001111111111111 482481 1826
C2 32
00000001001111111110010001100111 482480 1020
...
11110110111100111001111111111111 482481 1909
C3 31
00000000001111111101010001010101 482480 1103
...
00000000001111111101010001010101 482481 1957
Pixreg 248 10101011 (00111001)
Pixreg 566 11111110 (00111001)
SEU FIFO counter 126
00000000000000000000000000000000000000000000 482480 854
00000000000000000000000000000000000000000000 482480 889
00000000000000000000000000000000000000000000 482480 937
00000000000000000000000000000000000000000000 482480 972
...
00000000000000000000000000000000000000000000 482481 1909
00000000000000000000000000000000000000000000 482481 1957
Event 8 end
```

TOPIX

Output File

$$\sigma_{SEU} = \frac{Pixreg\,errors}{Fluence \cdot 640(celle) \cdot 8(bit)}$$

```
SEU FIFO counter 124
00000000000000000000000000000000000000000 605342 3767
11111111111111111111111111111111000000000 605342 3802
11111111111111111111111111111111111111111 605342 3850
11111111111111111111111111111111111111111 605342 3885
11111111111111111111111111111111111111111 605342 3933
11111111111111111111111111111111111111111 605342 3968
11111111111111111111111111111111111111111 605342 4016
11111111111111111111111111111111111111111 605342 4051
00000000000000000000000000000000111111111 605342 3
00000000000000000000000000000000000000000 605343 38
00000000000000000000000000000000000000000 605343 86
00000000000000000000000000000000000000000 605343 121
00000000000000000000000000000000000000000 605343 169
00000000000000000000000000000000000000000 605343 204
00000000000000000000000000000000000000000 605343 252
00000000000000000000000000000000000000000 605343 287
00000000000000000000000000000000000000000 605343 335
00000000000000000000000000000000000000000 605343 370
00000000000000000000000000000000000000000 605343 418
00000000000000000000000000000000000000000 605343 453
```

```
--------------------------------
Run end
21:10:45.733 02/11/2012
Measurement cycles
1981
Pixreg errors
13663
SEU counter
47159646
SEU edge counter
3628
FIFO bit errors
30794
Average cycle time
2390.7
--------------------------------
```

$$\sigma_{SEU} = \frac{FIFO\,errors}{Fluence \cdot 32(celle) \cdot 38(bit) \cdot 4(colonne)}$$

GBLD

```
Log start 12:51 05/11/2012
Registers written: 10000100 00011111 10101010 10101010 10101010 10101010 00000101
--------------------------------------------------
Error 12:52 05/11/2012
Registers read: 10000100 00011111 10101010 10101010 00101010 10101010 00000101
Error 12:55 05/11/2012
Registers read: 00000000 00000000 00000000 00000000 00000000 00000000 00000000
Error 13:11 05/11/2012
Registers read: 11000100 00011111 10101010 10101010 10101010 10101010 00000101
Error 13:12 05/11/2012
Registers read: 10000100 00011111 10101000 10101010 10101010 10101010 00000101
Error 13:19 05/11/2012
Registers read: 10000100 00011111 00101010 10101010 10101010 10101010 00000101
Error 13:24 05/11/2012
Registers read: 10000111 00011111 10101010 10101010 11101010 10101010 00000101
Error 13:25 05/11/2012
Registers read: 10000100 00011111 10101010 10101010 00101010 10101010 00000101
Error 13:25 05/11/2012
Registers read: 10000100 00011111 10101010 00101010 10101010 10101010 00000101
Error 13:30 05/11/2012
Registers read: 10000100 10011111 10101010 10101010 10101010 10101010 00000101
Error 13:30 05/11/2012
Registers read: 10000100 00011111 10111010 10101010 10101010 10101010 00000101
Error 13:38 05/11/2012
Registers read: 00000000 00000000 00000000 00000000 00000000 00000000 00000000
Error 13:38 05/11/2012
Registers read: 10000100 00011111 10101000 10101010 10101010 10101010 00000101
Error 13:40 05/11/2012
Registers read: 10000100 00011111 00101010 10101010 10101010 10101010 00000101
Error 13:41 05/11/2012
Registers read: 10000100 00011111 10101010 10101010 10101010 10100010 00000101
Error 13:43 05/11/2012
Registers read: 10000100 00011111 10101010 10101010 10101010 10101011 00000101
Error 13:45 05/11/2012
Registers read: 10000100 00011111 10101010 00101010 10101010 10101010 00000101
Log end 13:51 05/11/2012
Total errors 16
```

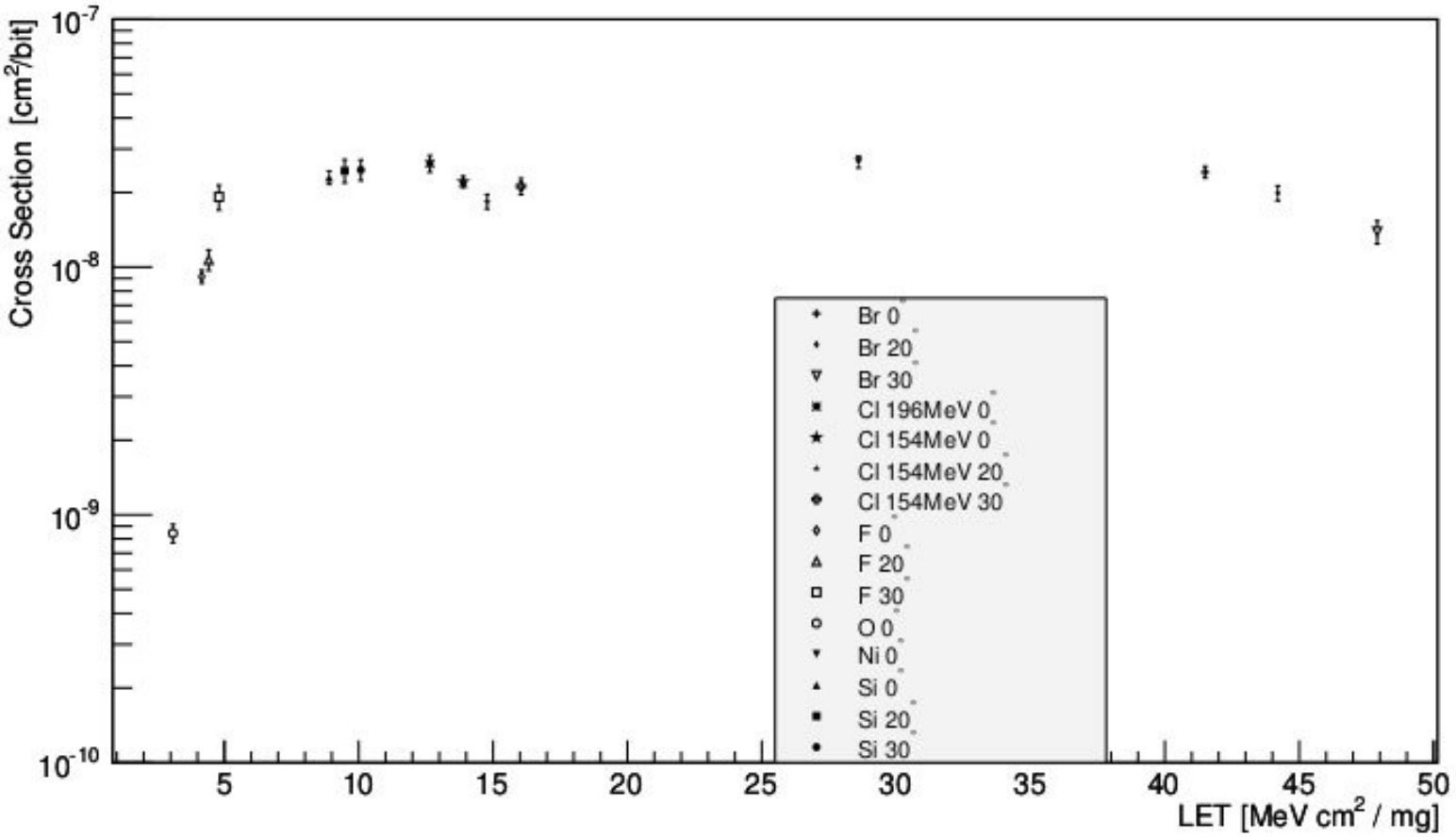
$$\sigma_{SEU} = \frac{Total\ errors}{Fluence \cdot 8(bit) \cdot 7(bin)}$$

Output File

Analisys

Configuration Register

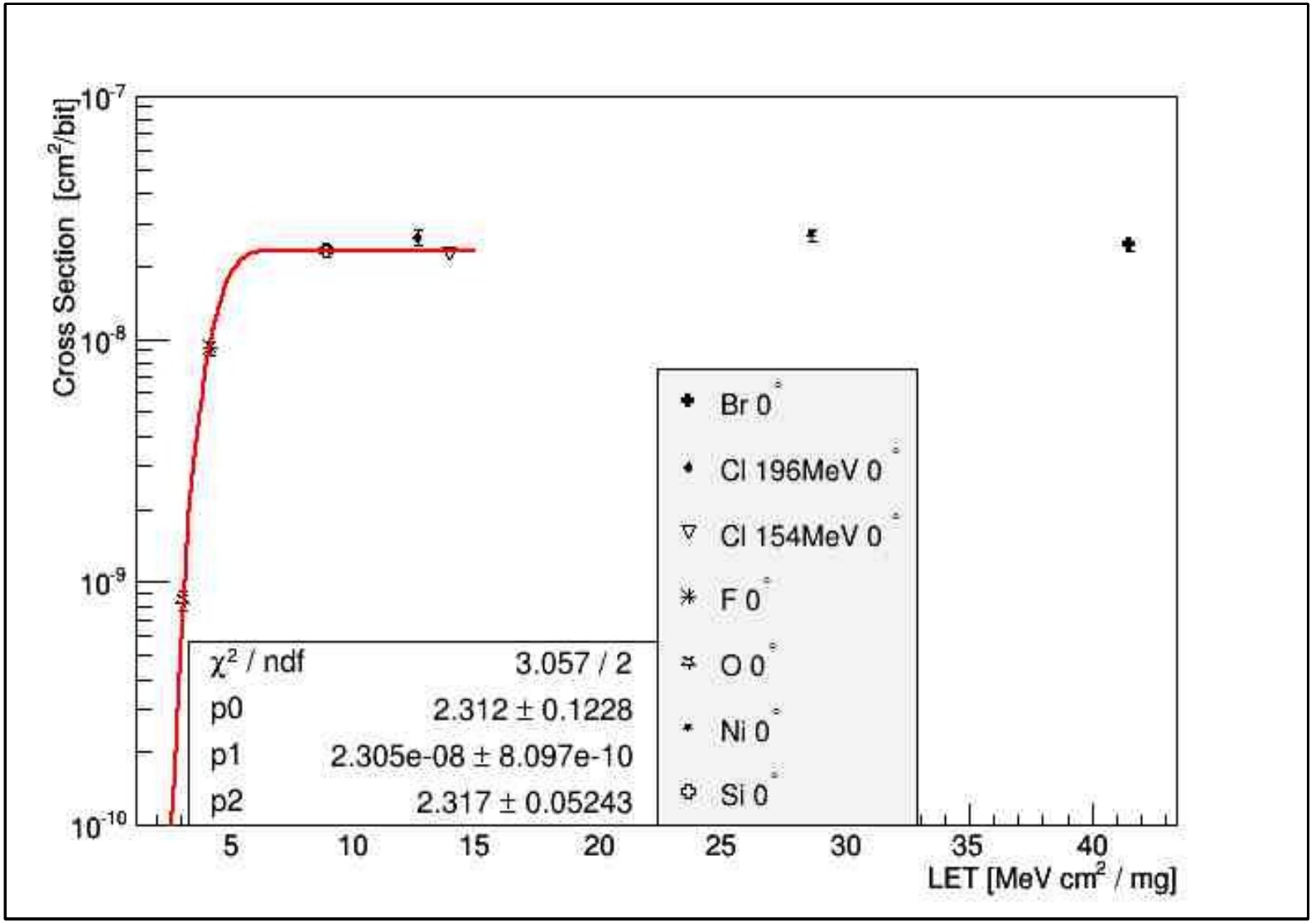
TOPIX



Analisys

Configuration Register

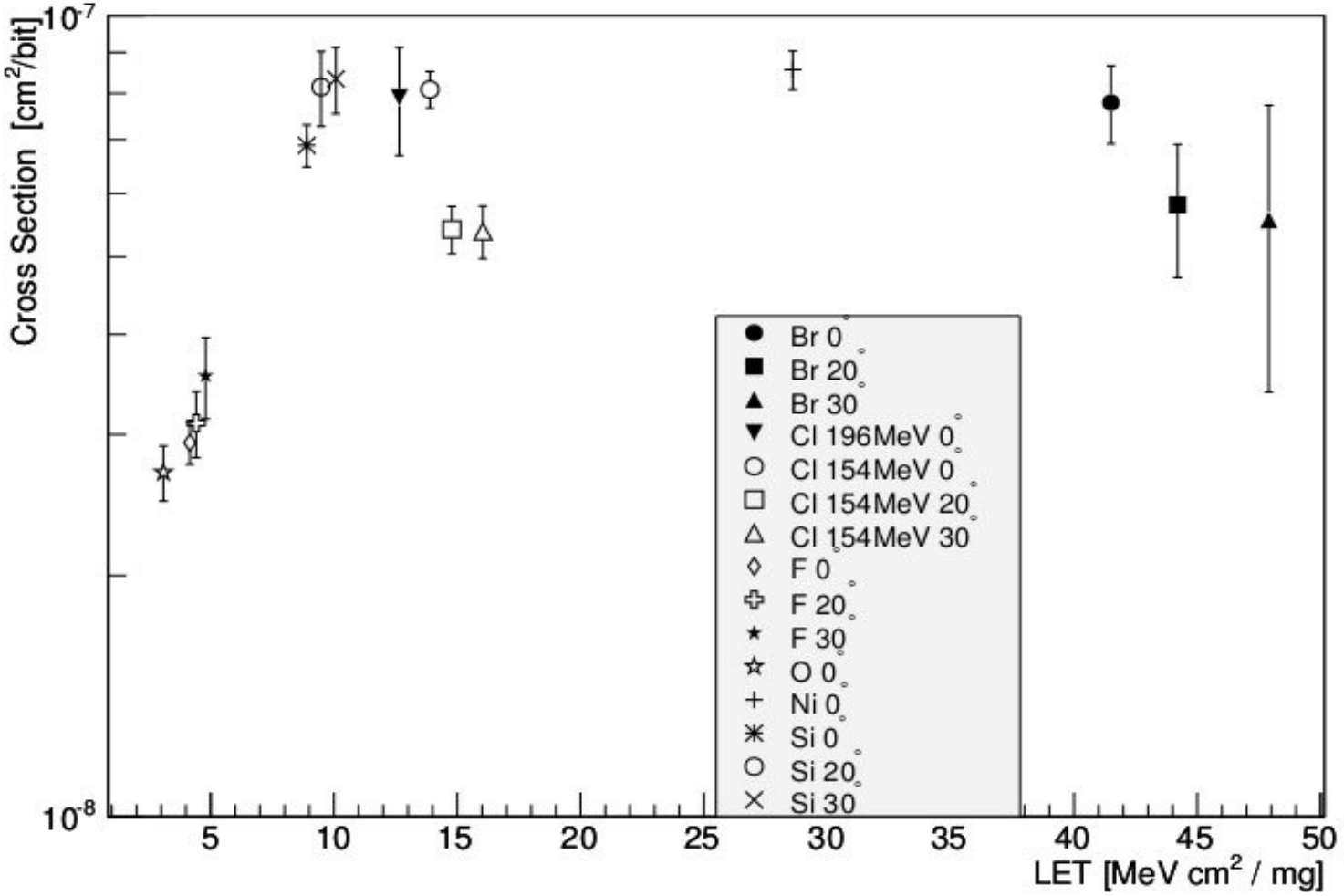
TOPIX



Only 0°. No **Ni, Br.**

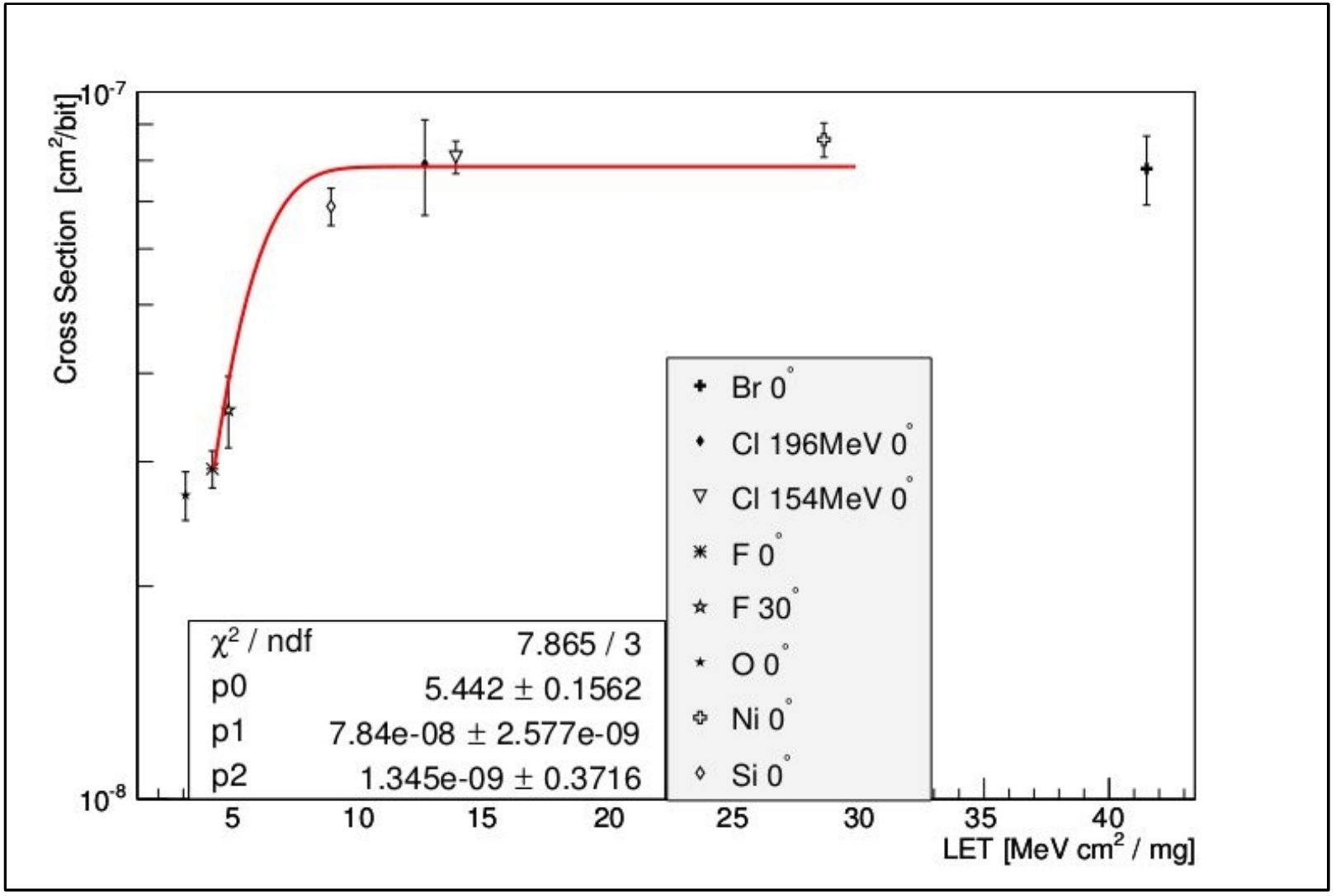
Analisys

Data Register **TOPIX**



Analisys

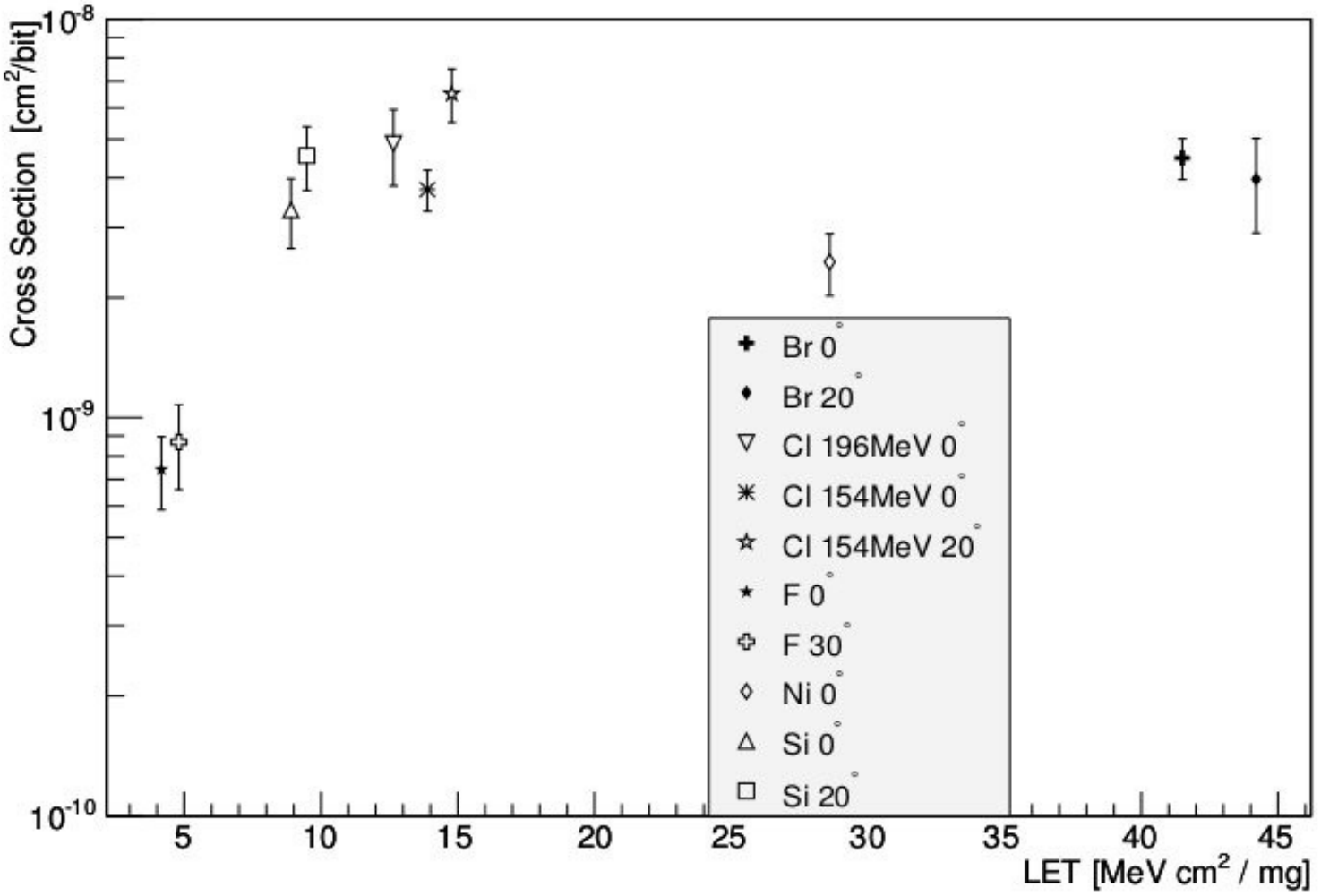
Data Register **TOPIX**



Only 0°, with **F 30°.** No **Br, O.**

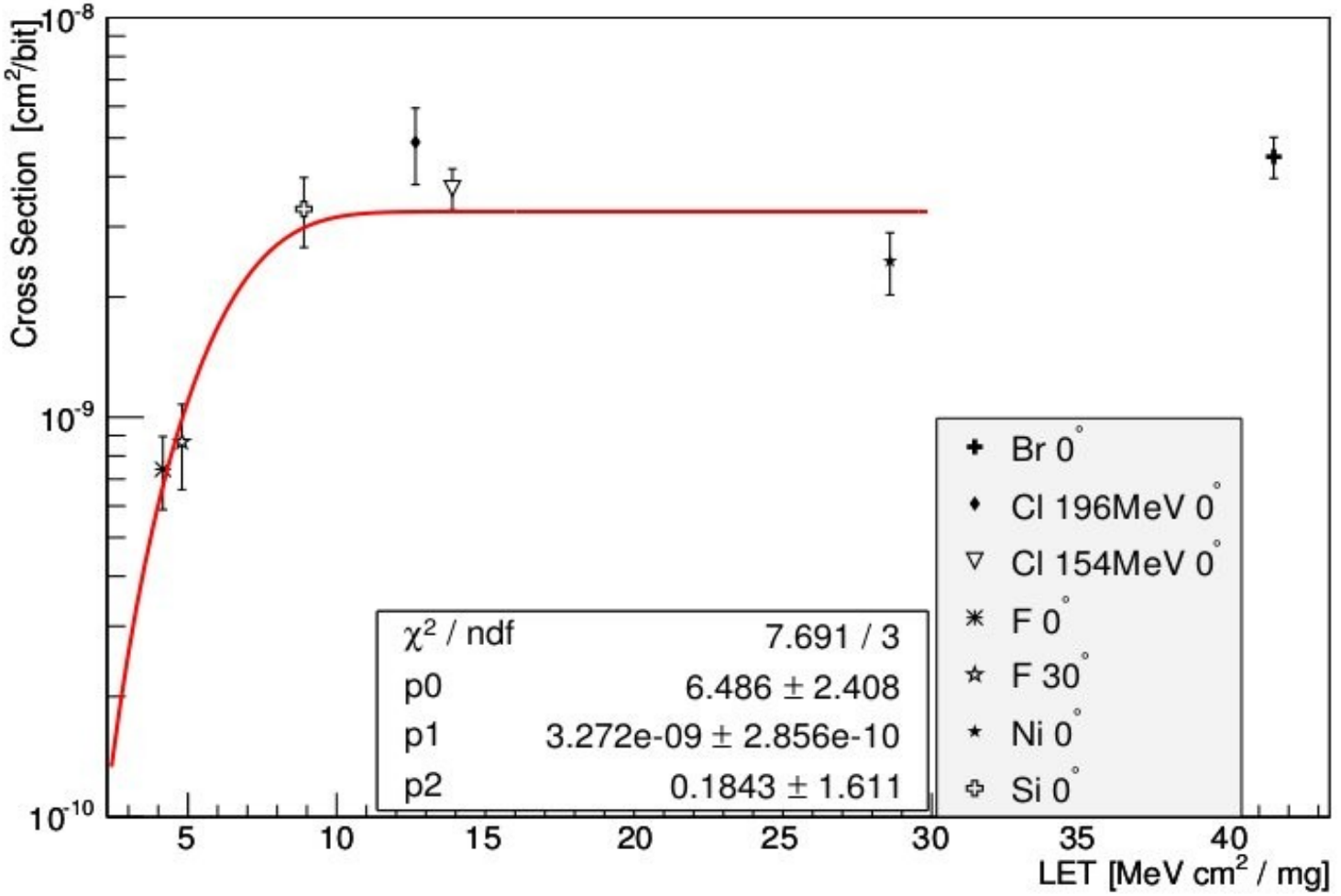
Analisys

I2C Register **GBLD**



Analisys

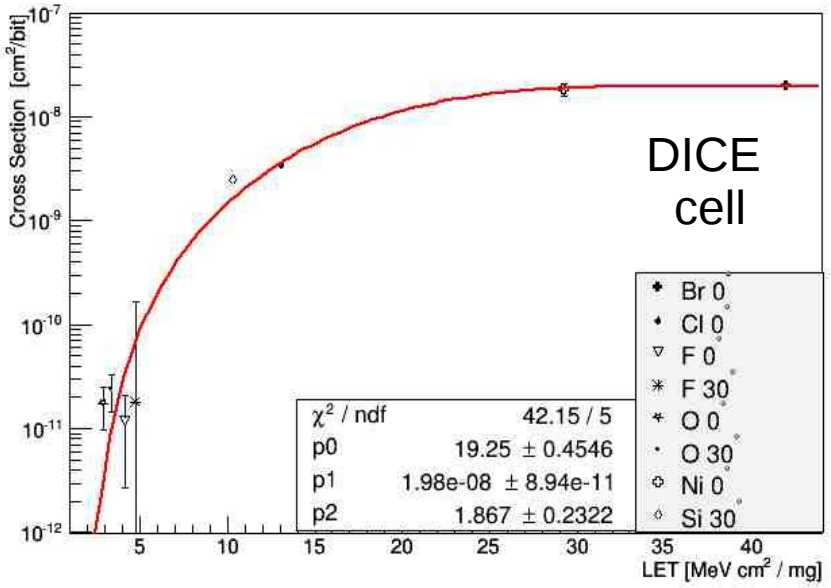
I2C Register **GBLD**



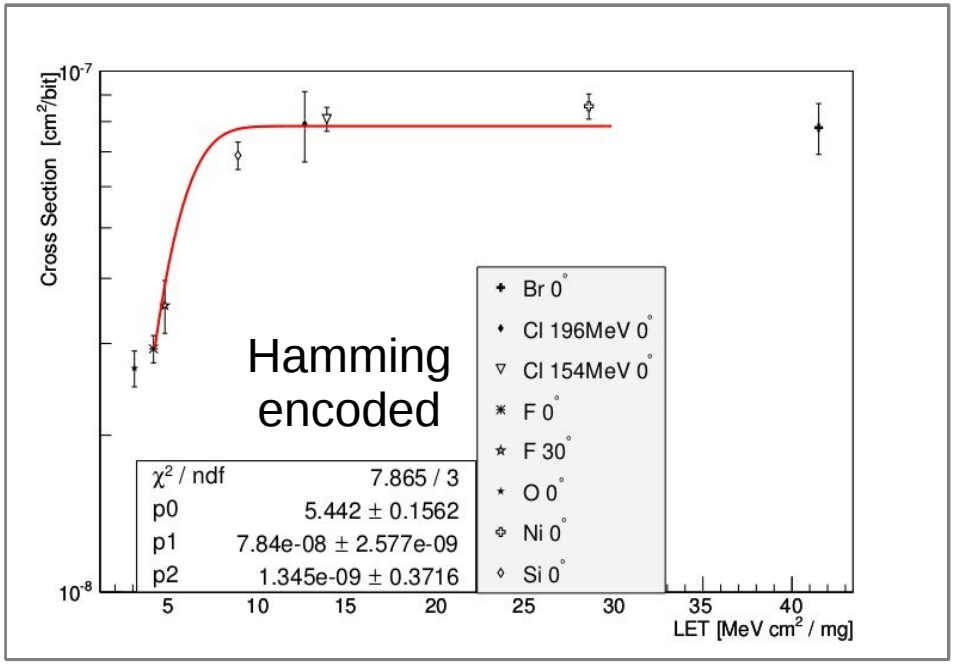
Only 0°, with **F 30°.** No **Br.**

1. **ToPiX_v2; Configuration Register**

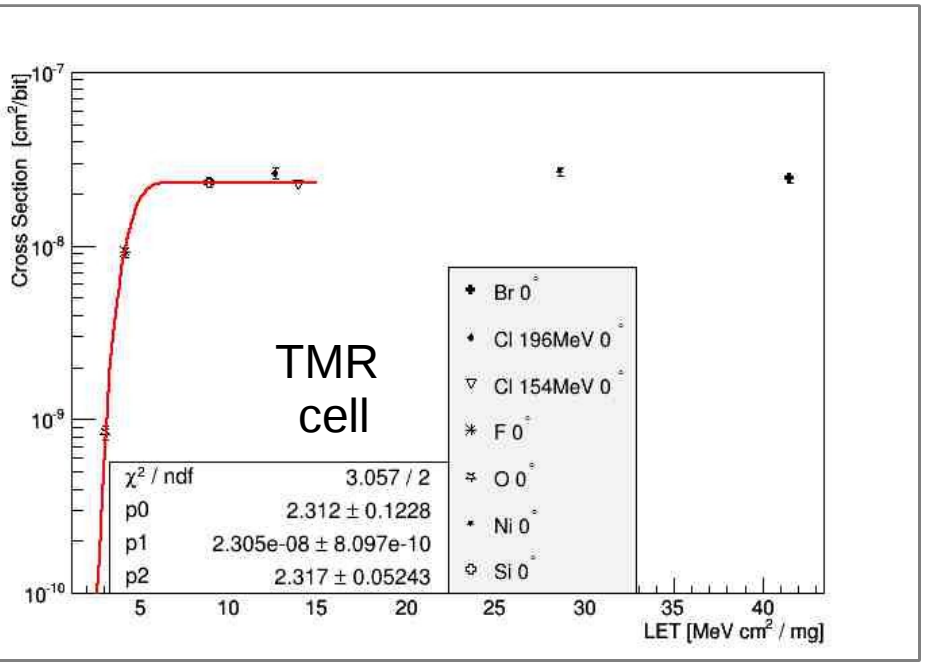
by Laura Zotti



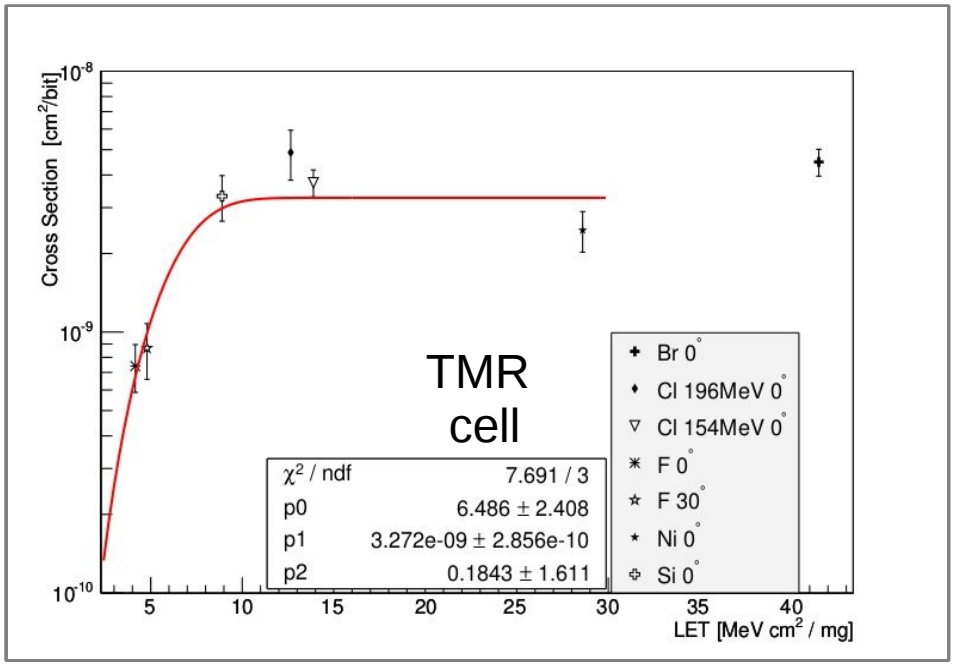
2. **ToPiX_v3; Data Register**



3. **ToPiX_v3; Configuration Register**



4. **GBLD_v4**



Summary

- **ToPiX_v4** *Data Register* : DICE cell;
- **ToPix_v4** *Configuration Register* : study in Triple Modular Redundancy and Hamming encoded with Flip Flop;
- **GBLD_v5** : Triple Modular Redundancy.

Thanks
for your attention!