

# STATUS OF TRBV3 READOUT FOR PANDA-STT

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PANDA Collaboration Meeting December 2013

# Outline

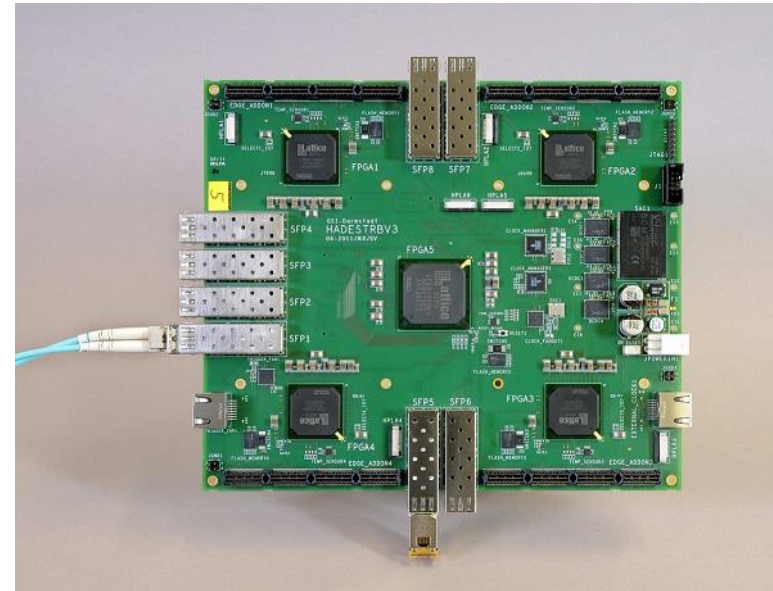


1. TRBv3 platform
2. Cracow ASIC FEE
3. Setup at Juelich
4. Summary

# Trigger Readout Board v3

TRBv3 Community

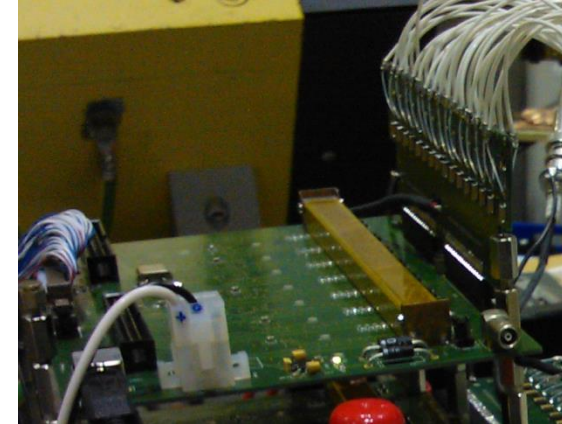
- Standalone measurement board
  - ▣ Central FPGA
    - Integrated trigger system
    - Integrated Slow Control
    - Readout of edge FPGAs
    - Data collection and transmission by GbE
    - Backplane connector for Addon support
  - ▣ Edge FPGA
    - Multichannel, high precision TDC
      - 64 channels + 1 reference (leading edge)
      - Up to 7.2 ps resolution
      - Multihit – 66MHz hitrate
      - 127 hits buffer
      - Reconfigurable – resolution in trade of channels number and edge detection
    - Mezzanine card support and readout
      - ADC front end
      - Additional optical links
      - ...
- Part of a complex system as general purpose board



# Cracow ASIC FEE board

Dominik Przyborowski, AGH in Cracow

- 8x Cracow ASIC
  - ▣ 4x input channels
- 32x LVDS TOT outputs
- 32x analog outputs
- Programmable ASIC settings and thresholds via ATMEGA and USB
- 6V power supply and 0.6A consumption
  
- Exchanged capacitors:
  - ▣ Noise from power supply reduced
  - ▣ Improved baseline holding



# Cracow ASIC FEE Board

Dominik Przyborowski, AGH in Cracow

Architecture Measurements Design of 2<sup>nd</sup> Prototype Su

## Design of 2<sup>nd</sup> Prototype

### Features not implemented in 1<sup>st</sup> prototype

- Lack of DACs for baseline control (high baseline dispersion was expected)
- Longer  $T_P$  (18 ns) in post-layout simulations

### Issues found during tests

- Saturation of preamplifier for large signals
- Analog buffer not adapted for high capacitive load

### Planned improvements

- Implementation of 8 channels
- Redesign of preamp/shaper for higher speed ( $T_P=10$  ns)
- DAC addition and BLH modification for uniform baseline
- Improvement of analog buffer
- Elimination of saturation for large signals

# Cracow ASIC FEE Board

Dominik Przyborowski, AGH in Cracow

Architecture Measurements Design of 2<sup>nd</sup> Prototype Summary

## Summary and plans

### Front-end development status

- 1<sup>st</sup> prototype of STT front-end fully functional
- Variable gain 3 – 24 mV/fC and peaking time  $\sim 20 - 40$  ns work well
- ENC  $\approx 1000$  e<sup>-</sup> for default conditions ( $K_{pre} = 2$  mV/fC,  $T_P = 10$  ns and  $C_{in} = 25$  pF)
- Tail cancellation works and could be trimmed to various types of input signals
- Readout module with 8 ASICs (32 channels) successfully used in test-beam

### Future plans

- New improved front-end design in progress:
  - 8 channels
  - DACs for threshold and baseline settings
  - Faster preamp/shaper
  - Stronger output buffer
  - Better performance for large signals
- Submission of new prototype planned at the end of this year (if funds available)

# The Setup at Juelich

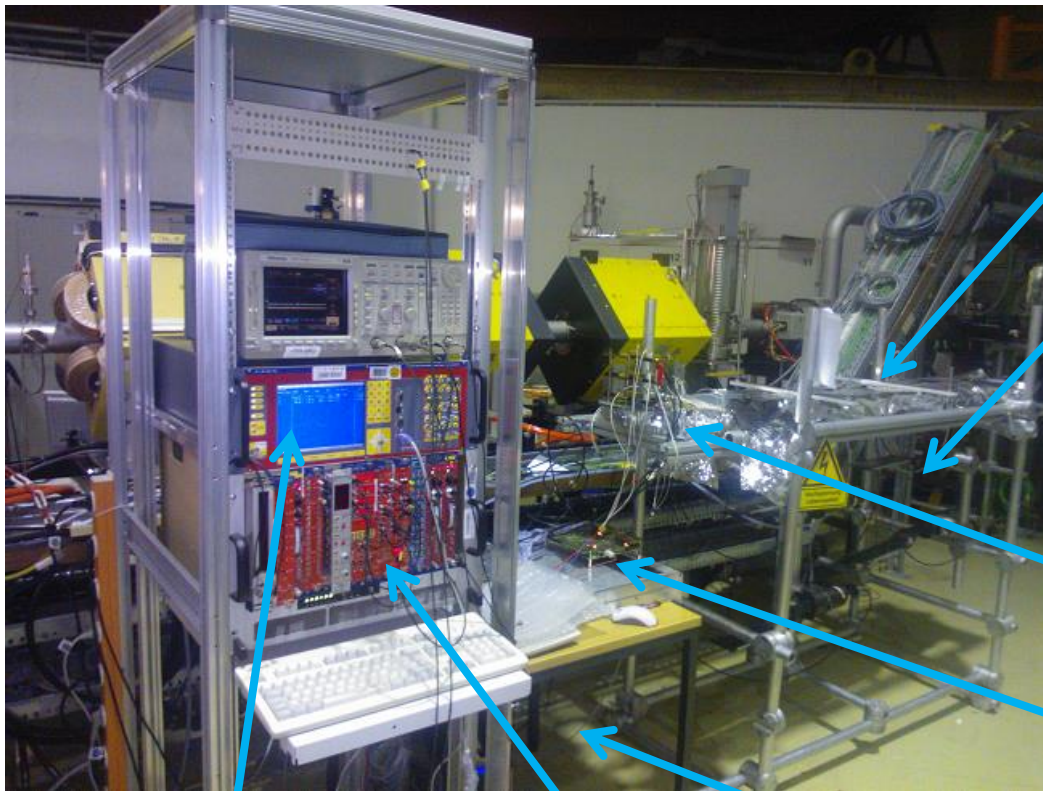
- 8 layers of 24 straws in a row
- 4x scintillators with PMTs for trigger
- Crate with NIM modules
- HV, LV power supplies
- Computers
- Remote access
- A lot of different stuff

From Juelich  
Thanks!

- 
- 3x FEE boards
  - 1x TRBv3
  - A bit of different stuff

From Cracow

# The Setup at Juelich



Straws

PMTs

FEE boards

TRBv3

Power supplies

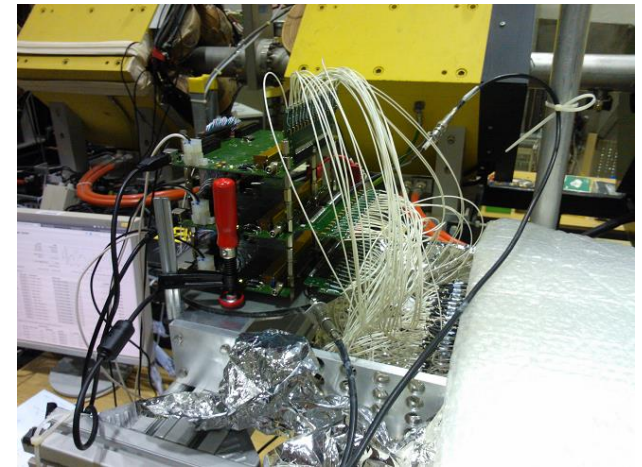
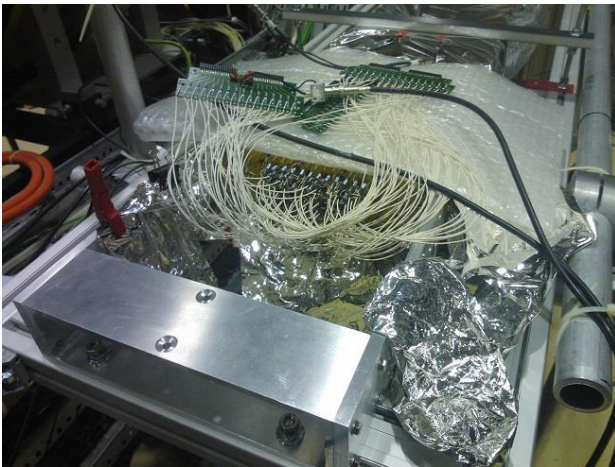
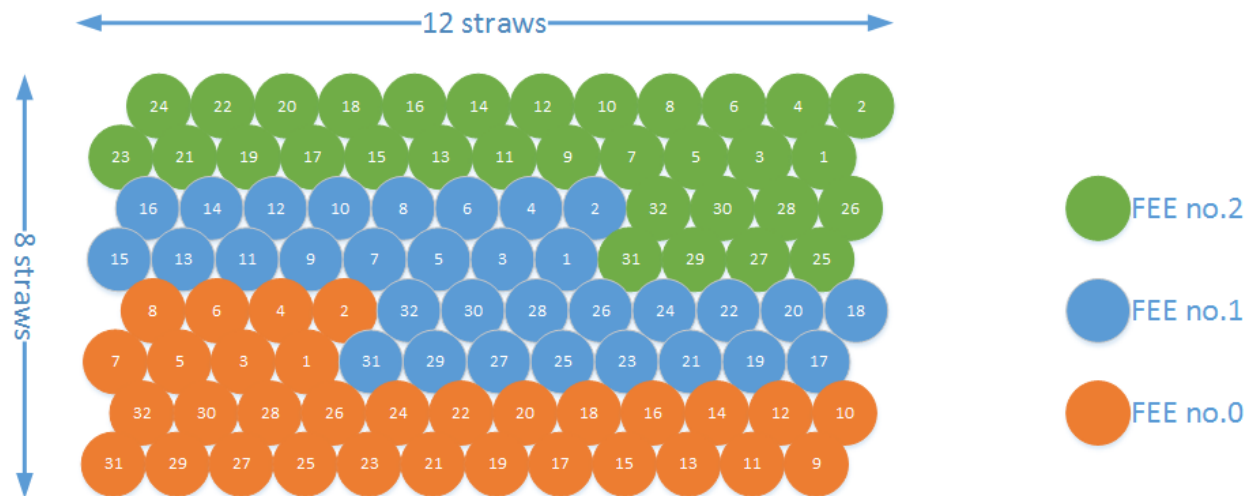
Trigger modules

Control PC



# The Setup at Juelich

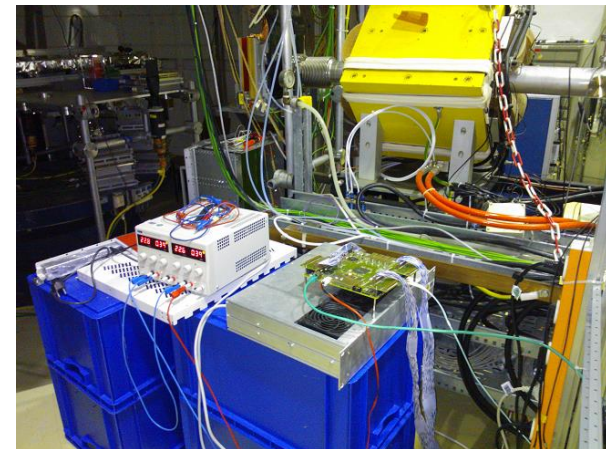
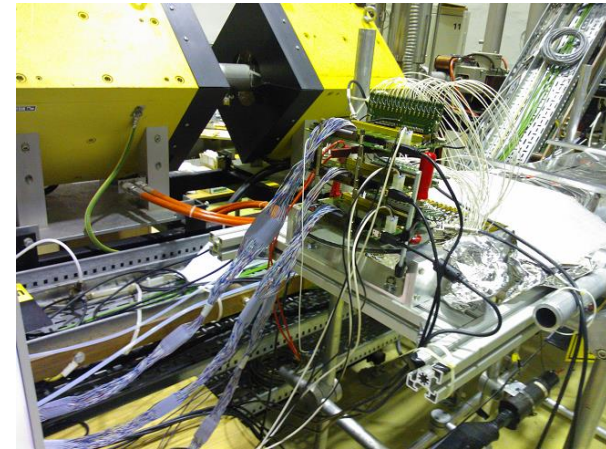
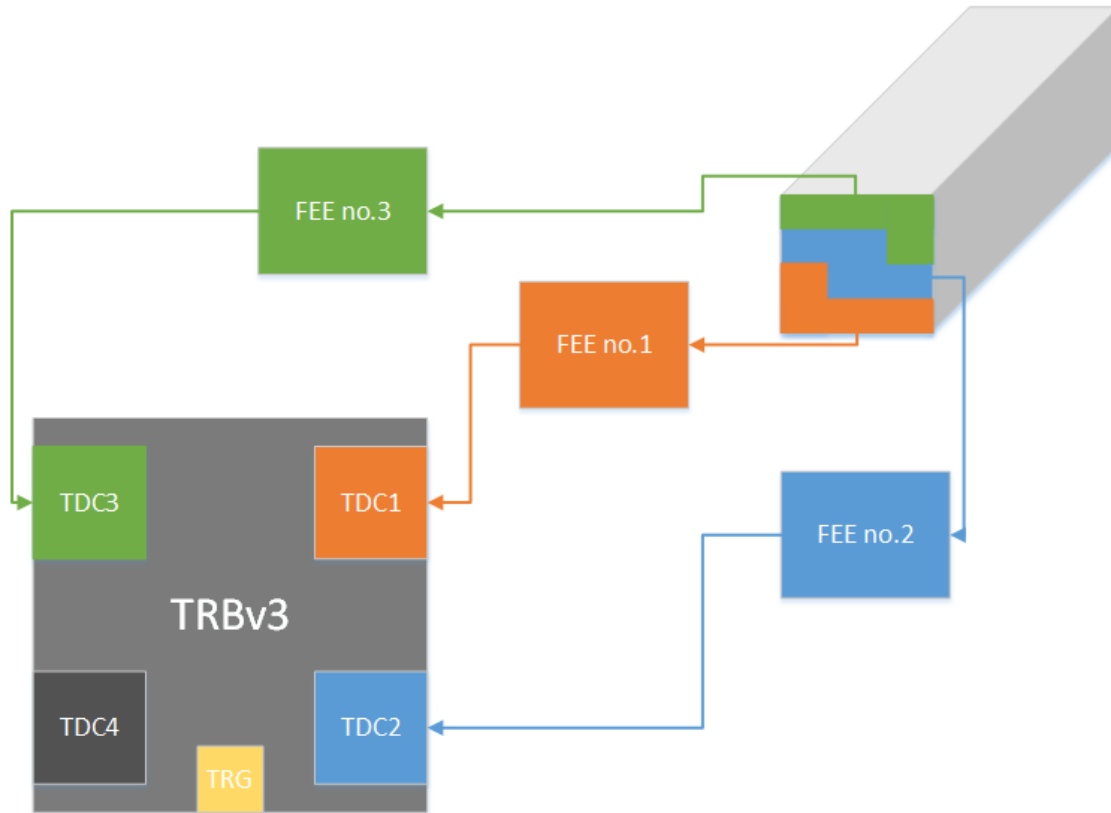
## □ Straws mapping



Thanks to Stephan!

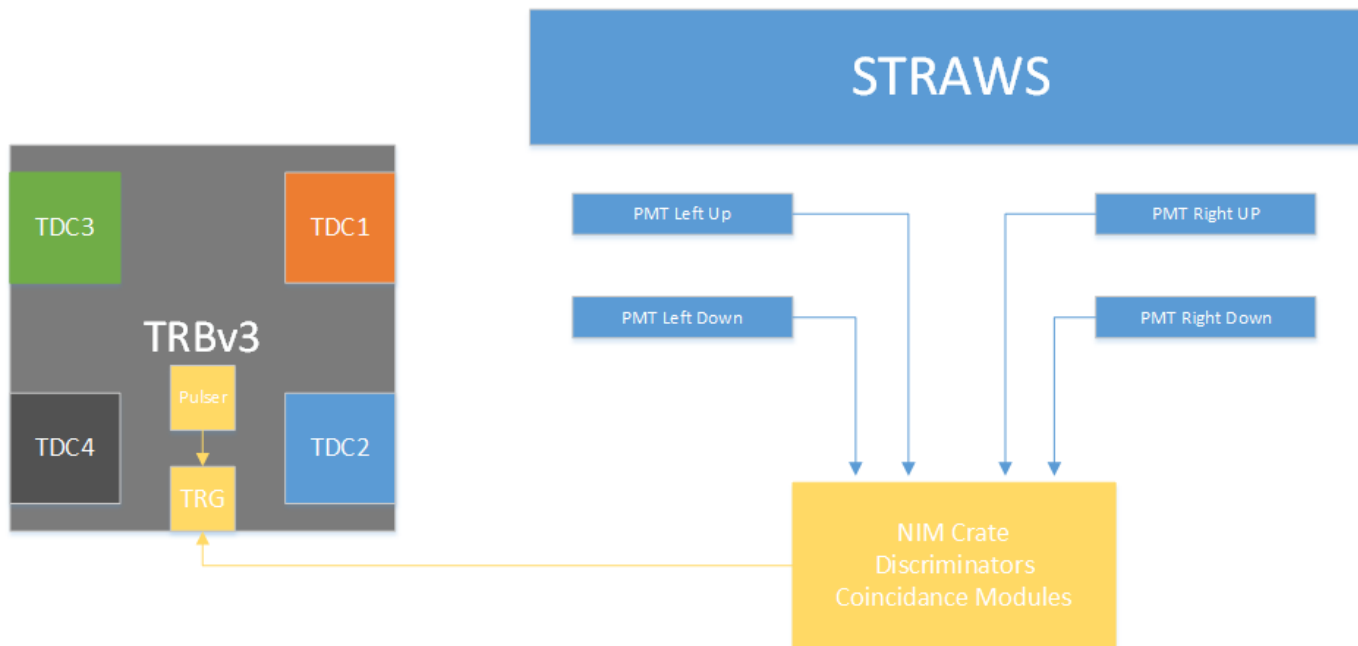
# The Setup at Juelich

## □ FEE boards connection



# The Setup at Juelich

- Triggering:
  - ▣ Internal pulser
  - ▣ Any PMTs configuration
  - ▣ Trigger saved by TDCs as reference channel



# Slow Control and Monitoring

- Startup scripts
- Central Trigger System Integrated on central FPGA
- Gigabit Ethernet connectivity
- Web-based interface
- Real-time monitoring and register status
  - ▣ Trigger rates
  - ▣ Individual TDC channel scalers

quick view status indicators

**Central Trigger System**

**Status overview**

Counter	Counts	Rate
Trigger asserted	875190732 cts...	1240.61 cr/s
Trigger rising edges	875190321 edges	1240.61 Hz
Trigger accepted	874194917 events	1239.92 Hz
Last Idle Time	1499080 ns	
Last Dead Time	1300 ns	789.23 KHz

Throttle:  Limit Trigger Rate to [ 1 ] KHz  
 Full Stop:  ignore all events

Export CTS Configuration:  as TrbCmd script  as shell script

**Trigger Channels**

#	Enable	Trg. Cond.	Assignment	TrbNet Type	Asserted	Edges
0	<input type="checkbox"/>	R. Edge	Ext. Logic - CBM	ext_physks_trigger	335.70 Counts	30.52 KHz
1	<input checked="" type="checkbox"/>	R. Edge	Periodical Pulser 0	ext_physks_trigger	200.00 Counts	200.00 Hz
2	<input type="checkbox"/>	R. Edge	Periodical Pulser 1	ext_physks_trigger	4.95 counts	4.95 Hz
3	<input type="checkbox"/>	R. Edge	Periodical Pulser 2	ext_physks_trigger	0.00 counts	0.00 Hz
4	<input type="checkbox"/>	R. Edge	Periodical Pulser 3	ext_physks_trigger	0.00 counts	0.00 Hz
5	<input checked="" type="checkbox"/>	R. Edge	Random Pulser 0	ext_physks_trigger	1040.78 counts	1040.78 Hz
6	<input type="checkbox"/>	R. Edge	Trigger Input 0	ext_physks_trigger	90.65 Months	306.96 KHz
7	<input type="checkbox"/>	R. Edge	Trigger Input 1	ext_physks_trigger	0.00 counts	0.00 Hz
8	<input type="checkbox"/>	R. Edge	Trigger Input 2	ext_physks_trigger	149.03 counts	125.76 Hz
9	<input type="checkbox"/>	R. Edge	Trigger Input 3	ext_physks_trigger	0.00 counts	0.00 Hz
10	<input type="checkbox"/>	R. Edge	Coincidence Module 0	ext_physks_trigger	100.00 Months	0.00 Hz
11	<input type="checkbox"/>	R. Edge	Coincidence Module 1	ext_physks_trigger	100.00 Months	0.00 Hz
12	<input type="checkbox"/>	R. Edge	Coincidence Module 2	ext_physks_trigger	100.00 Months	0.00 Hz
13	<input type="checkbox"/>	R. Edge	Coincidence Module 3	ext_physks_trigger	100.00 Months	0.00 Hz

**Trigger Input Configuration and Coincidence Detectors**

#	Imp. Rate	Invert	Delay	Input Modules	Spike Rej.	Override	#	Window	Coincidence Detectors	Inhibit Mask (3:0)
0	306.57 KHz	<input type="checkbox"/>	<input type="checkbox"/>	0 ns	0 ns	bypass	0	150 ns	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
1	0.00 Hz	<input type="checkbox"/>	<input type="checkbox"/>	0 ns	0 ns	bypass	1	150 ns	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
2	125.76 Hz	<input type="checkbox"/>	<input type="checkbox"/>	0 ns	0 ns	bypass	2	150 ns	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
3	0.00 Hz	<input type="checkbox"/>	<input type="checkbox"/>	0 ns	0 ns	bypass	3	150 ns	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

**Pulsers**

#	Periodical Pulsers	Random Pulsers	Mean Frequency
0	Low-Period: 200Hz, Frequency: 200.00 cr/s, 0 cr/s	0	1000Hz

Three input formats are supported:  
 1.) Enter the duration of the low-period in clock cycles by omitting a unit  
 2.) Enter the duration of the low-period in seconds by adding "s"  
 3.) Enter the frequency by appending "Hz"

Optional unit prefixes: n, u, m, k, M, G. Example time = 1e-3s, 1 Ms = 1000ns  
 Press enter or leave input to apply values. This might take a few moments and is completed as soon as the left column has changed.

**CTS Details**

Readout config:  Trigger Channel Counter,  Idle/Dead Counter,  Trigger statistics,  Timestamp

TD FSM Limit (debug only):  disabled

RO FSM Limit (debug only):  disabled

Endpoint: 0x7c00  
 Design compiled: Thu, 17 Jan 2013 11:00:39  
 TD FSM State: TD FSM\_IDLE  
 RO FSM State: RO FSM\_IDLE  
 RO Queue: Empty, words enqueued: 0  
 Current Trigger (15.0): 0011 1100 0100 0000, Not asserted  
 Buffered Trigger (10.0): 0011 1100 0100 0010, type: 0x1

all CTS controls are arranged on a single web page. Updates each sec. without reloading the page

context-sensitive state information in direct proximity of controls

when adjusting a module, related information are highlighted (currently editing the pulser's period further down the page)

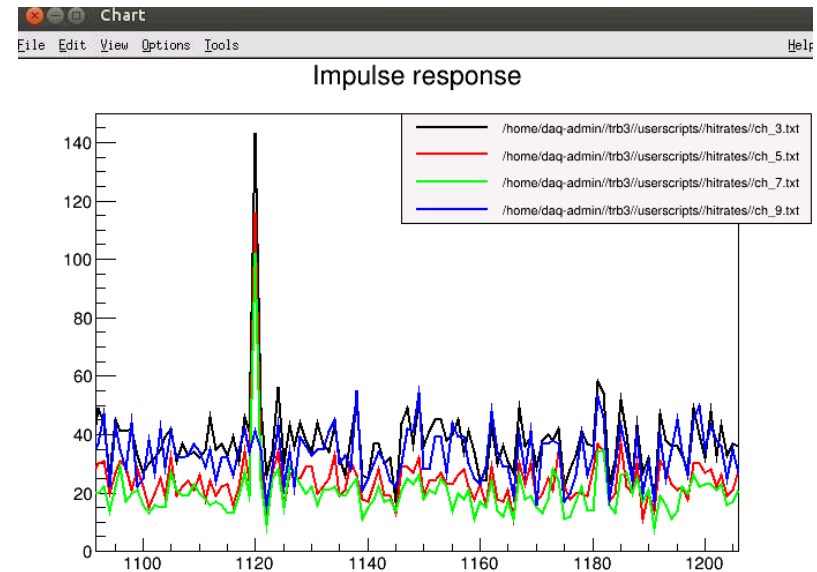
multi-unit support for comfortable user inputs

online help system to assist the user when editing controls

# Slow Control and Monitoring

## □ TDC scalers

Reg	Channel	e100	e101	e102	e103
c000	0	0	0	0	0
c001	1	554	8	0	0
c002	2	554	8	0	0
c003	3	28	17	2	0
c004	4	28	17	2	0
c005	5	18	10	3	0
c006	6	18	10	3	0
c007	7	15	10	6	0
c008	8	15	10	6	0
c009	9	29	7	4	386
c00a	10	29	7	4	386
c00b	11	3	9	11	0
c00c	12	3	9	11	0
c00d	13	38	13	4	0
c00e	14	38	13	4	0
c00f	15	26	15	1	0
c010	16	26	15	1	0
c011	17	51	12	6	0
c012	18	51	12	6	0
c013	19	48	14	5	0
c014	20	48	14	5	0
c015	21	71	9	2	0
c016	22	71	9	2	0
c017	23	84	7	1	0
c018	24	84	7	1	0
c019	25	99	4	1	0
c01a	26	99	4	1	0
c01b	27	91	5	7	0
c01c	28	91	5	7	0
c01d	29	93	0	4	0
c01e	30	93	0	4	0
c01f	31	73	4	3	171707
c020	32	73	4	3	171610
c021	33	63	5	5	0
c022	34	63	5	5	0
c023	35	66	4	6	0
c024	36	66	4	6	0
c025	37	6	3	5	0



- Easy thresholds setup
- Online monitoring of hit rates
  - Noisy channels
  - ASIC configuration loss
- Hit rate logger

# Slow Control and Monitoring

Paweł Strzempek

- ❑ Cracow ASIC FEE controller
  - ❑ USB communication
  - ❑ Multiple boards support
  - ❑ Logging

The screenshot shows the 'Panda FE configurator' window. It features a table for configuring eight ASICs (A through H). Each ASIC row includes a checked/unchecked status, a 'Baseline' value (all set to 1200 mV), and a grid of parameters: 'on/off' (checkbox), 'PreAmp gain' (dropdown, all set to 2), 'PreAmp T' (dropdown, all set to 200), 'Rp' (dropdown, all set to 10), 'Cp' (dropdown, all set to 10), 'Tp' (dropdown, all set to 11), 'Tail cancel.' (dropdown, all set to 'TC\_on'), 'Rt1' (dropdown, all set to 27), 'Ct1' (dropdown, all set to 7,5), 'Rt2' (dropdown, all set to 11), 'Ct2' (dropdown, all set to 1,65), and 'BLH' (checkbox, all set to 'ON').

Below the table is a 'Log' section with a text area containing the following text:

```
echo 0001000001111011100100000000 >/dev/ttyUSB0
echo 0001000110000010110100000000 >/dev/ttyUSB0
echo 0001001010000000010000000000 >/dev/ttyUSB0
echo 0001001110000001010000000000 >/dev/ttyUSB0
echo 0001011101111010110100000000 >/dev/ttyUSB0
```

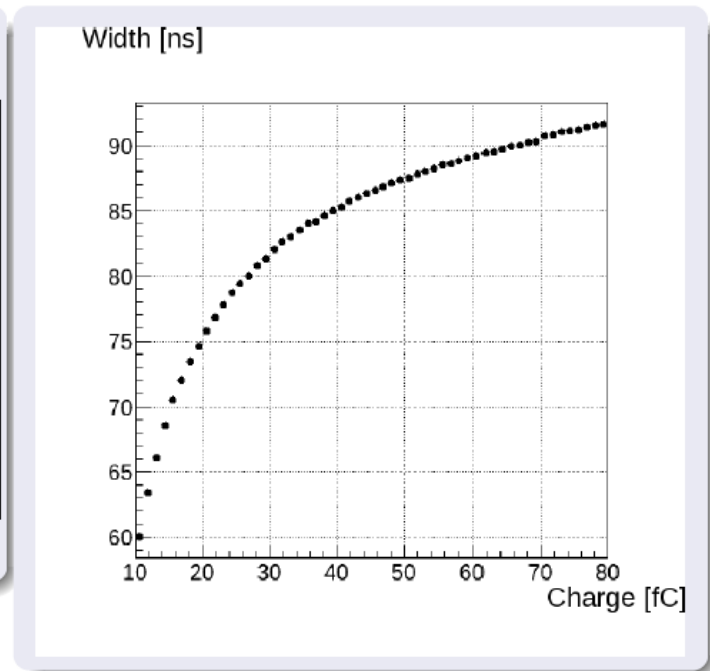
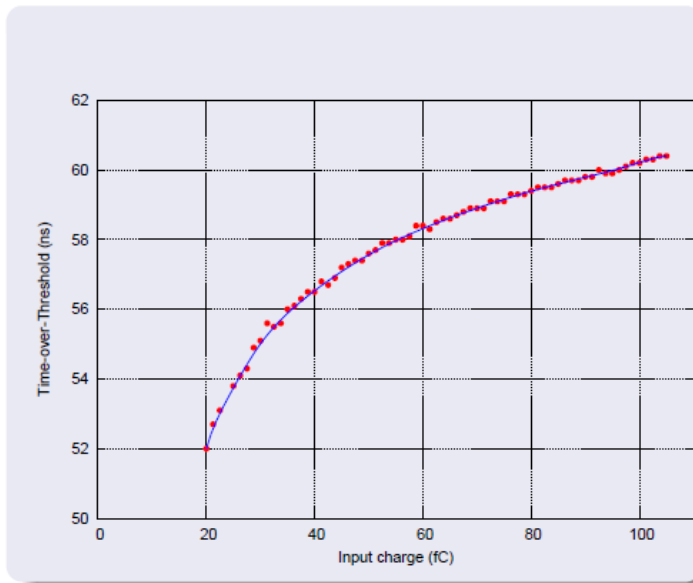
Below the log is a 'Default settings' section with 'Save' and 'Restore' buttons. To the right is a 'Board nr' field with the value '1' and a 'Send!' button. At the bottom right is an 'Exit' button. A 'Settings saved!' message is visible at the bottom left of the log area.

# Summary

- The setup in Juelich is prepared and ready for data taking
- TRBv3 used as standalone TDC platform
- Already some interesting data gathered  
(see the following talk of Jacek)

# Backup

## Measurement results Time-over-Threshold



Results achieved for delta pulse and different FEE settings