STATUS OF TRBV3 READOUT FOR PANDA-STT

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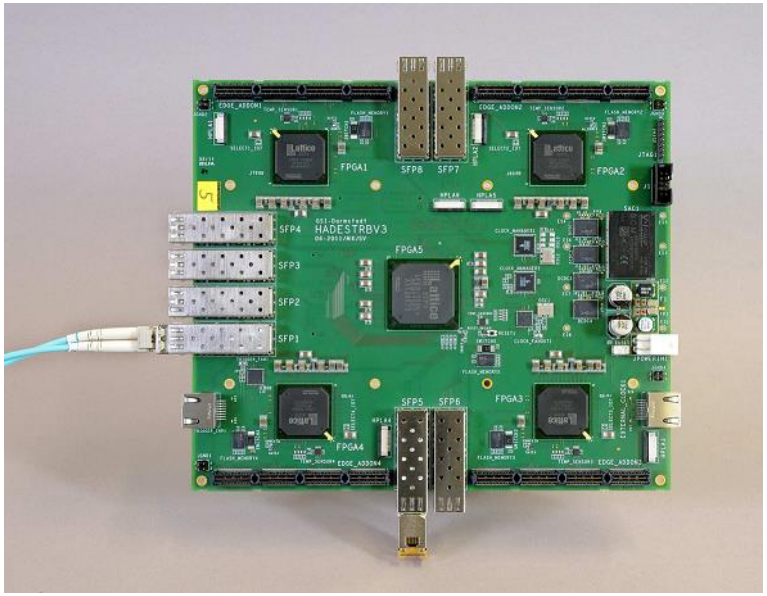
PANDA Collaboration Meeting December 2013

Outline

1. TRBv3 platform
2. Cracow ASIC FEE
3. Setup at Juelich
4. Summary

Trigger Readout Board v3

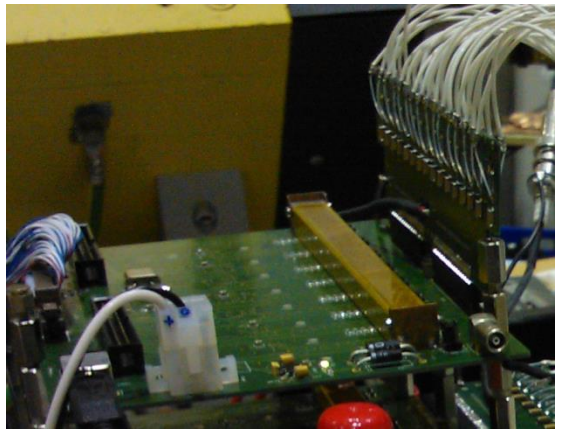


- Standalone measurement board
  - Central FPGA
    - Integrated trigger system
    - Integrated Slow Control
    - Readout of edge FPGAs
    - Data collection and transmission by GbE
    - Backplane connector for Addon support
  - Edge FPGA
    - Multichannel, high precision TDC
      - 64 channels + 1 reference (leading edge)
      - Up to 7.2 ps resolution
      - Multihit – 66MHz hitrate
      - 127 hits buffer
      - Reconfigurable – resolution in trade of channels number and edge detection
    - Mezzanine card support and readout
      - ADC front end
      - Additional optical links
      - …
- Part of a complex system as general purpose board

Cracow ASIC FEE board

Dominik Przyborowski, AGH in Cracow

- 8x Cracow ASIC
  - 4x input channels
- 32x LVDS TOT outputs
- 32x analog outputs
- Programmable ASIC settings and thresholds via ATMEGA and USB
- 6V power supply and 0.6A consumption



- Exchanged capacitors:
  - Noise from power supply reduced
  - Improved baseline holding

Cracow ASIC FEE Board

Design of 2nd Prototype

Features not implemented in 1st prototype

- Lack of DACs for baseline control (high baseline dispersion was expected)
- Longer T_P (18 ns) in post–layout simulations

Issues found during tests

- Saturation of preamplifier for large signals
- Analog buffer not addapted for high capacitive load

Planned improvements

- Implementation of 8 channels
- Redesign of preamp/shaper for higher speed (T_P=10 ns)
- DAC addition and BLH modification for uniform baseline
- Improvement of analog buffer
- Elimination of saturation for large signals

Cracow ASIC FEE Board

Summary and plans

Front–end development status

- 1^{st} prototype of STT front–end fully functional
- Variable gain 3 – 24 mV/fC and peaking time $\sim$ 20 – 40 ns work well
- ENC $\approx$ 1000 e^- for default conditions ($K_{pre} = 2mV/fC$, $T_P = 10ns$ and $C_{in} = 25pF$)
- Tail cancellation works and could be trimmed to various types of input signals
- Readout module with 8 ASICs (32 channels) succesfully used in test-beam

Future plans

- New improved front–end design in progress:
  - 8 channels
  - DACs for threshold and baseline settings
  - Faster preamp/shaper
  - Stronger output buffer
  - Better performance for large signals
- Submission of new prototype planned at the end of this year (if founds available)

The Setup at Juelich

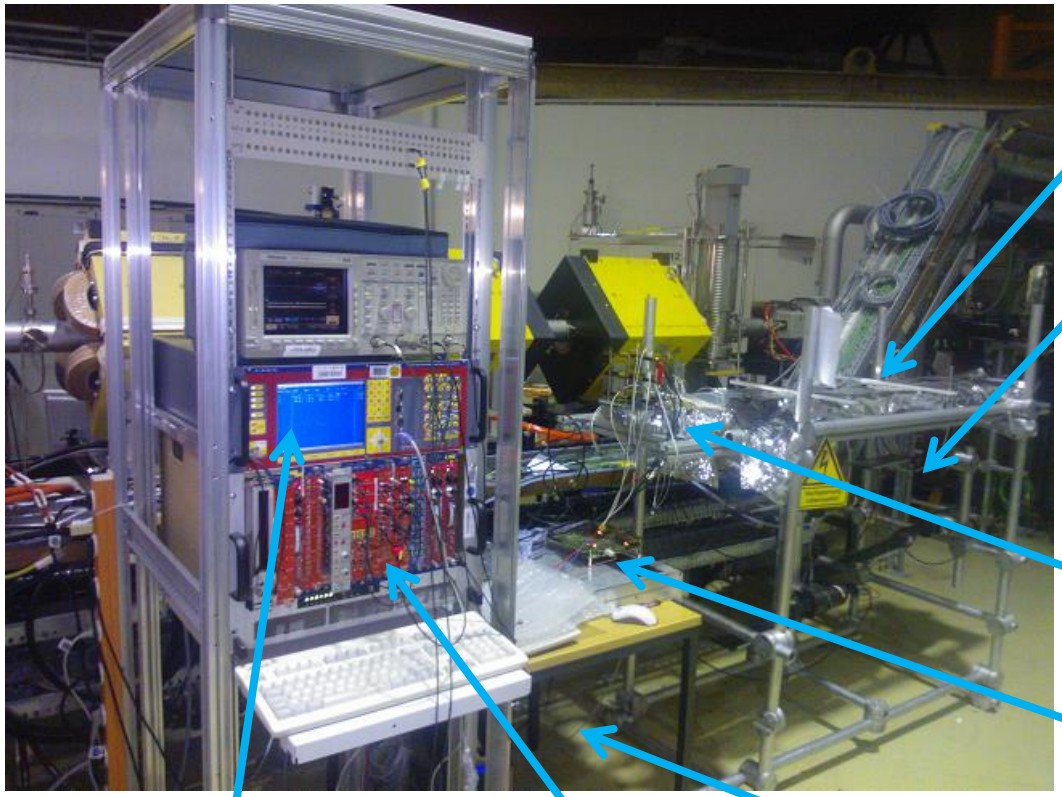
- 8 layers of 24 straws in a row
- 4x scintillators with PMTs for trigger
- Crate with NIM modules
- HV, LV power supplies
- Computers
- Remote access
- A lot of different stuff

From Juelich
Thanks!

- 3x FEE boards
- 1x TRBv3
- A bit of different stuff

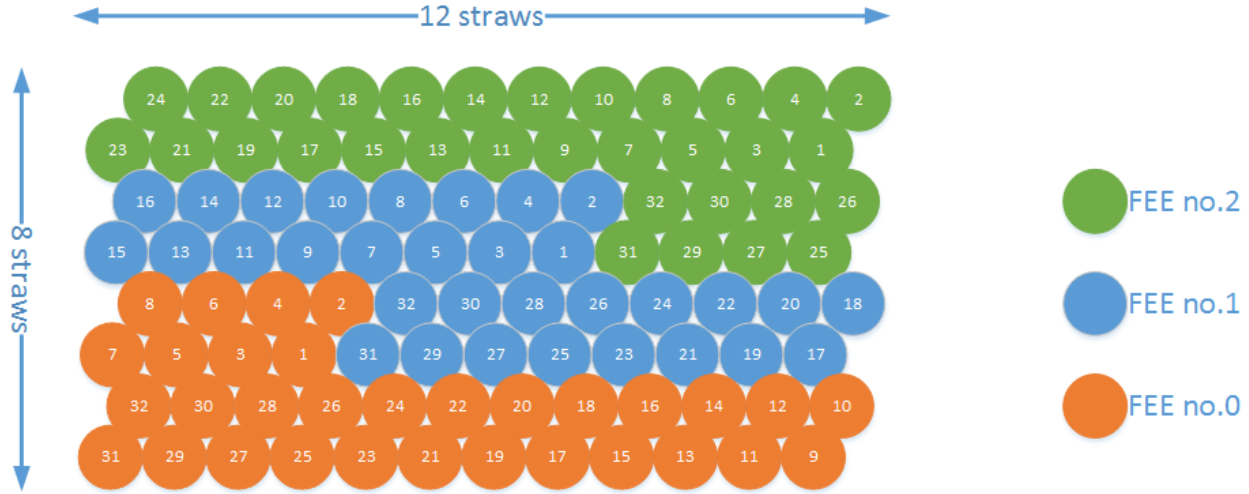
From Cracow

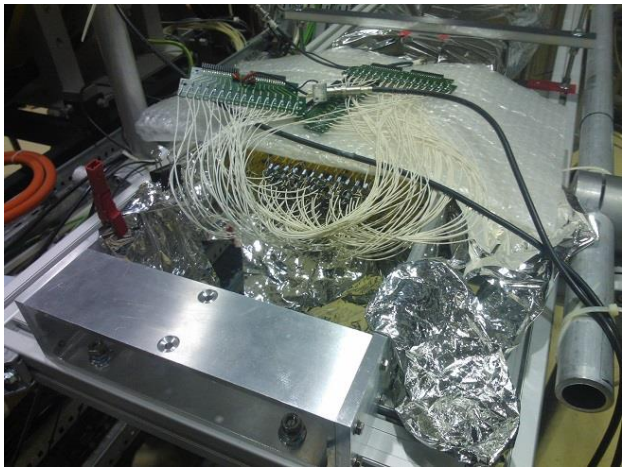
The Setup at Juelich



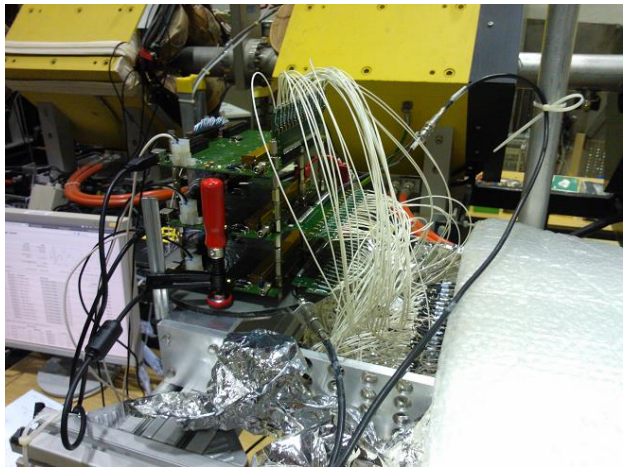
The Setup at Juelich

- Straws mapping



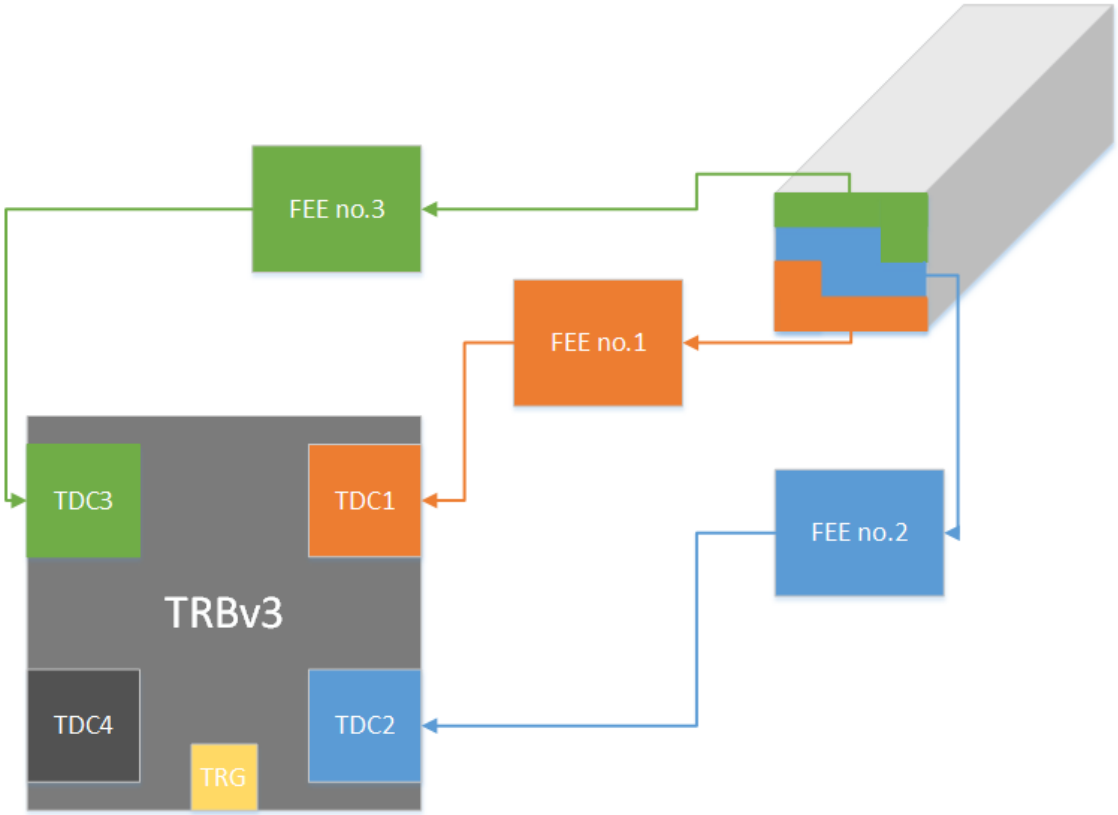


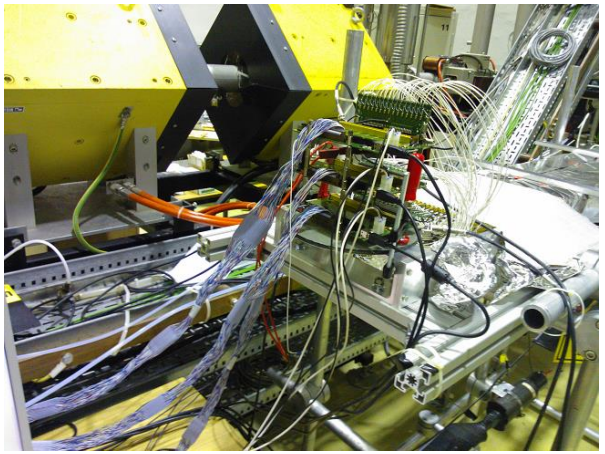
Thanks to Stephan!

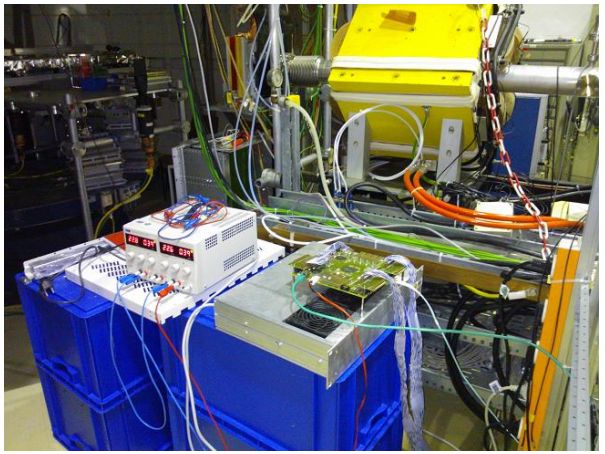


The Setup at Juelich

- FEE boards connection

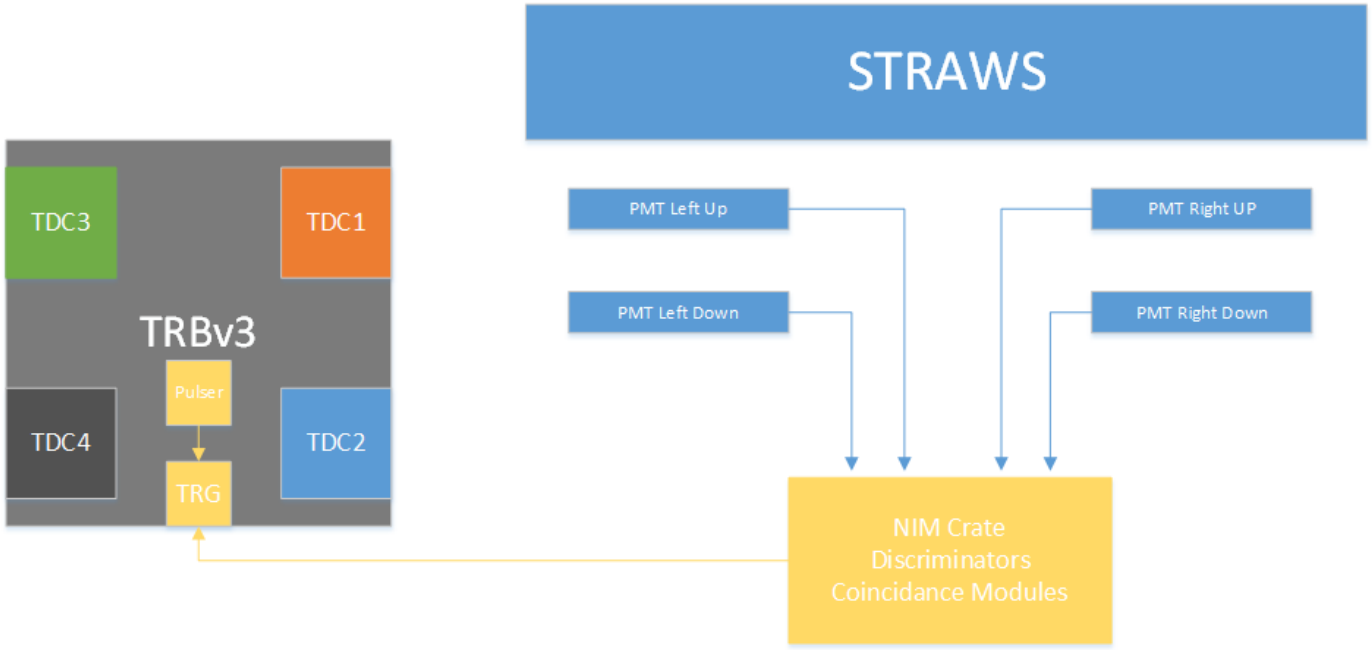






The Setup at Juelich

- Triggering:
  - Internal pulser
  - Any PMTs configuration
  - Trigger saved by TDCs as reference channel



Slow Control and Monitoring

- Startup scripts
- Central Trigger System

Integrated on central FPGA

- Gigabit Ethernet

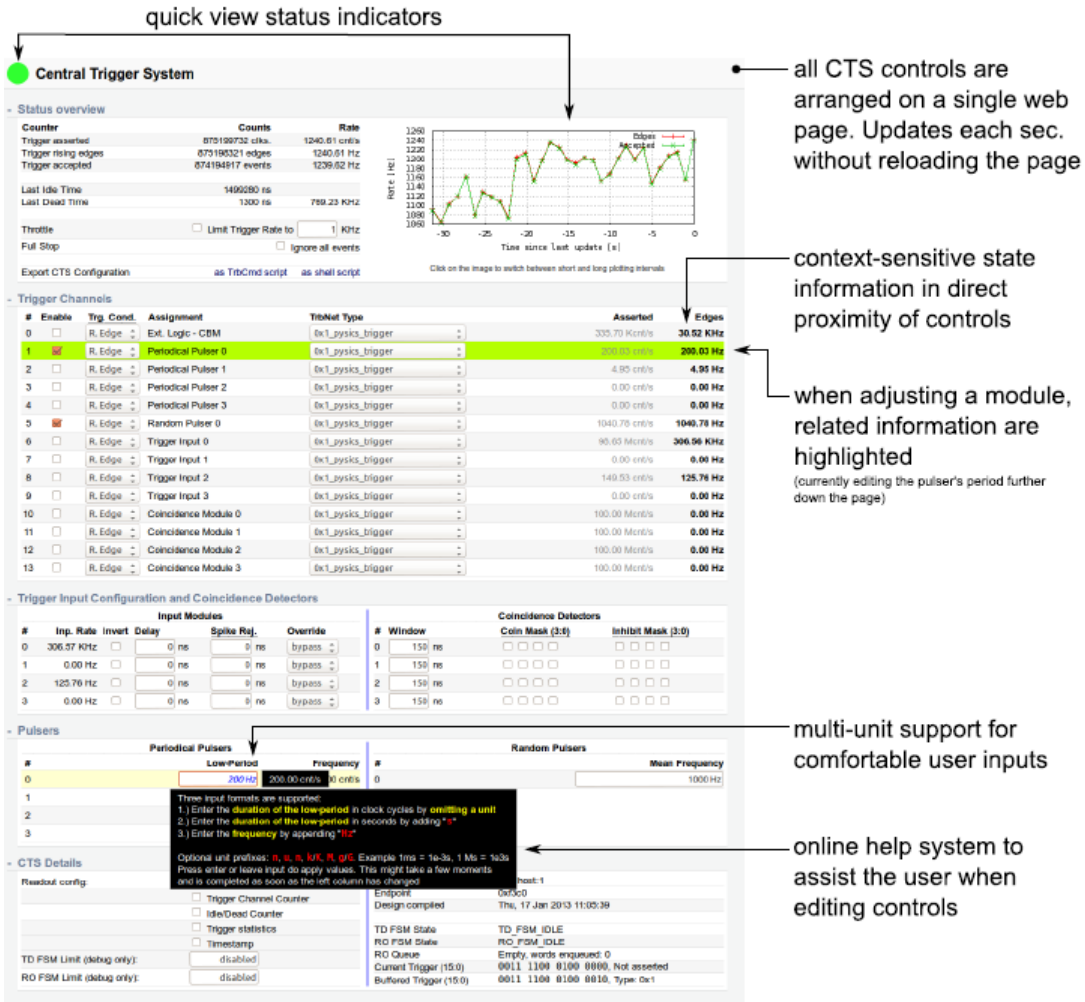
connectivity

- Web-based interface
- Real-time monitoring and

register status

  - Trigger rates
  - Individual TDC channel

    scalers

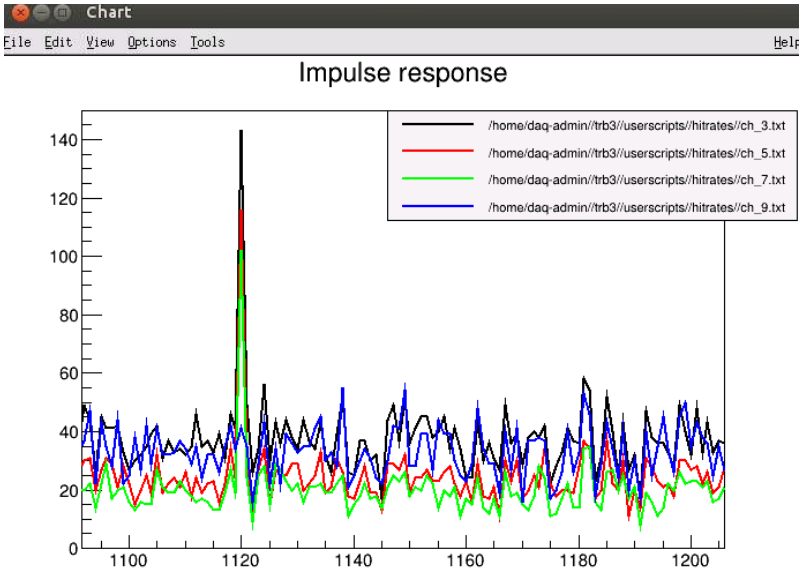


A. Neiser – JINST_012P_1113

Slow Control and Monitoring

- TDC scalers

Reg	Channel	e100	e101	e102	e103
c000	0	0	0	0	0
c001	1	554	8	0	0
c002	2	554	8	0	0
c003	3	28	17	2	0
c004	4	28	17	2	0
c005	5	18	10	3	0
c006	6	18	10	3	0
c007	7	15	10	6	0
c008	8	15	10	6	0
c009	9	29	7	4	386
c00a	10	29	7	4	386
c00b	11	3	9	11	0
c00c	12	3	9	11	0
c00d	13	38	13	4	0
c00e	14	38	13	4	0
c00f	15	26	15	1	0
c010	16	26	15	1	0
c011	17	51	12	6	0
c012	18	51	12	6	0
c013	19	48	14	5	0
c014	20	48	14	5	0
c015	21	71	9	2	0
c016	22	71	9	2	0
c017	23	84	7	1	0
c018	24	84	7	1	0
c019	25	99	4	1	0
c01a	26	[illegible]	4	1	0
c01b	27	91	5	7	0
c01c	28	91	5	7	0
c01d	29	93	0	4	0
c01e	30	93	0	4	0
c01f	31	73	4	3	171707
c020	32	73	4	3	171610
c021	33	63	5	5	0
c022	34	63	5	5	0
c023	35	66	4	6	0
c024	36	66	4	6	0

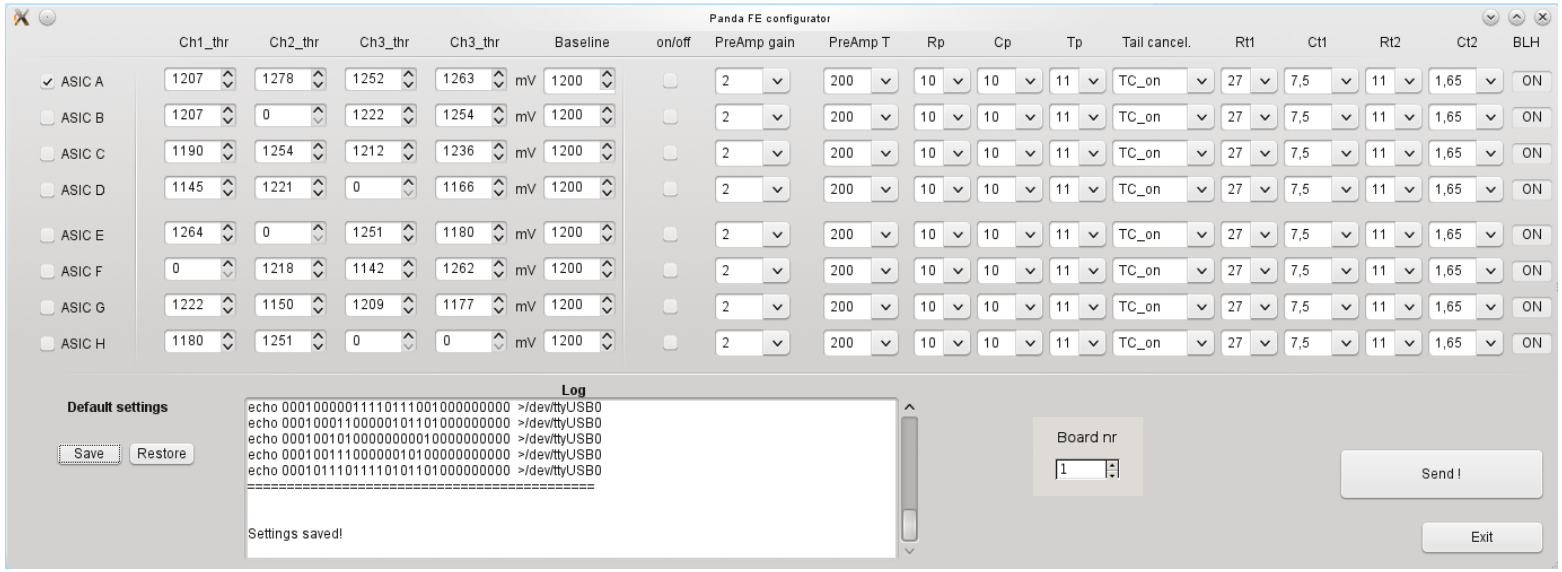


- Easy thresholds setup
- Online monitoring of hit rates
  - Noisy channels
  - ASIC configuration loss
- Hit rate logger

Slow Control and Monitoring

Paweł Strzempek

- Cracow ASIC FEE controller
  - USB communication
  - Multiple boards support
  - Logging



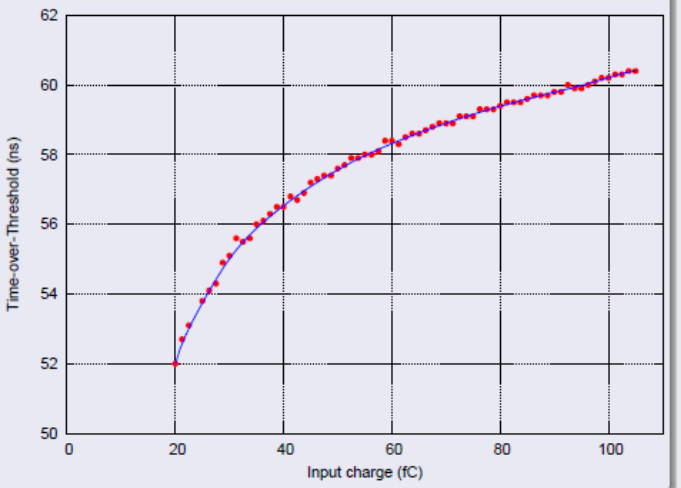
Summary

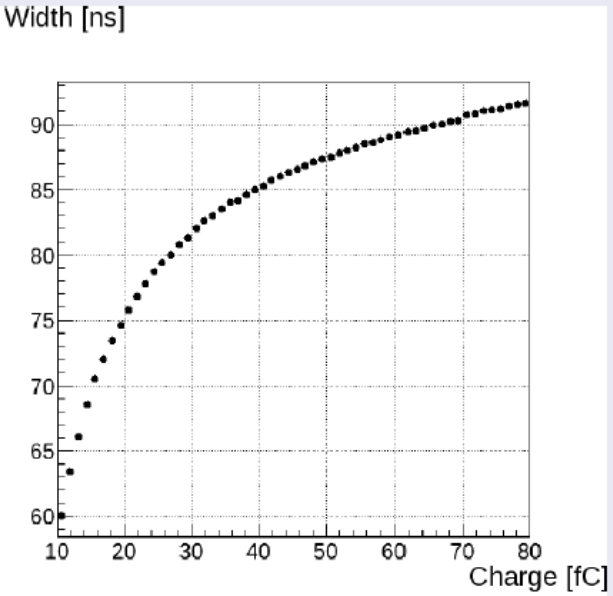
- The setup in Juelich is prepared and ready for data taking
- TRBv3 used as standalone TDC platform
- Already some interesting data gathered

  (see the following talk of Jacek)

Backup

Measurement results
Time–over–Threshold





Results achieved for delta pulse and different FEE settings