

# FPGA-based read-out systems

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# FPGA-based read-out systems

- FPGA based systems
- HADES DAQ Upgrade
- Use cases
- Synergies between experiments
- New Developments

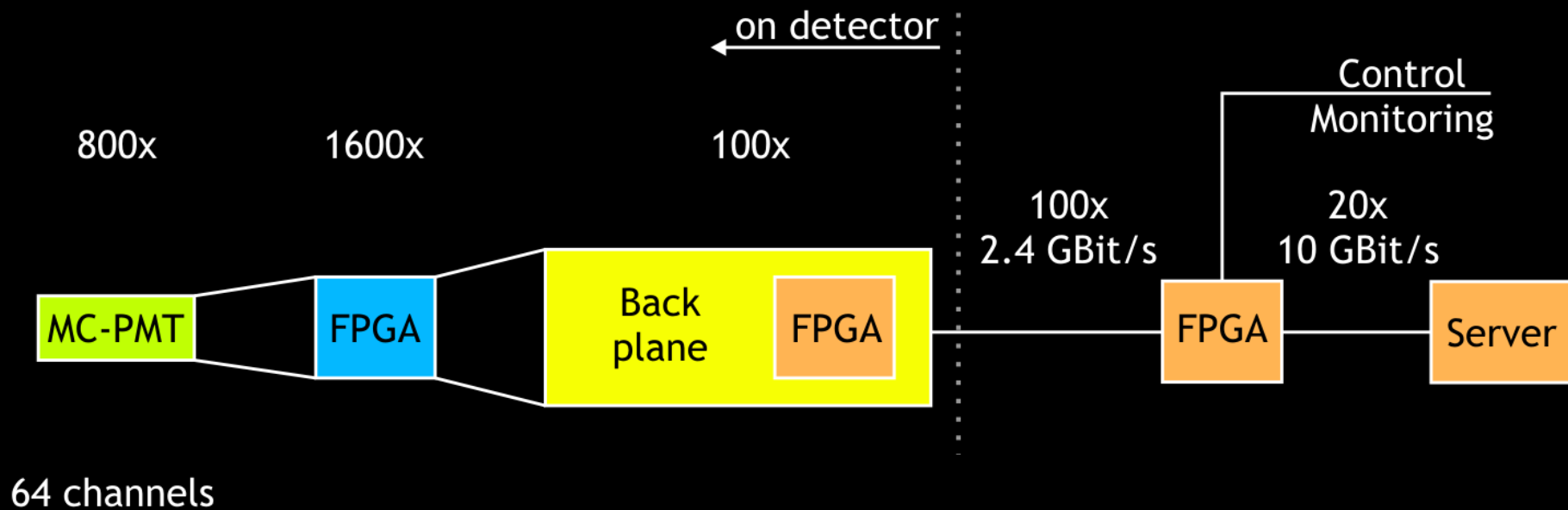
# FPGA-based Data Acquisition

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- A typical DAQ system comprises:
  - Very many channels ( $> 100k$ )
  - which have to be read-out very often ( $> 100 \text{ kHz}$ )
  - very well synchronized ( $< 100 \text{ ps}$ )
  - producing lots of data ( $> 1000 \text{ MBit/s}$ )
- Can not be done with regular CPUs, but by special ASICs
  - very expensive and complicated
- Perfect environment to employ programmable logic devices

# FPGA as Multi-Purpose Devices

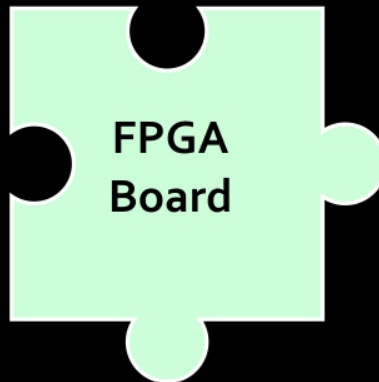
## CBM RICH: Planned read-out chain



# The DAQ Challenge

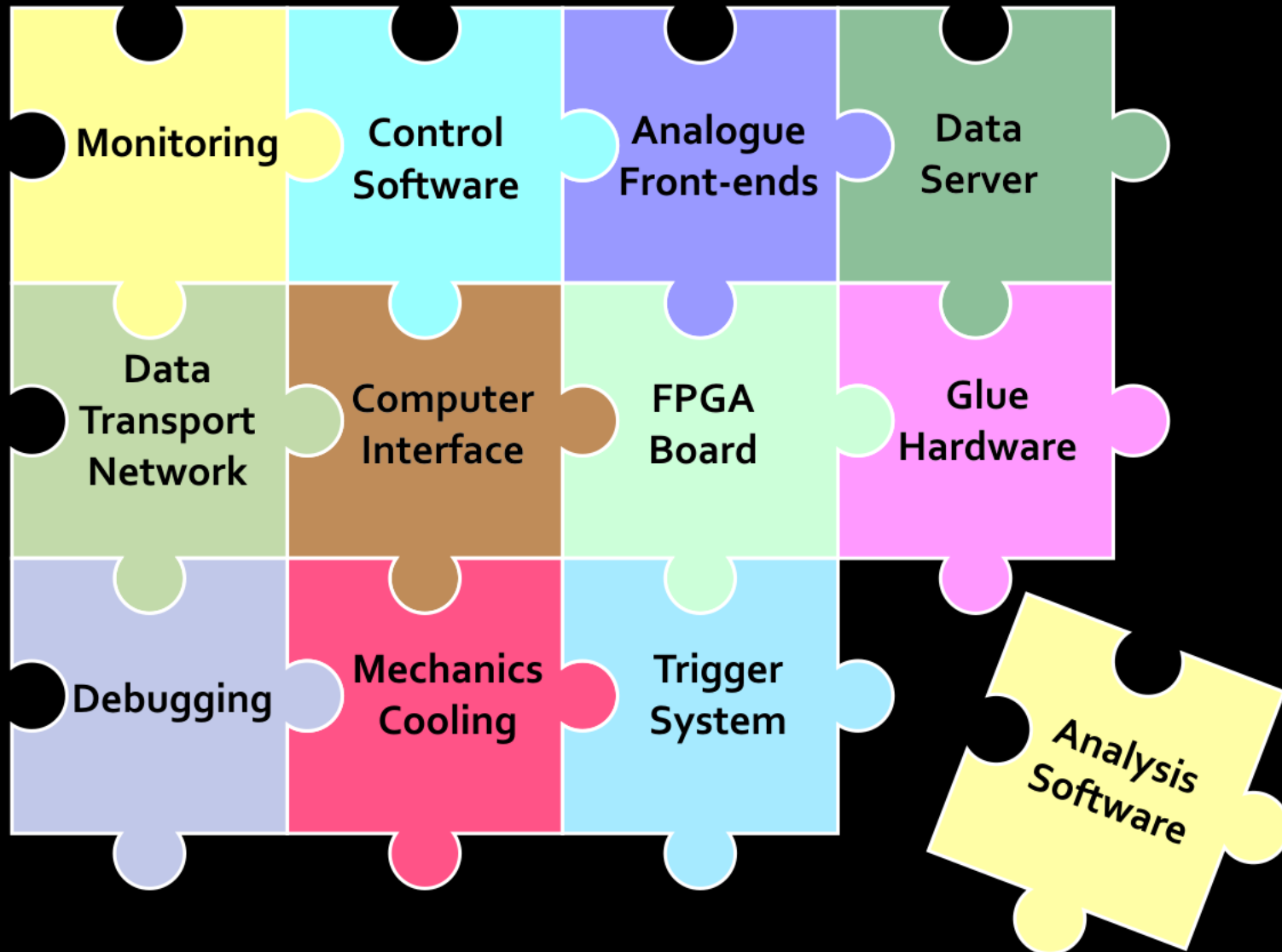
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- Designing hardware is only one part of the story:

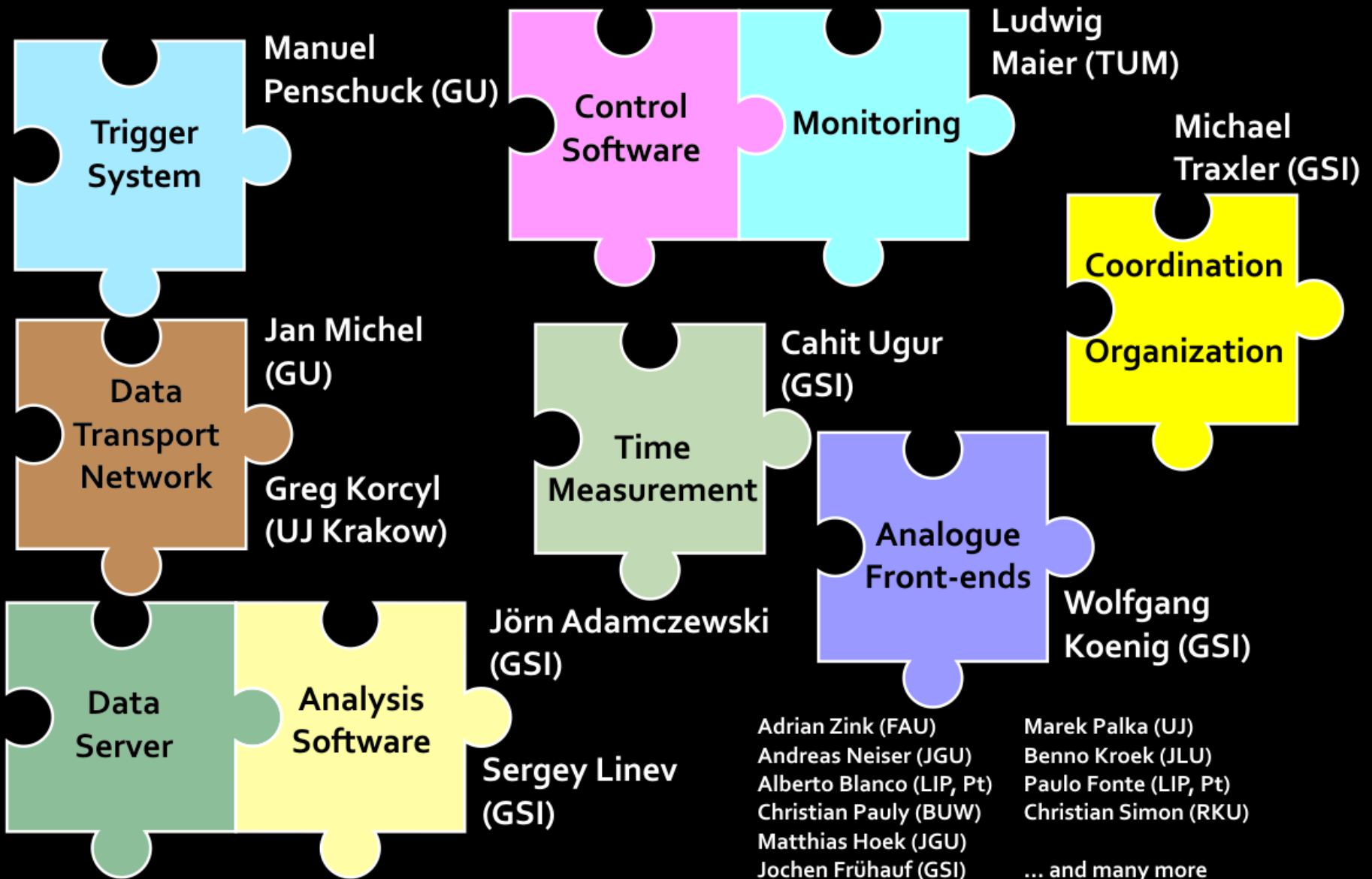


# The DAQ Challenge

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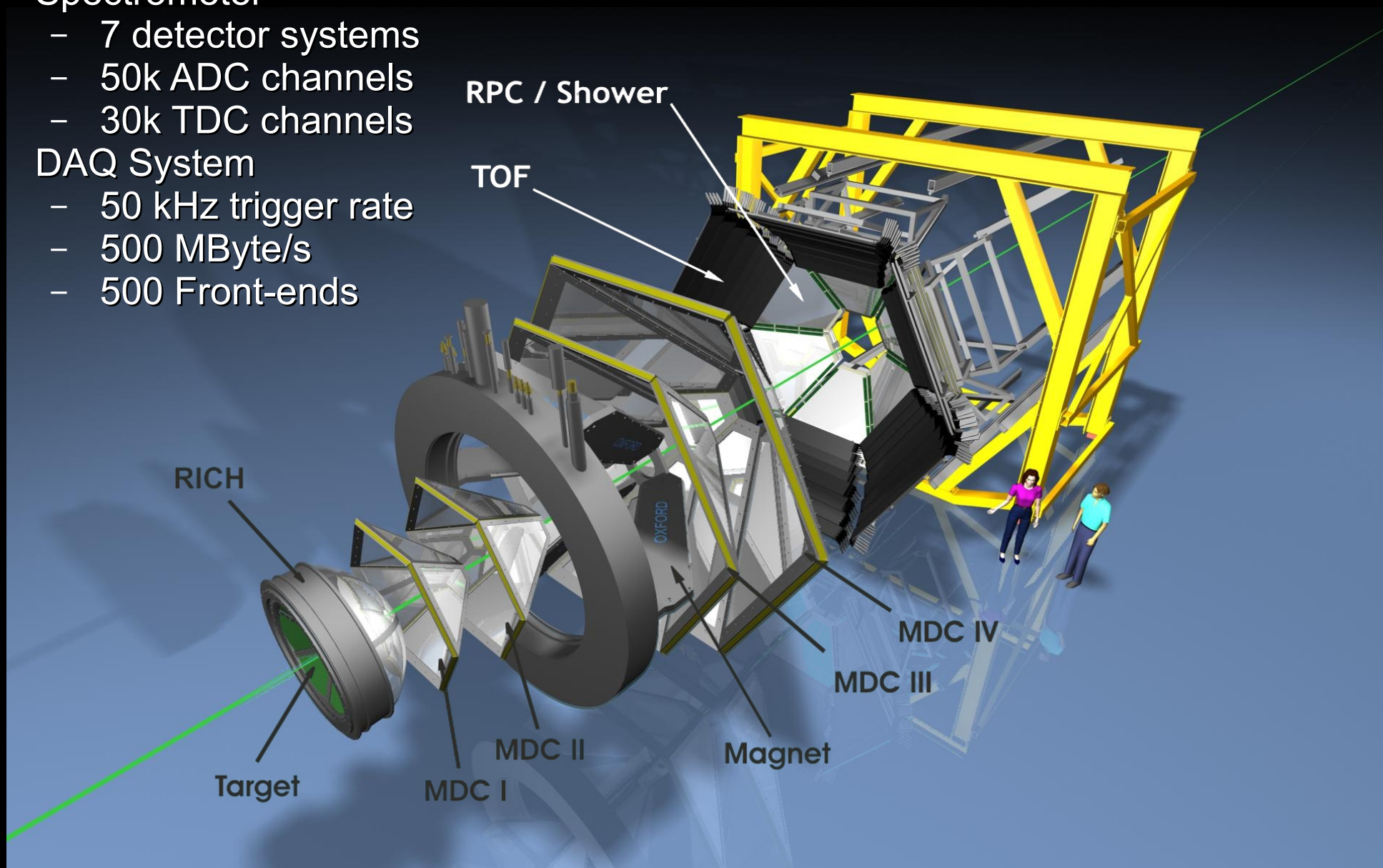


# Divide and Conquer – The TRB concept



# HADES

- Spectrometer
  - 7 detector systems
  - 50k ADC channels
  - 30k TDC channels
- DAQ System
  - 50 kHz trigger rate
  - 500 MByte/s
  - 500 Front-ends



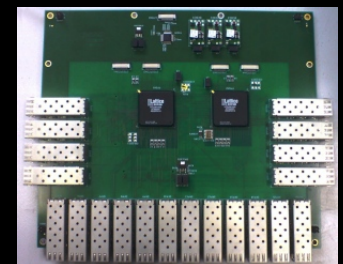
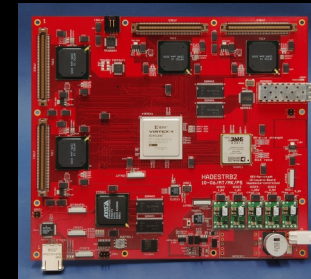
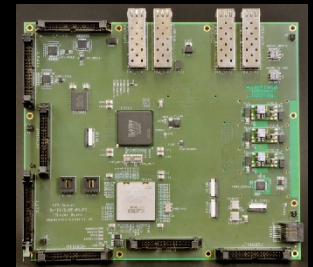
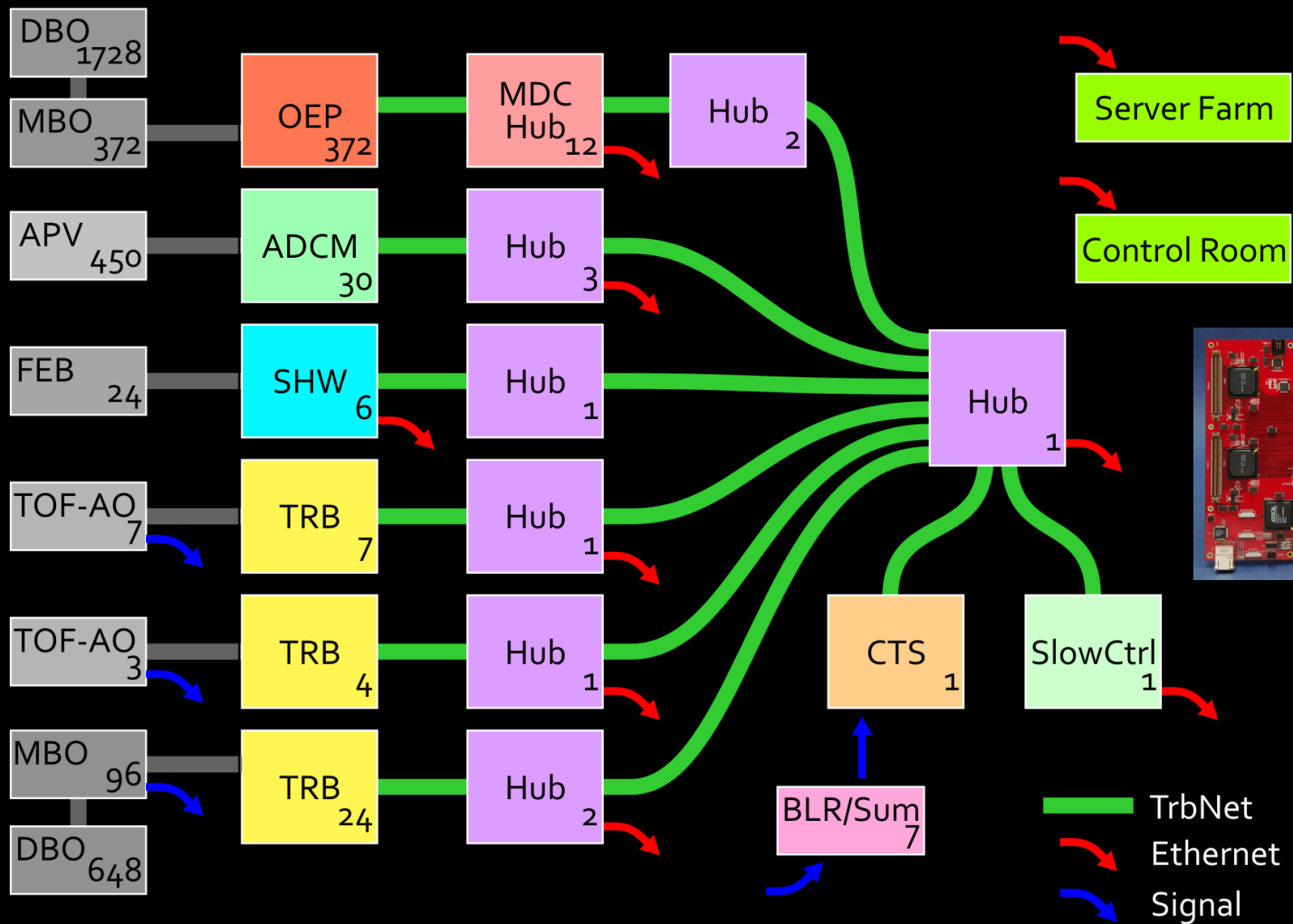


# HADES Upgrade Program

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- Complete DAQ upgrade 2007 - 2012
  - preparation for gold beam in 2012 (20 kHz interaction)
  - increase data rate capabilities 30-fold
- Further upgrades planned for operation at FAIR
  - Calorimeter, drift chamber read-out
- Au+Au @ 1.23 AGeV/u in April 2012
  - 7 billion events, 150 TByte of data
- $\pi$  + p in August 2014

# HADES Upgrade Developments



# Slow-Control / Monitoring

- Easy-to-use monitoring tools are very important, but often ignored
  - during experiments several weeks long, experts are rare!
  - Developments can be shared between users of similar systems

14:21:42 Tactical Overview

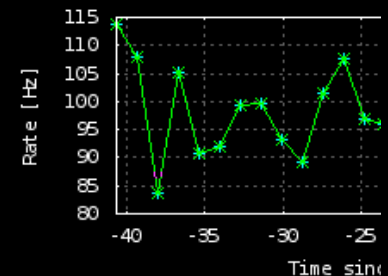
Main	Wall Clock 14:21:41	Current Rate 10377	Online QA	Last Restart 45m50s ago	Speech Output running
DAQ	TrbNet OK	Timeouts on 0 boards	Busy 12.6%	Read-out	Spill Count
Trig	Spill Sum No Spills	Accept. PT1 0% / 0%	Trigger Source 10.0kHz M2C	Start/PT1 0.00	Hodo Count 16 / 0
Rate	PT1 Rate 1.3k / 0	Start Rate 570 / 0	Hodo Rate 14 / 1	Pion1 Rate 274k / 0	Pion2 Rate 583 / 0
Srv	Disk Level 93%	Max. CPU 43%	Icinga OK	TRB OK	Pwrsply OK
EB	#EB running act. 3/3 (te)	ΔRate EB-CTS -436 (-5%)	Data Rate 73 MB - 7 kB	#Evt Discarded 25	#Evt w/ errors 0 (0.0%)
MDC	MBO Reinit	MBO w/o data 81 errors	Temperature 65/62/59/58	Link Errors	Voltages 39 warnings
Endp	MDC system OK	RICH system OK	TOF system OK	RPC system OK	Sh/FW/SN/CTS OK
Fee	Rich APVs	TRB TDC	FEE Error	Trg. Inputs	Trigger
Pion	NX Status OK	Pion 0 HV 158.6/0.580	Pion 1 HV 159.4/1.048	Pion Cool -20.0° / -20.1°	Pion SED
Other	Magnet	RICH HV 2.50 / 2.50 kV	Shower Data rates	MDC HV 1.7/1.0/1.0/1.0	HV Sequencer 70/70

Other-MDC HV (14:21:41): Error  
MDC high voltage in all four planes  
Minimum [V]: 1748.75 / 999.5 / 999 / 999.5  
Maximum [V]: 1749.25 / 1000.25 / 999.75 / 1000.25  
Nominal [V]: 1750 / 1770 / 1500 / 1700

## Central Trigger System

### - Status overview

Counter	Counts	Rate
Trigger asserted	1215509051 clks.	104.46 s <sup>-1</sup>
Trigger rising edges	7691389 edges	104.46 Hz
Trigger accepted	11432020 events	104.46 Hz
Last Idle Time	230120 ns	
Last Dead Time	1300 ns	769.23 KHz

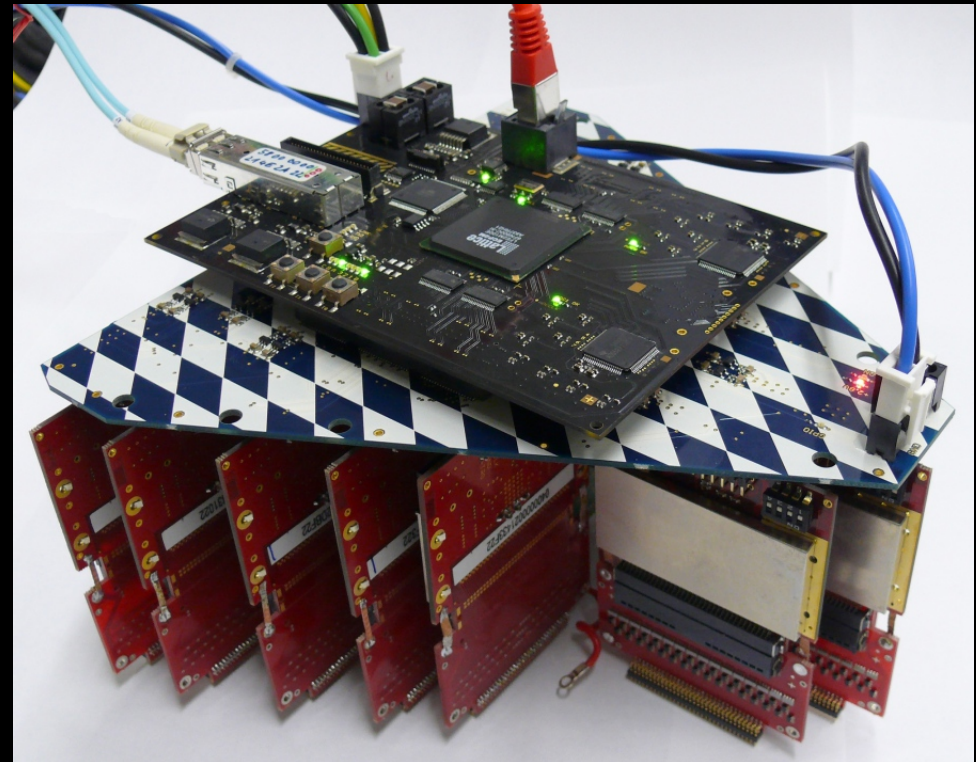


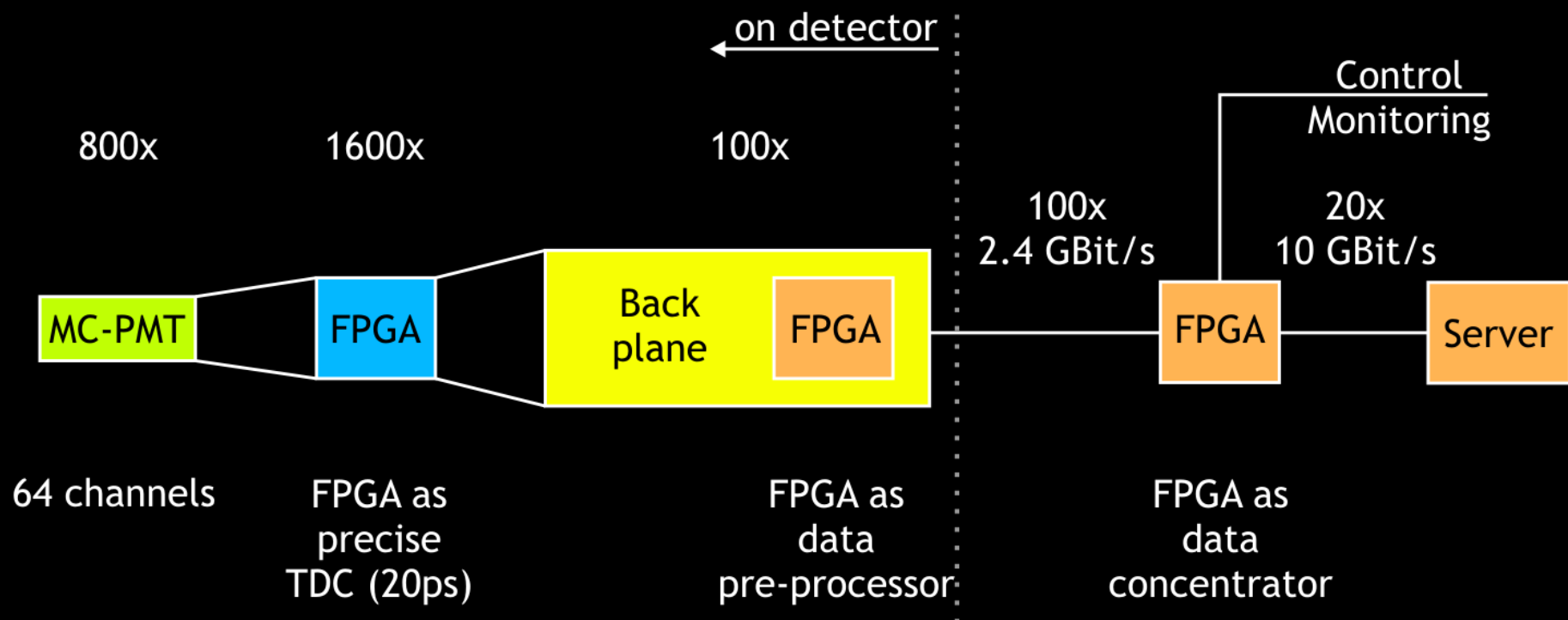
0240	0241	0242	0243	0250	0251	0252	0253
40.4	45.3	41.4	44.6	37.4	36.0	35.1	35.4
42.2	45.1	43.6	45.3	40.9	39.6	36.5	37.5
42.5	42.7	41.9	---	42.9	41.7	37.9	39.9
43.6	43.8	43.8	---	43.6	42.6	39.6	40.6

# FPGA - “Traditional” Fields

- Bridge to other connections
  - Ethernet, PCIe
- Buffering & Transporting data
- Controlling external components
- Pre-processing of data

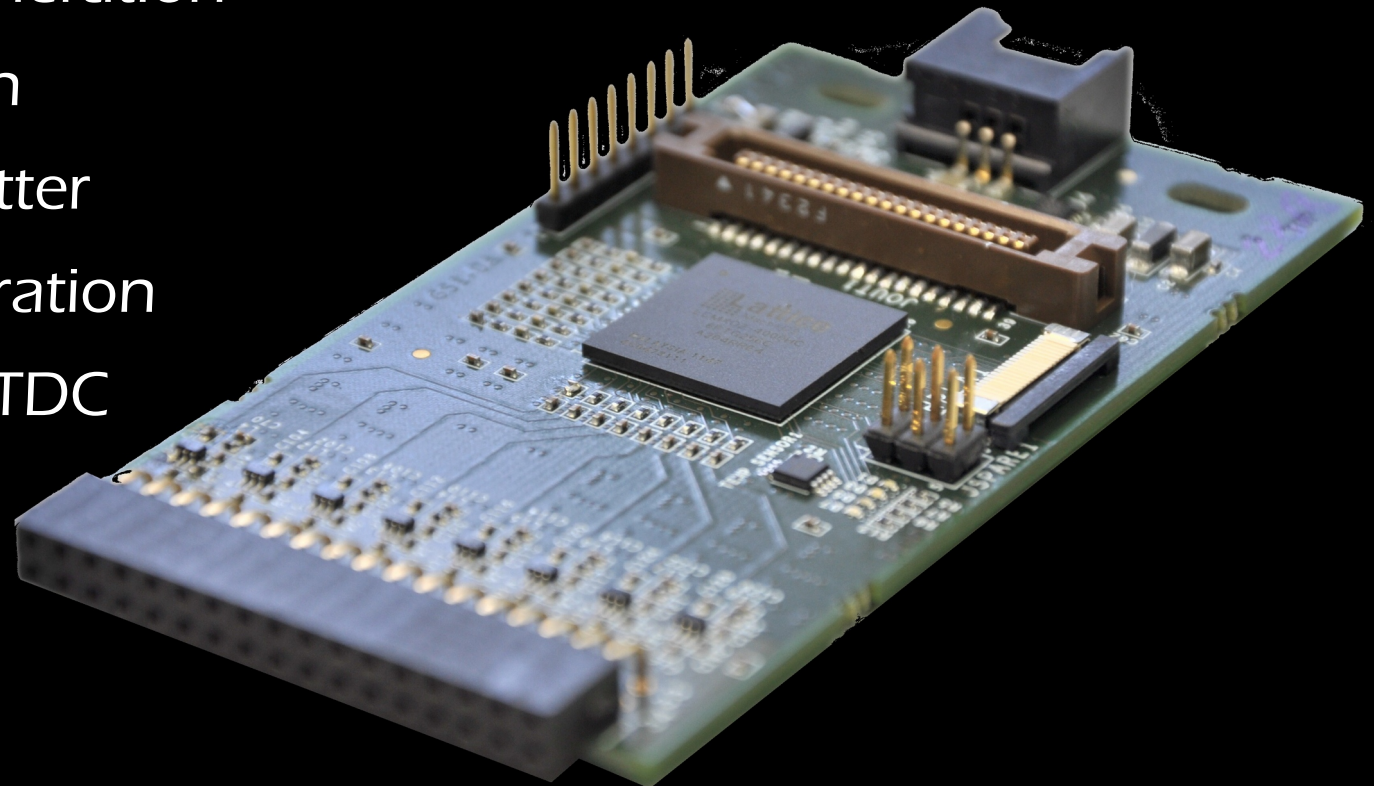
HADES RICH Electronics





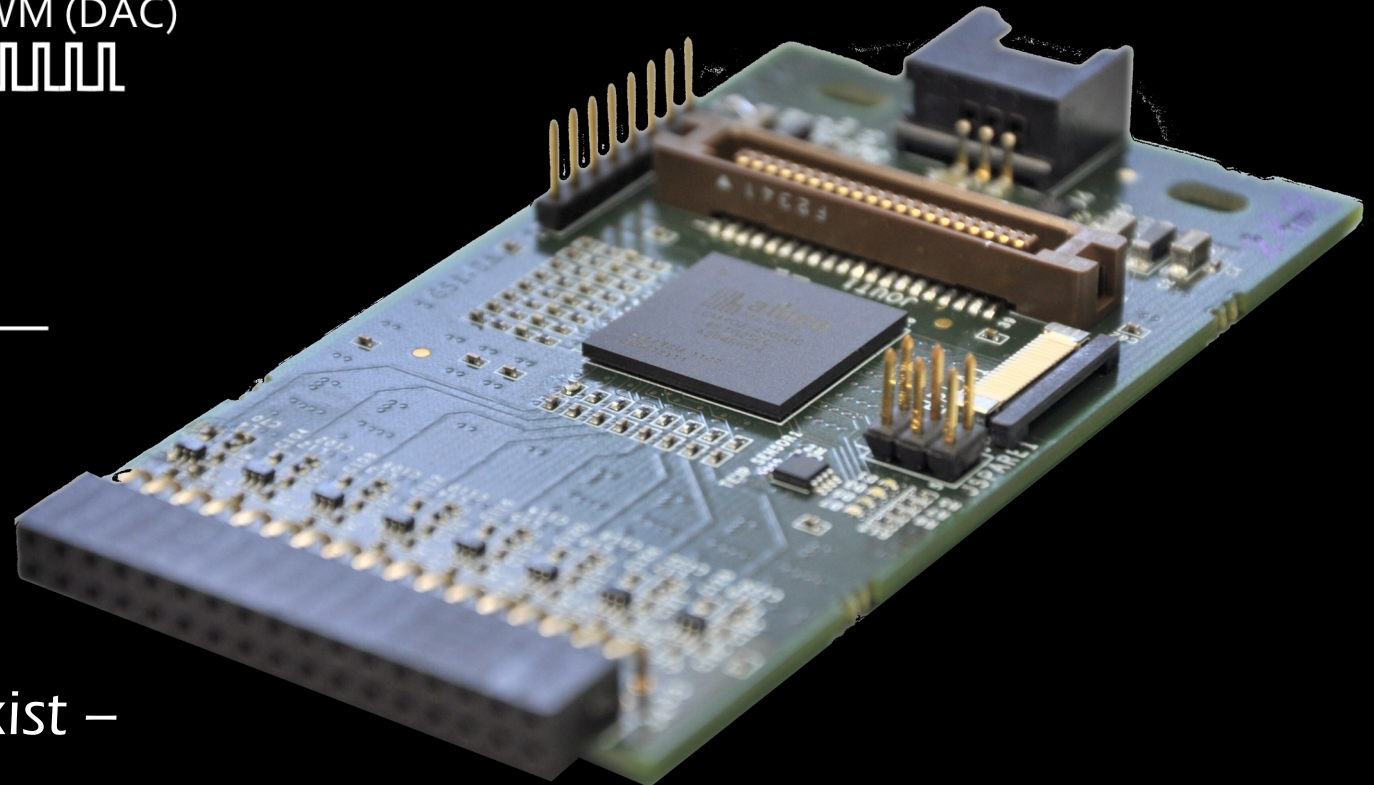
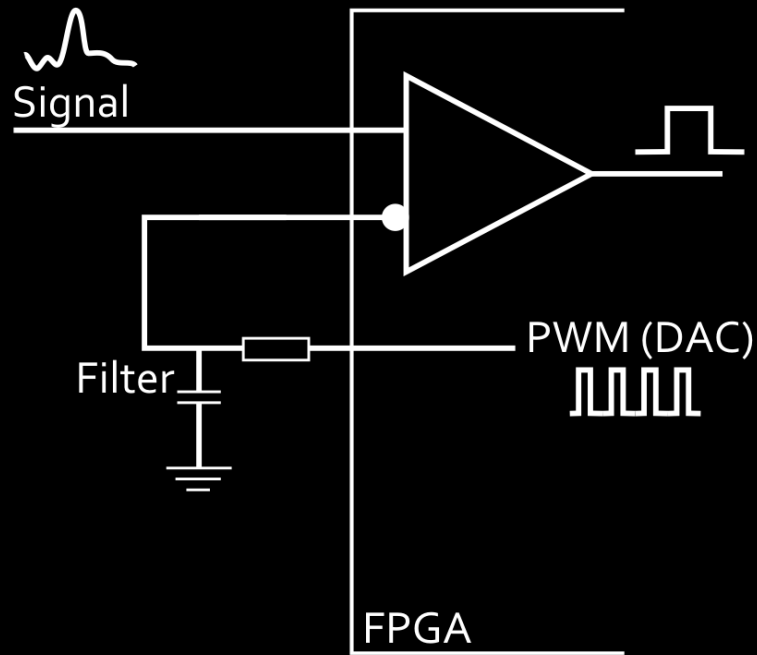
# FPGA – replacing front-end electronics

- Plug-on module for e.g. MC-PMTs
- Amplifiers in discrete off-the-shelf components
- FPGA does everything else
  - Threshold generation
  - Discrimination
  - LVDS transmitter
  - Trigger Generation
- Could do 500ps TDC
- active comp.:  
< 3€ / chan.





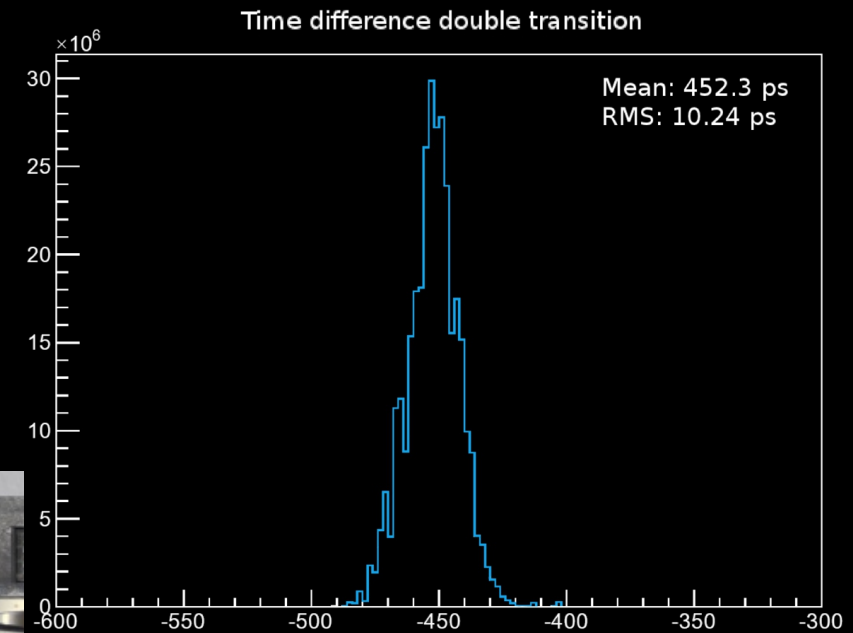
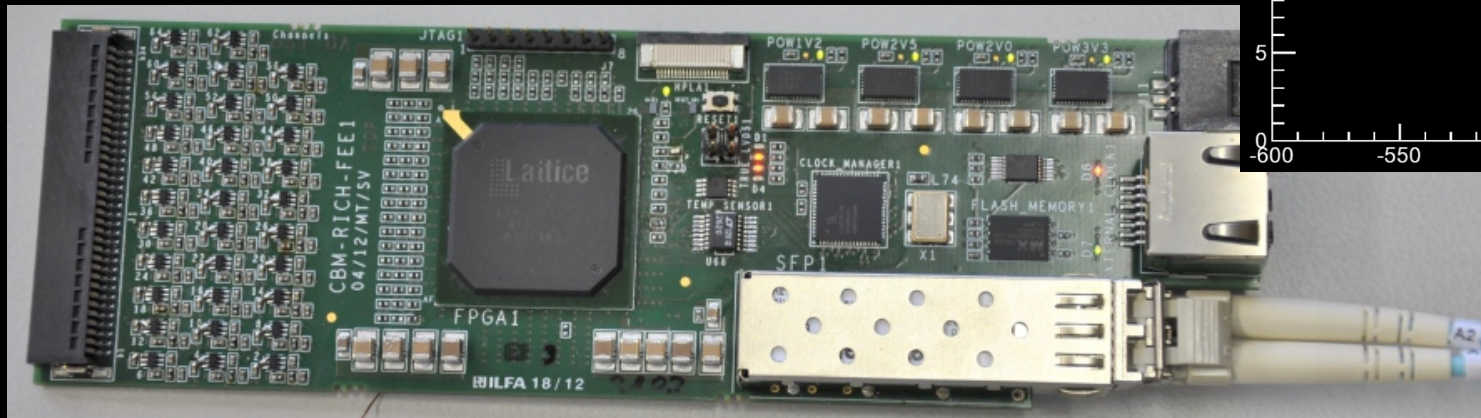
# FPGA – replacing front-end electronics



- Discriminators exist – for LVDS inputs

# FPGA – Precision Time Measurement

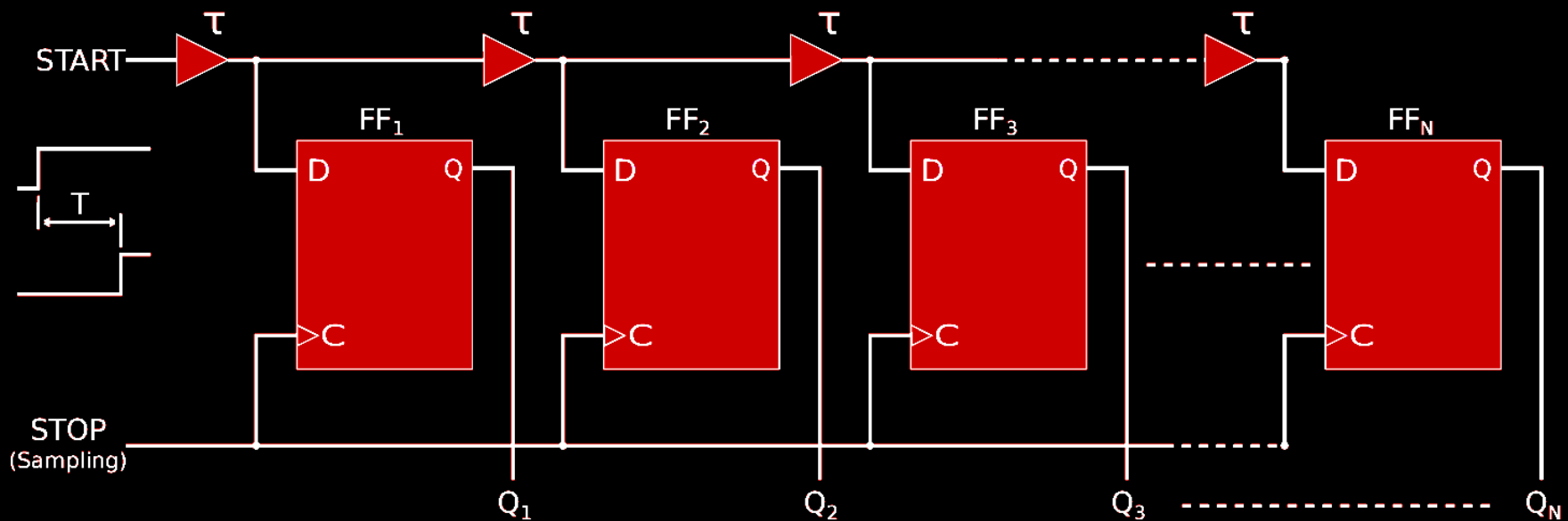
- TDC-in-FPGA technology now in use by many groups at GSI/FAIR
  - CBM, Hades, PANDA, R3B ...



FPGA run at few 100 MHz – how can they measure 10 ps !?

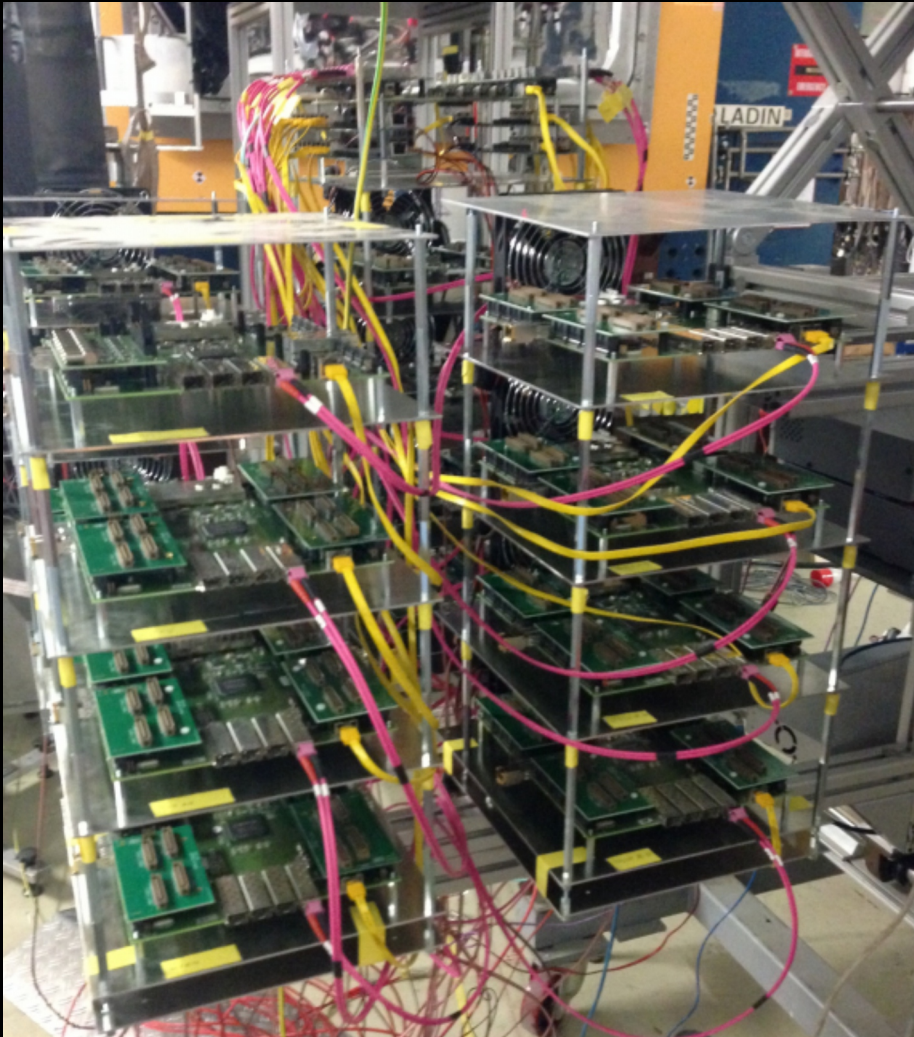


# FPGA – Precision Time Measurement

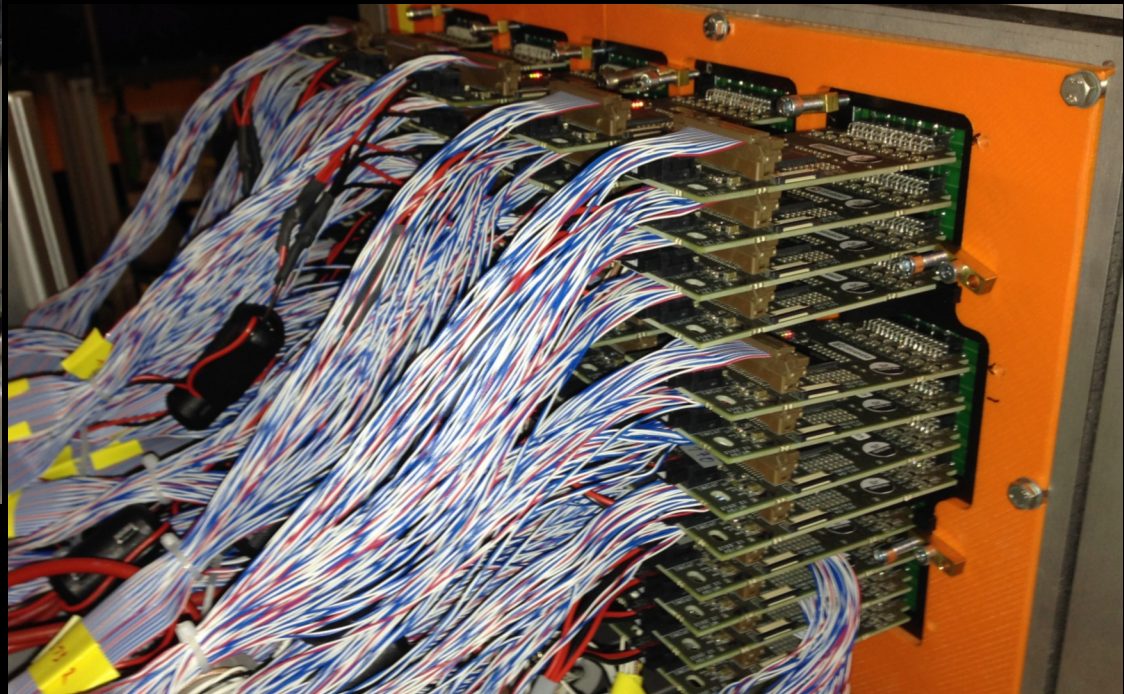


- Some key features for a “standard configuration”
  - < 20 ps precision (RMS)
  - up to 48 channels per FPGA, (<10€/chan incl. read-out)
  - high multi-hit capability
  - > 50 MHz/channel peak
- Everything subject to setup-specific adjustments

# Synergies – not only in development



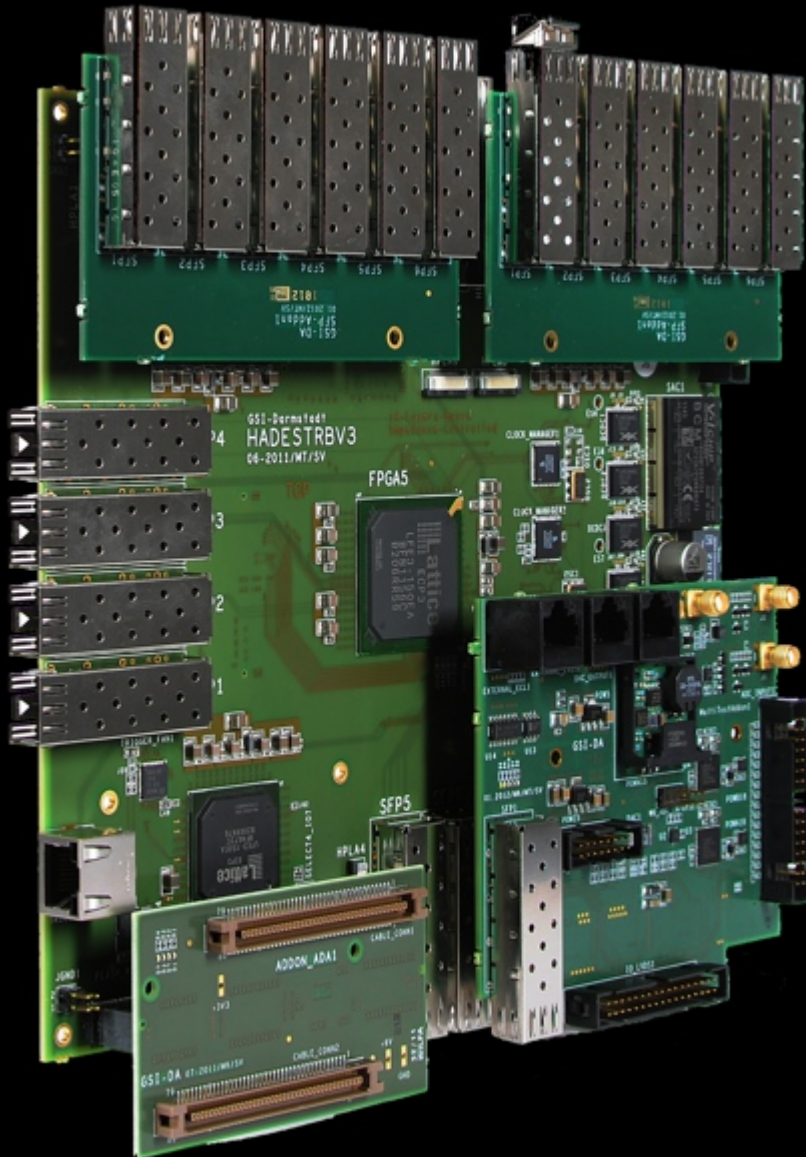
- Panda Barrel DIRC prototype test  
September @ GSI
  - > 1000 channels PreAmp & TDC
- Same hardware currently being  
prepared for  
CBM RICH test, November @ CERN



Pictures: Jochen Schwiening



# A general purpose platform: TRB3



- FPGA platform
  - 5 ECP3 FPGA
  - 8 SFP
- 5 AddOn connectors
  - 208 I/O incl. 6 Serdes
- Stand-alone operation
  - GbE for communication

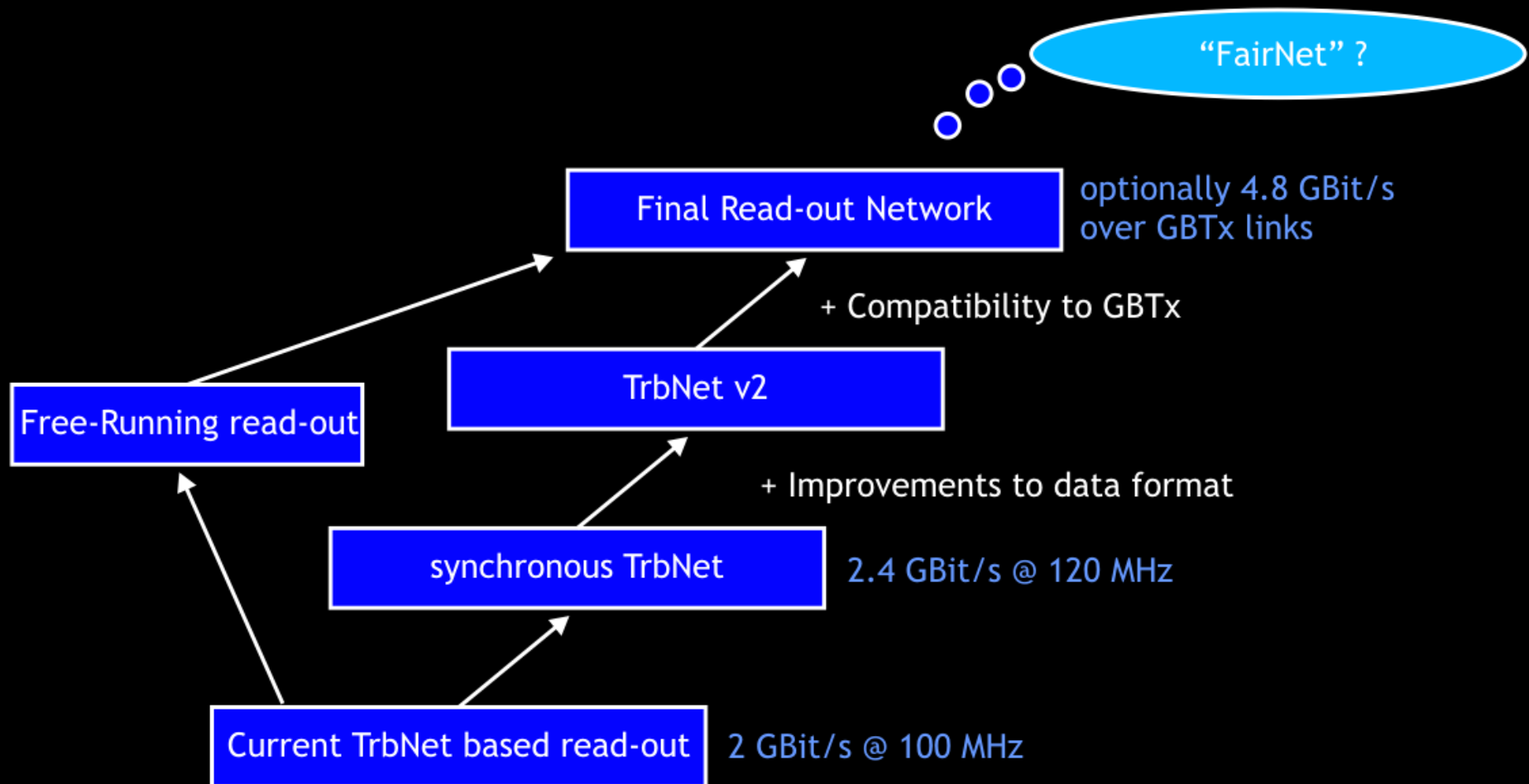
# CBM MVD

- CBM RICH & CBM MVD
  - very different systems
  - 50k PMT channel vs. fully integrated MAPS pixel sensors (900 cm<sup>2</sup> / 150MPixel)
- Based on the same read-out platform
- Will use the same read-out network



# Outlook: Network

- The existing programming does not fit to all needs of FAIR experiments, but can be adapted



# Conclusion

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- FPGA Platforms are a very versatile tool for many aspects of data taking.
  - can easily be adapted to any needs
  - can also serve to work in the analog world
- The TRB3 collaboration has become a huge project
  - > 20 user groups world-wide
  - lively discussion, many people testing new features
- Hardware from the TRB project - not only in physics
  - in medicine (human PET – LIP Coimbra) and
  - in geology (x-ray scanning of corals)