Contribution ID: **20** Type: **not specified**

Overview of the STS-XYTER – a dedicated front-end chip for the CBM Silicon Tracking System

The STS-XYTER is a 128-channel charge-sensitive front-end chip, designed specifically for the Silicon Tracking System of the CBM experiment. The chip features a self-triggering architecture, which enables it to measure the signal amplitude and the time of arrival in each input channel autonomously, as soon as the signal in the given channel exceeds a predefined threshold. The design time resolution is about 10 ns, the dynamic range is 15 fC, and the amplitude is digitized with an integrated 5-bit flash ADC. Two shapers with distinct rise times are used to achieve low rate of noise hits in combination with the good time resolution, and low power consumption (6 mW/channel). The back end of the current version of the STS-XYTER is capable of transmitting the information of up to about 3*10^7 hits/s over four 500Mbps LVDS links. The characterization of chips samples is ongoing. An overview of the chip architecture as well as the operation principle will be given.

Invited Talk (yes/no)?

no

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